



AK1542

20 to 600MHz Integer-N Frequency Synthesizer

1. Overview

Consisting a highly accurate charge pump that supports current adjustment in 64 steps, a reference divider, a programmable divider and a dual-modulus prescaler (P/P+1), the AK1542 provides high performance, low consumption current and small footprint for a wide range of frequency conversions . This synthesizer also has two general-purpose output pins which allow it to be used to control the RF front end.

An ideal Phase Locked Loop (PLL) can be achieved by combining the AK1542 with the external loop filter and VCO (Voltage Controlled Oscillator). Access to the registers is controlled via a 3-line serial interface. The operating supply voltage is from 2.7 to 5.5V; and the supply voltage for the charge pump and that for the serial interface can be driven separately.

2. Features

- Operating frequency: 20 to 600MHz
- Programmable charge pump current: 106 to 6784uA typical
 The charge pump current can be changed in 64 steps; and the current range can be adjusted by the external resistance.
 Two current settings can be specified with the register and switched over from one to another using the timer.
- Supply Voltage: 2.7 to 5.5 V (PVDD and CPVDD pins)
- Separate power supply for the charge pump: PVDD to 5.5V (CPVDD pin)
- On-chip power-saving features
- On-chip lock detection feature of PLL: Direct output to the PFD (Phase frequency detector) or digital filtering output can be selected.
- General-purpose output: It has two general-purpose output ports to control peripheral parts.
- Consumption current: 3.4mA typical (excluding a charge pump current)
- Package: 24pin QFN (0.5mm pitch, 4mm x 4mm x 0.75mm)
- Operating temperature: -40C° to 85C°

Table of Contents

1.	Overview	1
2.	Features	1
3.	Block Diagram	3
4.	Pin Functional Description	4
5.	Absolute Maximum Ratings	6
6.	Recommended Operating Range	6
7.	Electrical Characteristics	7
8.	Block Functional Descriptions	11
9.	Register Map	20
10.	Register Function Description	22
11.	IC Interface Schematic	30
12.	Recommended Schematic for Off-Chip Component	32
13.	Power-up Sequence	34
14.	Typical Evaluation Board Schematic	35
15.	Block Diagram by Power Supply	36
16.	Outer Dimensions	37
17.	Marking	38

In this specification (draft version), the following notations are used for specific signal and register names:

[Name]: Pin name

<Name>: Register group name (Address name)

{Name}: Register bit name

3. Block Diagram

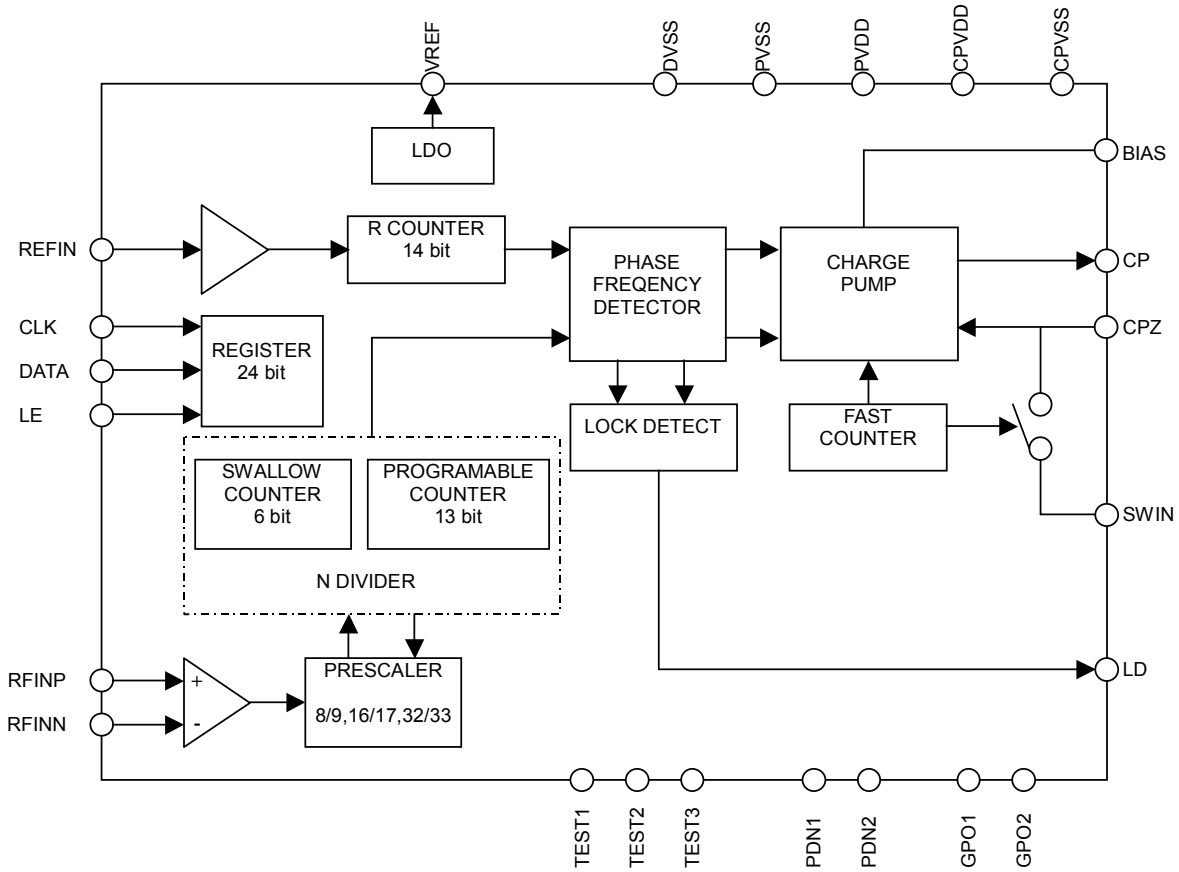


Fig. 1 Block Diagram

4. Pin Functional Description

Table 1 Pin Functions

No.	Name	I/O	Pin Functions	Power down	Remarks
1	CPVDD	P	Power supply for charge pump		
2	TEST3	DI	Test pin 3		Internal pull-down, Schmidt trigger input
3	TEST1	DI	Test pin 1		Internal pull-down, Schmidt trigger input
4	LE	DI	Load Enable		Schmidt trigger input
5	DATA	DI	Serial data input		Schmidt trigger input
6	CLK	DI	Serial clock		Schmidt trigger input
7	LD	DO	Lock detect	“Low”	
8	PDN2	DI	Power down pin for PLL		Schmidt trigger input
9	PDN1	DI	Power down signal for LDO		Schmidt trigger input
10	REFIN	AI	Reference input		
11	TEST2	DI	Test pin 2		Internal pull-down, Schmidt trigger input
12	GPO1	DO	General-purpose output pin 1	“Low”	
13	GPO2	DO	General-purpose output pin 2	“Low”	
14	DVSS	G	Digital ground pin		
15	VREF	AO	Connect to LDO reference voltage capacitor	“Low”	
16	RFINN	AI	Prescaler input		
17	RFINP	AI	Prescaler input		
18	PVDD	P	Power supply for peripherals		
19	BIAS	AIO	Resistance pin for setting charge pump current		
20	PVSS	G	Ground pin for peripherals		
21	CP	AO	Charge pump output	“Hi-Z”	
22	CPZ	AIO	Connect to the loop filter capacitor		Notes 1) & 2)
23	SWIN	AI	Connect to resistance pin for fast lockup		Notes 1) & 2)
24	CPVSS	G	Ground pin for charge pump power supply		

Note 1) For detailed functional descriptions, see the section “Charge Pump and Loop Filter” in “8. Block Functional Description” below.

Note 2) The input voltage from the [CPZ] pin is used in the internal circuit. The [CPZ] pin must not be open even when the fast lockup feature is unused. For the output destination from the [CPZ] pin, see

“P.14 Fig.5 Loop Filter Schematic”. The [SWIN] pin could be open even when the first lockup feature is not used.

Note 3) Power down refers to the state where [PDN1]=[PDN2]=“Low” after power-on.

AI: Analog input pin	AO: Analog output pin	AIO: Analog I/O pin	DI: Digital input pin
DO: Digital output pin	P: Power supply pin	G: Ground pin	

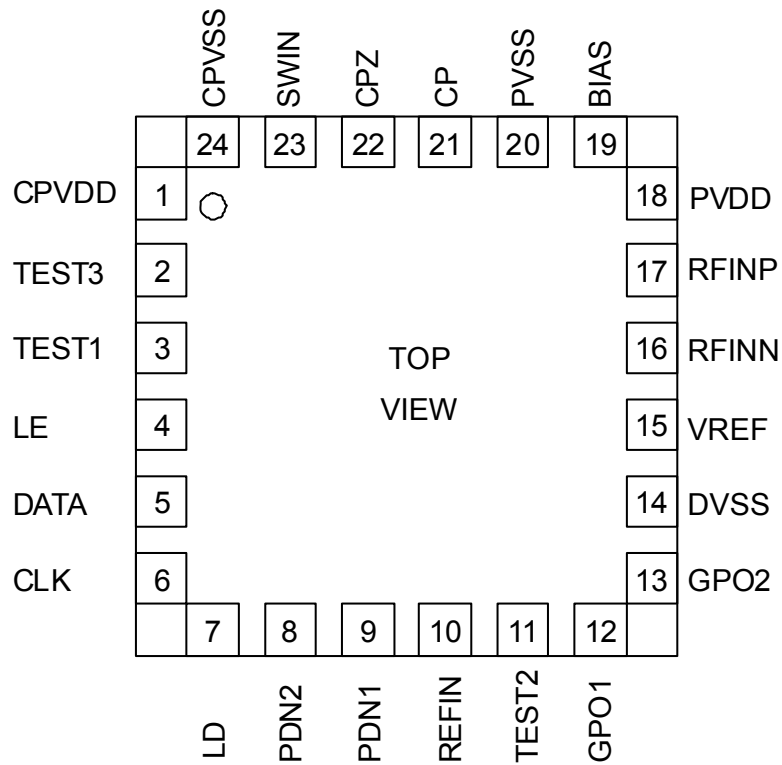


Fig. 2 Package Pin Layout

5. Absolute Maximum Ratings

Table 2 Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit	Remarks
Supply Voltage	VDD1	-0.3	6.5	V	Note 1) Applied to the [PVDD] pin
	VDD2	-0.3	6.5	V	Note 1) Applied to the [CPVDD] pin
Ground Level	VSS1	0	0	V	Voltage ground level applied to the [PVSS] pin
	VSS2	0	0	V	Voltage ground level applied to the [CPVSS] pin
	VSS3	0	0	V	Voltage ground level applied to the [DVSS] pin
Analog Input Voltage	VAIN1	VSS1-0.3	VDD1+0.3	V	Notes 1) & 2)
	VAIN2	VSS2-0.3	VDD2+0.3	V	Notes 1) & 3)
Digital Input Voltage	VDIN	VSS3-0.3	VDD1+0.3	V	Notes 1) & 4)
Input Current	IIN	-10	10	mA	
Storage Temperature	Tstg	-55	125	°C	

Note 1) 0V reference for all voltages.

Note 2) Applied to the [REFIN], [RFINN] and [RFINP] pins.

Note 3) Applied to the [CPZ] and [SWIN] pins.

Note 4) Applied to the [CLK], [DATA], [LE], [PDN1], [PDN2], [TEST1], [TEST2] and [TEST3] pins.

Exceeding these maximum ratings may result in damage to the AK1542. Normal operation is not guaranteed at these extremes.

6. Recommended Operating Range

Table 3 Recommended Operating Range

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
Operating Temperature	Ta	-40		85	°C	
Supply Voltage	VDD1	2.7	3.3	5.5	V	Applied to the [PVDD] pin
	VDD2	VDD1	5.0	5.5	V	Applied to the [CPVDD] pin

Note 1) VDD1 and VDD2 can be driven individually within the recommended operating range.

The specifications are applicable within the recommended operating range (supply voltage/operating temperature).

7. Electrical Characteristics

1. Digital DC Characteristics**Table 4 Digital DC Characteristics**

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Remarks
High level input voltage	Vih		0.8VDD1			V	Note 1)
Low level input voltage	Vil				0.2VDD1	V	Note 1)
High level input current 1	Iih1	Vih = VDD1=5.5V	-1		1	μA	Note 2)
High level input current 2	Iih2	Vih = VDD1=5.5V	27	55	110	μA	Note 3)
Low level input current	Iil	Vil = 0V, VDD1=5.5V	-1		1	μA	Note 1)
High level output voltage	Voh	Ioh = -500μA	VDD1-0.4			V	Note 4)
Low level output voltage	Vol	Iol = 500μA			0.4	V	Note 4)

Note 1) Applied to the [CLK], [DATA], [LE], [PDN1], [PDN2], [TEST1], [TEST2] and [TEST3] pins.

Note 2) Applied to the [CLK], [DATA], [LE], [PDN1] and [PDN2] pins.

Note 3) Applied to the [TEST1], [TEST2] and [TEST3] pins.

Note 4) Applied to the [LD] pin.

2. Serial Interface Timing

<Write-In Timing>

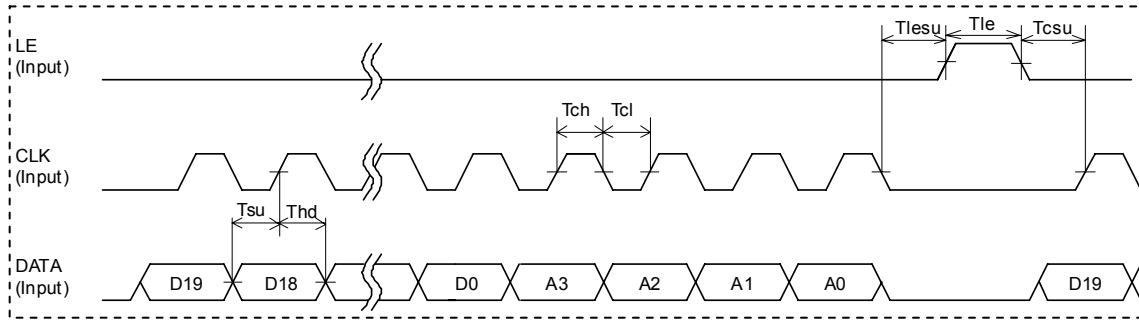


Fig. 3 Serial Interface Timing

Table 5 Serial Interface Timing

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
Clock L level hold time	Tchl	40			ns	
Clock H level hold time	Tch	40			ns	
Clock setup time	Tcsu	20			ns	
Data setup time	Tsu	20			ns	
Data hold time	Thd	20			ns	
LE Setup Time	Tlesu	20			ns	
LE Pulse Width	Tle	40			ns	

Note 1) LE pin has to set “Low” after register data setting completed. If LE pin keeps “High” with CLK operation, the register may not be guaranteed proper setting.

Note 2) While LE pin is setting “Low”, 24 iteration clocks have to be set with CLK pin. If 25 or larger clocks are set, the last 24 clocks synchronized data are valid.

3. Analog Circuit Characteristics

The resistance of 27kΩ is connected to the [BIAS] pin, VDD1=2.7 to 5.5V, VDD2=VDD1 to 5.5V, $-40^{\circ}\text{C} \leq T_a \leq 85^{\circ}\text{C}$

Parameter	Min.	Typ.	Max.	Unit	Remarks
RF Characteristics					
Input Sensitivity	-15		+5	dBm	Input frequency $\geq 100\text{MHz}$
	-5		+5		$20\text{MHz} \leq \text{Input frequency} < 100\text{MHz}$
Input Frequency	20		600	MHz	
REFIN Characteristics					
Input Sensitivity	0.4		2	Vpp	
Input Frequency	5		40	MHz	
Maximum Allowable Prescaler Output Frequency			75	MHz	
Phase Detector					
Phase Detector Frequency			3	MHz	
Charge Pump					
Charge Pump Maximum Value		6784		μA	
Charge Pump Minimum Value		106		μA	
Icp TRI-STATE Leak Current		1		nA	$0.5 \leq V_{cpo} \leq VDD2-0.5$
Mismatch between Source and Sink Currents (Note 1)			10	%	$V_{cpo} = VDD2/2$, $T_a = 25^{\circ}\text{C}$
Icp vs. Vcpo (Note 2)			15	%	$0.5 \leq V_{cpo} \leq VDD2-0.5$, $T_a = 25^{\circ}\text{C}$
Others					
VREF Rise Time			50	μs	
Consumption Current					
IDD1			10	μA	[PDN1]="Low", [PDN2]="Low"
IDD2		3.4	5	mA	Note 3)
IDD3		4.7		mA	Note 4)

Note 1) Mismatch between Source and Sink Currents: $\frac{(|I_{\text{sink}}| - |I_{\text{source}}|)}{(|I_{\text{sink}}| + |I_{\text{source}}|)/2} \times 100$ [%]

Note 2) See "Fig. 4 Charge Pump Characteristics - Voltage vs. Current": Icp vs. Vcpo:

$$\frac{\{1/2 \times (|I1| - |I2|)\}}{\{1/2 \times (|I1| + |I2|)\}} \times 100$$
 [%]

Note 3) [PDN1]="High", [PDN2]="High" IDD for [PVDD]

Note 4) [PDN1]="High", [PDN2]="High" IDD for [CPVDD]

IDD does not include the operation current in fast lockup mode.

Note 5) [PDN1]="High", [PDN2]="High", the total current consumption = IDD2 + IDD3 + charge pump setting

Note 6) In the shipment test, the exposed pad on the center of the back of the package is connected to ground.

Resistance Connected to the BIAS Pin for Setting Charge Pump Output Current

Parameter	Min.	Typ.	Max.	Unit	Remarks
BIAS resistance	22	27	33	kΩ	

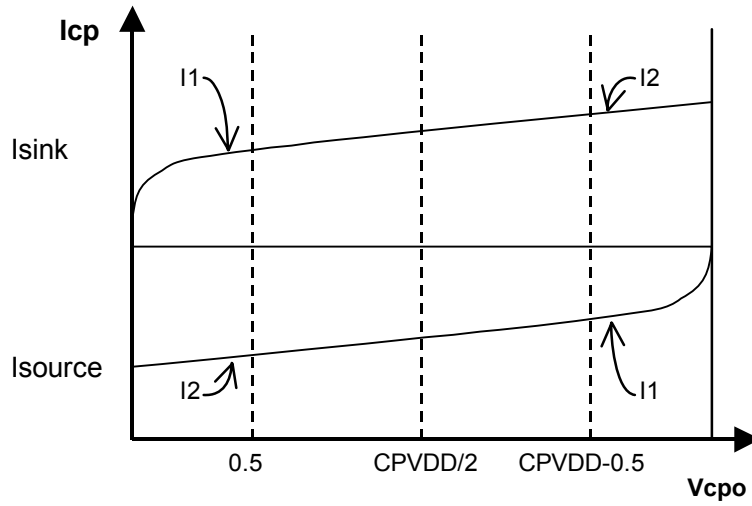


Fig. 4 Charge Pump Characteristics - Voltage (V_{cpo}) vs. Current (I_{cp})

8. Block Functional Descriptions

1. Frequency Setup

The following formula is used to calculate the frequency setting for the AK1542.

Frequency setting (external VCO output frequency) = $F_{PFD} \times N$

N	: Dividing number $N = [(P \times B) + A]$
F_{PFD}	: Phase detector frequency $F_{PFD} = [\text{REFIN}]$ pin input frequency / R counter dividing number
P	: Prescaler Value (See <Address2>:{Pre[1:0]})
B	: B (Programmable) counter value (See <Address1>:{B[12:0]})
A	: A (Swallow) counter value (See <Address1>:{A[5:0]})

○ Calculation examples

When the [REFIN] pin input frequency is 10MHz, the phase detector frequency $F_{PFD} = 5\text{kHz}$ and the frequency setting = 460.1MHz;

[The AK1542 Settings]

$R=10000000/5000 = 2000$ (<Address3> : {R[13:0]}=2000dec)

$P=32$ (<Address2>:{Pre[1:0]} =10bin)

$B=2875$ (<Address1>:{B[12:0]} =2875dec)

$A=20$ (<Address1>:{A[5:0]} =20dec)

Frequency setting = $5000 \times [(32 \times 2875) + 20] = 460.1\text{MHz}$

○ About division conditions

The conditions for division settings for A and B counters are as follows:

$A \geq 2$ A counter (6 bits): A decimal number from 2 to 63 can be set.

$B \geq 3$ B counter (13 bits): A decimal number from 3 to 8191 can be set.

$B > A$

A dividing number N cannot be consecutively set below the lower limits, which are shown as follows:

When $P=8$, $N+1$ for $A=8$ and $B=9$, namely, a division number which is equivalent to or smaller than $[(8 \times 9) + 8] + 1 = 81$ cannot be consecutively set.

When $P=16$, $N+1$ for $A=16$ and $B=17$, namely, a division number which is equivalent to or smaller than $[(16 \times 17) + 16] + 1 = 289$ cannot be consecutively be set.

When $P=32$, $N+1$ for $A=32$ and $B=33$, namely, a division number which is equivalent to or smaller than $[(32 \times 33) + 32] + 1 = 1089$ cannot be consecutively set.

When P = 8 (Namely, dividing ratio is 8/9)

P	B[12:0]	A[5:0]	Dividing number N = [(P x B) + A]	Remarks
8	3	2	26	
.	.	.	.	
8	8	7	71	
8	9	2	74	
8	9	3	75	
.	.	.	.	
8	9	8	80	
8	10	2	82	A number equivalent to or smaller than 81 cannot be consecutively set.
8	10	3	83	
.	.	.	.	
8	100	9	809	
.	.	.	.	
8	8191	62	65590	
8	8191	63	65591	

When P = 16 (Namely, dividing ratio is 16/17)

P	B[12:0]	A[5:0]	Dividing number N = [(P x B) + A]	Remarks
16	3	2	50	
.	.	.	.	
16	16	15	271	
16	17	2	274	
16	17	3	275	
.	.	.	.	
16	17	16	288	
16	18	2	290	A number which is equivalent to or smaller than 289 cannot be consecutively set.
16	18	3	291	
.	.	.	.	
16	4099	7	65591	
.	.	.	.	
16	8191	62	131118	
16	8191	63	131119	

When P = 32 (Namely, dividing ratio is 32/33)

P	B[12:0]	A[5:0]	Dividing number N = [(P x B) + A]	Remarks
32	3	2	98	
.	.	.	.	
32	32	31	1055	
32	33	2	1058	
32	33	3	1059	
.	.	.	.	
32	33	32	1088	
32	34	2	1090	A number which is equivalent to or smaller than 10898 cannot be consecutively set.
32	34	3	1091	
.	.	.	.	
32	4097	15	131119	
.	.	.	.	
32	8191	62	262174	
32	8191	63	262175	

2. Charge Pump and Loop Filter

In the AK1542, the fast lockup could be achieved by changing a charge pump current and enabling the loop filter. This is called Fast Lockup mode. For details, see "3. Fast Lockup Mode" on page 14.

The loop filter is external and connected to [CP], [SWIN] and [CPZ] pins. The [CPZ] pin should be connected to the R2 and C2, which are intermediate nodes, even if the Fast Lockup is not used. Therefore, R2 must be connected to the [CP] pin, while C2 must be connected to the ground.

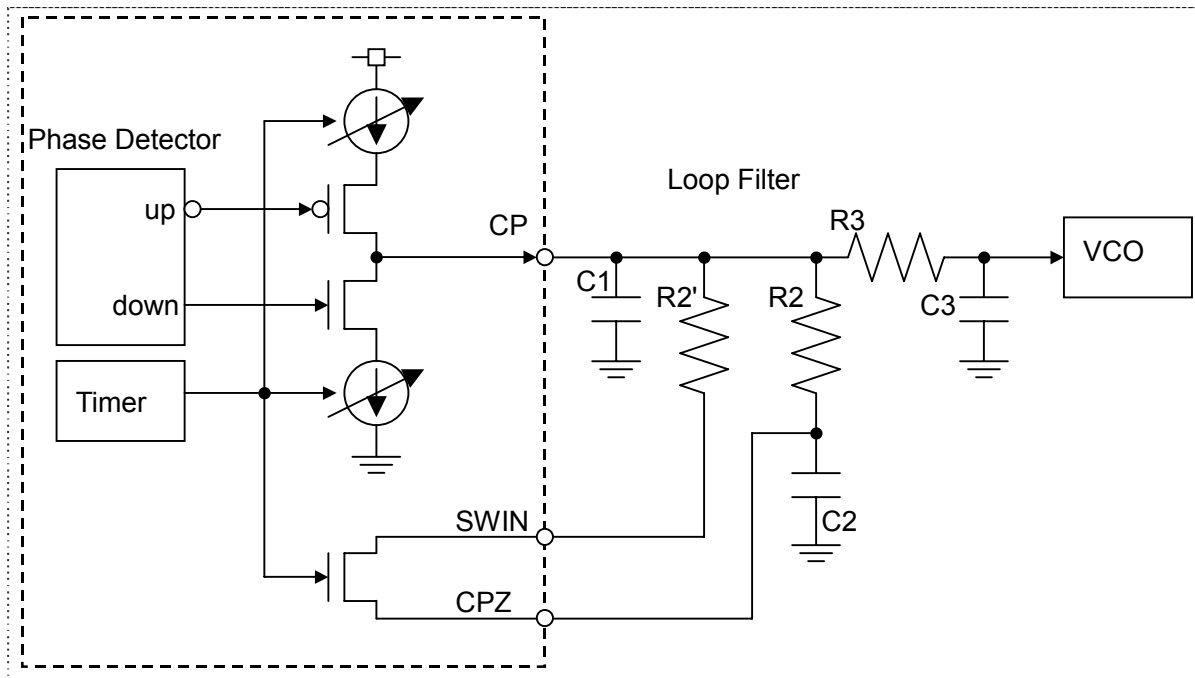


Fig. 5 Loop Filter Schematic

3. Fast Lockup Mode

Setting D[16]={FSTEN} in < Address4 > to 1 enables the Fast Lock Up mode for the AK1542.

Changing a frequency setting(The frequency is changed at the rising edge of [LE] when <Address1> and <Address2> are accessed.) or [PDN2] pin is set "Low" to "High" with {STEN}=1 enables the Fast Lockup mode. The loop filter switch turns ON during the timer period specified by the counter value in D[12:0] = {ST[12:0]} in < Address4 >, and the charge pump for the Fast Lockup mode (Charge Pump 2) set by D[11:6] = { CP2[5:0] } in < Address2 > is enabled.

After the timer period elapsed, the loop filter switch turns OFF, the charge pump for normal operation (Charge Pump 1) set by D[5:0] = { CP1[5:0] } in < Address2 > is enabled and thus normal operation returns.

The register D[12:0] = {FAST[12:0]} in < Address4 > is used to set the timer period for this mode. The following formula is used to calculate the time period:

$$\text{Phase detector frequency cycle} \times \text{counter value set in } \{ \text{FAST}[12:0] \}$$

The charge pump current could be adjust with 64 steps for both normal operation (Charge Pump 1) and the Fast Lockup operation (Charge Pump 2).

The absolute value of the charge pump current is determined by the Resistor value connected to the [BIAS] pin. The following formula shows the relationship between the resistance value, the register setting and the electric current value.

$$\text{Charge pump minimum current (Icp_min) [A]} = 2.862 / \text{Resistance connected to the [BIAS] pin ohm}$$

$$\text{Charge pump current [A]} = \text{Icp_min [A]} \times (\text{CP1 or CP2 setting} + 1)$$

The allowed range value for the resistance connected to the [BIAS] pin is from 22 to 33 [kΩ]. For details of current settings, see "Register Functional Description".

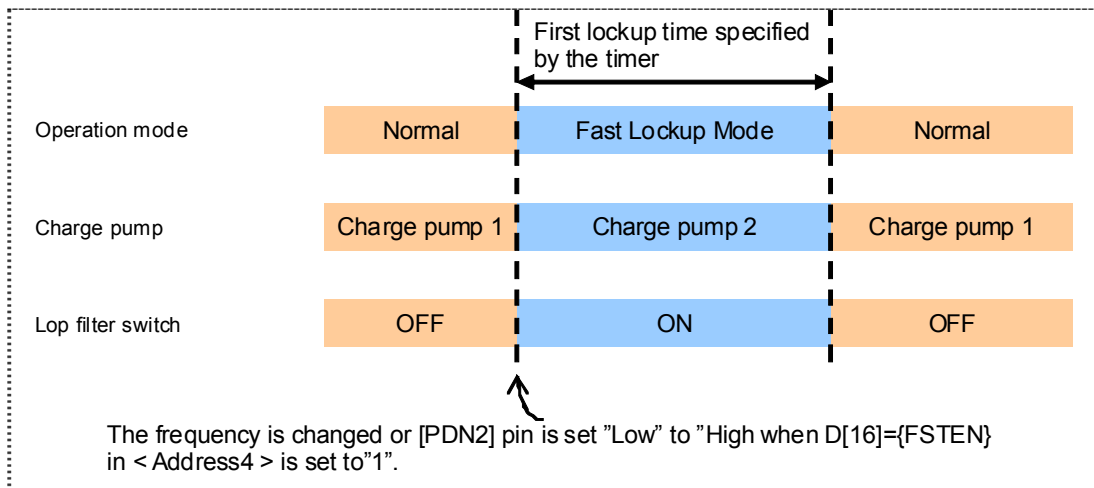


Fig. 6 Timing Chart for Fast Lockup Mode

4. Lock Detect (LD) Signal

In the AK1542, the lock detect output can be selected by $D[13] = \{LD\}$ in $\langle \text{Address4} \rangle$. When $D[13]$ is set to "1", the phase detector outputs provide a phase detection as an analog level (comparison result) . This is called analog lock detect. When $D[13]$ is set to "0", the lock detect signal is output according to the internal logic. This is called digital lock detect.

4.1 Analog Lock Detect

In analog lock detect, the phase detector output comes from the LD pin.

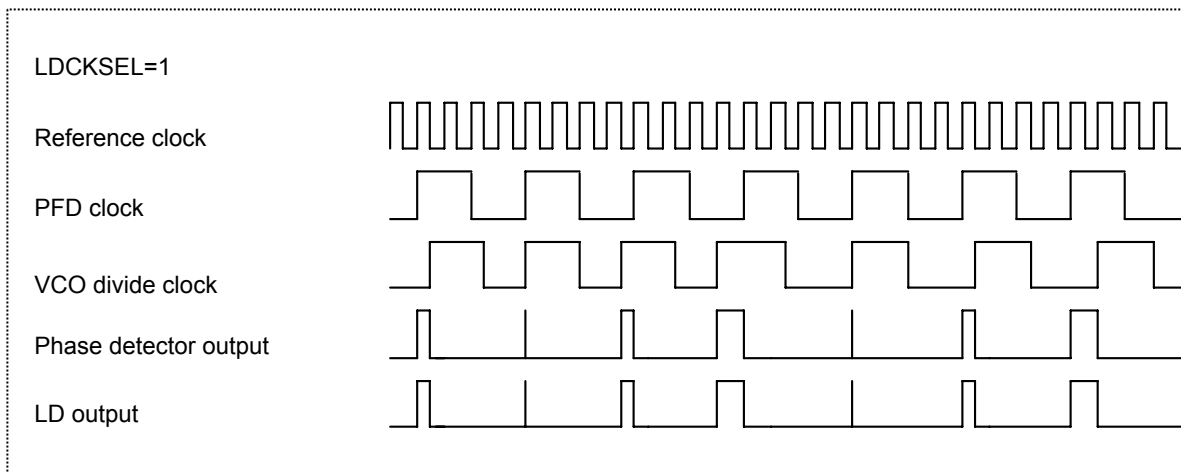


Fig. 7 Analog Lock Detect Operation

4.2 Digital Lock Detect

In the digital lock detect, the [LD] pin outputs is "Low" every time when the frequency is set. And the [LD] pin outputs is "High" (which means the locked state) when a phase error smaller than T is detected for N times consecutively. If the phase error is larger than T is detected for N times consecutively then the [LD] pin outputs is "High" and then the [LD] pin outputs is "Low"(which means the unlocked state).

The threshold counts for lock detection N could be set by D[18:17]={LDCNTSEL[1:0]} in < Address4 >.

{LDCNTSEL[1:0]} settings and corresponding counts (N) are as follows:

- 00: N = 7
- 01: N = 15
- 10: N = 31
- 11: N = 63

The lock detect signal is shown below:

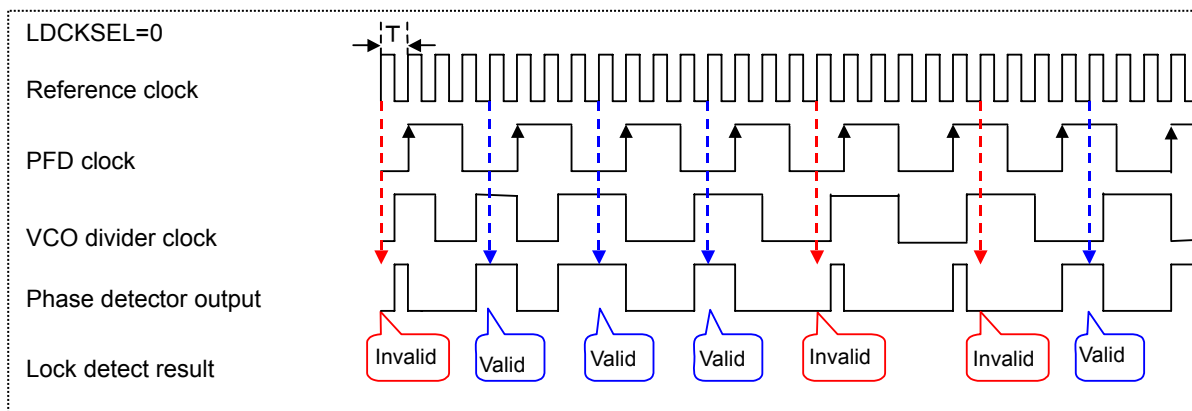


Fig. 8 Lock Detect Operations

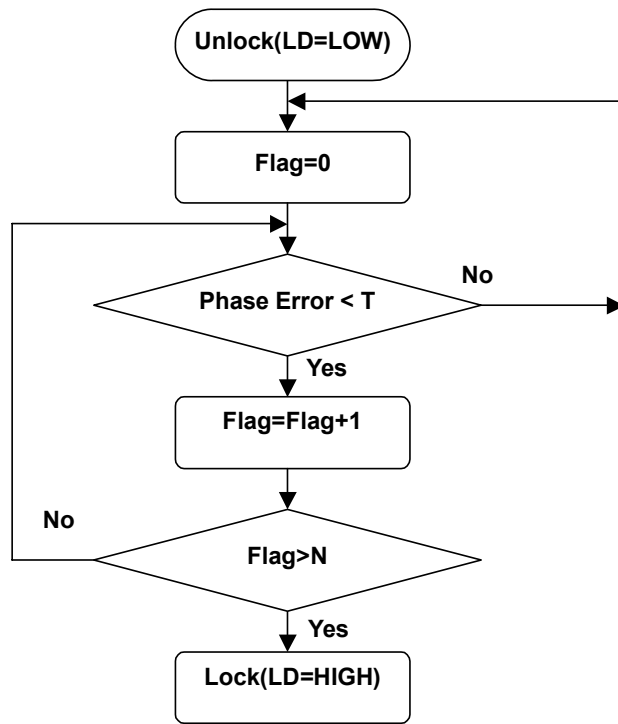


Fig. 9 Transition Flow Chart: Unlock State to Lock State

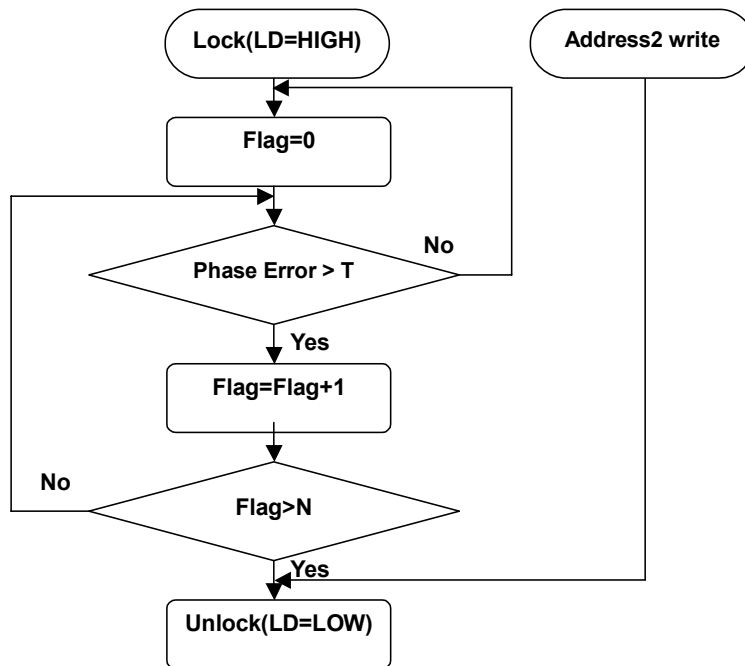


Fig. 10 Transition Flow Chart: Lock State to Unlock State

5. Reference Input

The reference input could be set to a dividing number in the range of 4 to 16383 using {R1[13:0]}, which is a 14-bit address of D[13:0] in < Address3 >. A dividing number from 0 to 3 could not be set.

6. Prescaler and Swallow Counter

The dual modular prescaler ($P/P + 1$) and the swallow counter are used to provide a large dividing ratio. The prescaler is set by {PRE[1:0]}, which is a 2-bit address of D[9:8] in < Address3 >.

{PRE[1:0]}="00": P=8, dividing ratio = 8/9

{PRE[1:0]}="01": P=16, dividing ratio = 16/17

{PRE[1:0]}="10": P=32, dividing ratio = 32/33

{PRE[1:0]}="11": Prohibited

7. Power Save Mode

The AK1542 can be operated in the power-down or power-save mode as necessary by using the external control pins [PDN1] and [PDN2].

- **Power On**

See "13. Power-up Sequence".

- **Normal Operation**

Pin name		State
PDN1	PDN2	
0	0	Power down
0	1	Prohibited
1	0	Power save Note 1) and Note 2)
1	1	Normal Operation

Note 1) Register setup can be made 50 μ s after [PDN1] is set to "High". The charge pump is in the Hi-Z state.

Note 2) Register settings are maintained when [PDN2] is set to "Low" during normal operation.

9. Register Map

Name	Data	Address			
A/B	D19~D0	0	0	0	1
CP		0	0	1	0
Ref/Pres		0	0	1	1
Function		0	1	0	0
GPO		0	1	0	1

	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Address
A/B	-	B [12]	B [11]	B [10]	B [9]	B [8]	B [7]	B [6]	B [5]	B [4]	B [3]	B [2]	B [1]	B [0]	A [5]	A [4]	A [3]	A [2]	A [1]	A [0]	0x01
CP	-	-	-	-	-	-	-	-	CP2 [5]	CP2 [4]	CP2 [3]	CP2 [2]	CP2 [1]	CP2 [0]	CP1 [5]	CP1 [4]	CP1 [3]	CP1 [2]	CP1 [1]	CP1 [0]	0x02
Ref/Pres	-	-	-	-	PRE [1]	PRE [0]	R [13]	R [12]	R [11]	R [10]	R [9]	R [8]	R [7]	R [6]	R [5]	R [4]	R [3]	R [2]	R [1]	R [0]	0x03
Function	-	LDCNT SEL[1]	LDCNT SEL[0]	FAST EN	CP HiZ	CP POLA	LD	FAST [12]	FAST [11]	FAST [10]	FAST [9]	FAST [8]	FAST [7]	FAST [6]	FAST [5]	FAST [4]	FAST [3]	FAST [2]	FAST [1]	FAST [0]	0x04
GPO	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	GPO 2	GPO 1	0x05

∴ Don't Care.

Note 1) The data in addresses 0x02 and 0x03 are committed to all related circuits when address 0x01 is written, which means that the data of these 3 addresses (0x01, 0x02 and 0x03) are committed to all related circuits at a time.

Note 2) The initial register values are not defined. Therefore, even after [PDN1] is set to "High", each bit value remains undefined. In order to set all register values, it is required to write the data in all addresses of the register.

- **Notes for writing into registers**

- (1) The data at addresses 0x02 and 0x03 are committed to all related circuits when address 0x01 is written, which means that the data of these 3 addresses (0x01, 0x02 and 0x03) are committed to all related circuits at the same time.
- (2) Addresses 0x04 and 0x05 could be written separately from other addresses.
- (3) The initial register values are not defined. Therefore, even after PDN1 is turned ON, each bit value remains undefined. In order to set all register values, it is required to write the data in all addresses of the register.

- **Examples of writing into registers**

(Ex. 1) Power-On ⇒Writing these three-word data is required.

- (1) Write a charge pump current value to address 0x02.
The data at address 0x02 is not committed to all related circuits at this time. Instead, it is stored in the on-chip buffer.
- (2) Write a division number for the prescaler and a reference counter value to address 0x03.
The data at the address 0x03 is not committed to all related circuits at this time. Instead, it is stored in the on-chip buffer.
- (3) Write values for A counter and B counter at the address 0x01.
The data of these 3 addresses (0x01, 0x02 and 0x03) are committed to all related circuits at this time.

(Ex. 2) Changing frequency settings

- (1) Write values for A counter and B counter at the address 0x01.
The data of these 3 addresses (0x01, 0x02 and 0x03) are committed to all related circuits at a time. The latest data written into addresses 0x02 and 0x03 are committed.

(Ex. 3) Changing charge pump current ⇒Writing these two-word data is required.

- (1) Write a charge pump current value at the address 0x02.
The data in address 0x02 is not committed to all related circuits at this time. Instead, it is stored in the on-chip buffer.
- (2) Write values for A counter and B counter at the address 0x01.
The data of these 3 addresses (0x01, 0x02 and 0x03) are committed to all related circuits at a time. The latest data written into address 0x03 is committed.

(Ex. 4) Changing reference dividing number ⇒Writing these two-word data is required.

- (1) Write a division number for the prescaler and a reference counter value at the address 0x03.
The data at the address 0x03 is not committed to all related circuits at this time. Instead, it is stored in the on-chip buffer.
- (2) Write values for A counter and B counter at the address 0x01.
The data of these 3 addresses (0x01, 0x02 and 0x03) are committed to all related circuits at a time. The latest data written into address 0x03 is committed.

10. Register Function Description
--

< Address1 :A/B >

D19	D[18:6]	D[5:0]	Address
-	B[12:0]	A[5:0]	0001

A[5:0]: A (Swallow) counter value

D5	D4	D3	D2	D1	D0	Function	Remarks
0	0	0	0	0	0	0	Prohibited
0	0	0	0	0	1	1 Dec	Prohibited
0	0	0	0	1	0	2 Dec	
0	0	0	0	1	1	3 Dec	
DATA							
1	1	1	1	0	1	61 Dec	
1	1	1	1	1	0	62 Dec	
1	1	1	1	1	1	63 Dec	

B[12:0]: B (Programmable) counter value

D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Function	Remarks
0	0	0	0	0	0	0	0	0	0	0	0	0	0	Prohibited
0	0	0	0	0	0	0	0	0	0	0	0	1	1 Dec	Prohibited
0	0	0	0	0	0	0	0	0	0	0	1	0	2 Dec	Prohibited
0	0	0	0	0	0	0	0	0	0	0	1	1	3 Dec	
DATA														
1	1	1	1	1	1	1	1	1	1	1	0	1	8189 Dec	
1	1	1	1	1	1	1	1	1	1	1	1	0	8190 Dec	
1	1	1	1	1	1	1	1	1	1	1	1	1	8191 Dec	

*** Requirements for A[5:0] and B[12:0]**

The data at A[5:0] and B[12:0] must meet the following requirements:

$$A[5:0] \geq 2, B[12:0] \geq 3, B[12:0] > A[5:0]$$

See "1. Frequency Setup" on Page 12 for details of the relationship between a frequency division number and the data at A[5:0] and B[12:0].

< Address2 :CP >

D19	D18	D17	D16	D15	D14	D13	D12	D[11:6]	D[5:0]	Address
-	-	-	-	-	-	-	-	CP2[5:0]	CP1[5:0]	0010

CP1[5:0] : Charge pump current for normal operation

CP2[5:0] : Charge pump current for the Fast Lockup mode

In the AK1542, two types of charge pump current CP1 and CP2 could be set.

CP1 is the charge pump current setting for normal operation.

CP2 is the charge pump current setting for the Fast Lockup mode.

The following formula shows the relationship between the resistance value, the register setting and the electric current value.

Charge pump minimum current (Icp_min) [A] = 2.862 / Resistance connected to the [BIAS] pin ohm]

Charge pump current [A] = Icp_min [A] x (CP1 or CP2 + 1)

CP1[5:0] CP2[5:0]	Charge pump currents [μ A]			CP1[5:0] CP2[5:0]	Charge pump currents [μ A]		
	22k Ω	27k Ω	33k Ω		22k Ω	27k Ω	33k Ω
000000	130	106	87	100000	4293	3498	2862
000001	260	212	173	100001	4423	3604	2949
000010	390	318	260	100010	4553	3710	3035
000011	520	424	347	100011	4683	3816	3122
000100	650	530	434	100100	4813	3922	3209
000101	781	636	520	100101	4943	4028	3296
000110	911	742	607	100110	5074	4134	3382
000111	1041	848	694	100111	5204	4240	3469
001000	1171	954	781	101000	5334	4346	3556
001001	1301	1060	867	101001	5464	4452	3643
001010	1431	1166	954	101010	5594	4558	3729
001011	1561	1272	1041	101011	5724	4664	3816
001100	1691	1378	1127	101100	5854	4770	3903
001101	1821	1484	1214	101101	5984	4876	3989
001110	1951	1590	1301	101110	6114	4982	4076
001111	2081	1696	1388	101111	6244	5088	4163
010000	2212	1802	1474	110000	6374	5194	4250
010001	2342	1908	1561	110001	6505	5300	4336
010010	2472	2014	1648	110010	6635	5406	4423
010011	2602	2120	1735	110011	6765	5512	4510
010100	2732	2226	1821	110100	6895	5618	4597
010101	2862	2332	1908	110101	7025	5724	4683
010110	2992	2438	1995	110110	7155	5830	4770
010111	3122	2544	2081	110111	7285	5936	4857
011000	3252	2650	2168	111000	7415	6042	4943
011001	3382	2756	2255	111001	7545	6148	5030
011010	3512	2862	2342	111010	7675	6254	5117
011011	3643	2968	2428	111011	7805	6360	5204
011100	3773	3074	2515	111100	7936	6466	5290
011101	3903	3180	2602	111101	8066	6572	5377
011110	4033	3286	2689	111110	8196	6678	5464
011111	4163	3392	2775	111111	8326	6784	5551

< Address3 :Ref/Pres >

D19	D18	D17	D16	D[15:14]	D[13:0]	Address
-	-	-	-	PRE[1:0]	R[13:0]	0011

PRE[1:0] : Prescaler division ratio (8/9, 16/17, 32/33)

The following settings can be chosen for the prescaler division.

D15	D14	Function	Remarks
0	0	8/9 (P=8)	
0	1	16/17 (P=16)	
1	0	32/33 (P=32)	
1	1	Prohibited	

R[13:0]: Reference clock division number

The following settings can be chosen for the reference clock division.

The allowed range is 4 (1/4 division) to 16383 (1/16383 division).

0 to 3 cannot be set.

D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Function	Remarks
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Prohibited
0	0	0	0	0	0	0	0	0	0	0	0	0	1	1/1 division	Prohibited
0	0	0	0	0	0	0	0	0	0	0	0	1	0	1/2 division	Prohibited
0	0	0	0	0	0	0	0	0	0	0	0	1	1	1/3 division	Prohibited
0	0	0	0	0	0	0	0	0	0	0	1	0	0	1/4 division	
DATA															
1	1	1	1	1	1	1	1	1	1	1	1	0	1	1/16381 division	
1	1	1	1	1	1	1	1	1	1	1	1	1	0	1/16382 division	
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1/16383 division	

< Address4 :Function>

D19	D18	D17	D16	D15	D14	D13	D[12:0]	Address
-	LDCNT SEL[1]	LDCNT SEL[0]	FAST EN	CP HiZ	CP POLA	LD	FAST[12:0]	0100

LDCNTSEL[1:0] : Counter value for lock detect

The counter value for digital lock detect can be set.

D18	D17	Function	Remarks
0	0	Counter value = 7	
0	1	Counter value = 15	
1	0	Counter value = 31	
1	1	Counter value = 63	

FASTEN : The Fast Lockup mode enable/disable setting

The Fast Lockup mode can be enabled or disabled.

D16	Function	Remarks
0	The data in CP2[2:0] and FAST[12:0] are disabled.	
1	The data in CP2[2:0] and FAST[12:0] are enabled.	

CPHiZ: TRI-STATE output setting for charge pumps 1 and 2

D15	Function	Remarks
0	Charge pumps are activated.	Use this setting for normal operation.
1	TRI-STATE	Note 1)

Note 1) The charge pump output is turned OFF and put in the high-impedance (Hi-Z) state.

CPPOLA: Selects positive or negative output polarity for CP1 and CP2.

D14	Function	Remarks
0	Positive	
1	Negative	

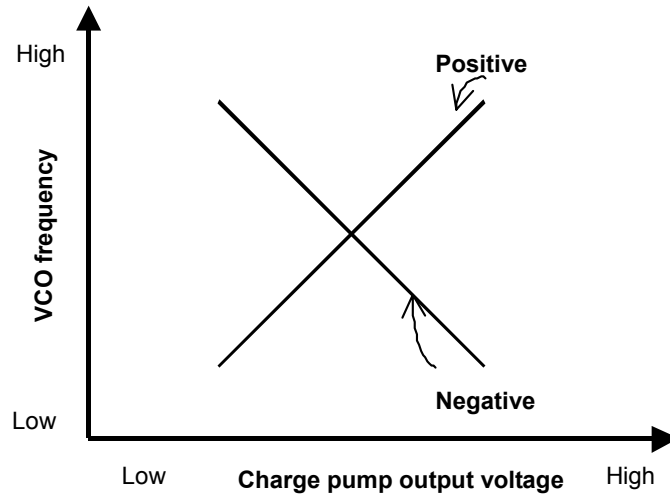


Fig. 11 Charge Pump Output Polarity

LD: Selects analog or digital for Lock Detect.

D13	Function	Remarks
0	Digital lock detect mode	
1	Analog lock detect mode	

For detailed functional descriptions, see the section “Lock Detect (LD) Signal” in “8. Block Functional Description”.

FAST[12:0] : FAST counter value

A decimal number from 1 to 8191 can be set. This value determines the time period during which the CP2 is ON for the Fast Lockup mode.

After the time period calculated by [phase detector frequency cycle x {FAST[12:0]} setting], the CP2 is turned OFF.

0 could not be set.

D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Function	Remarks
0	0	0	0	0	0	0	0	0	0	0	0	0	0	Prohibited
0	0	0	0	0	0	0	0	0	0	0	0	1	1 Dec	
0	0	0	0	0	0	0	0	0	0	0	1	0	2 Dec	
DATA														
1	1	1	1	1	1	1	1	1	1	1	0	1	8189 Dec	
1	1	1	1	1	1	1	1	1	1	1	1	0	8190 Dec	
1	1	1	1	1	1	1	1	1	1	1	1	1	8191 Dec	

< Address5 :GPO>

D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Address
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	GPO2	GPO1	0101

GPO2: The state of the GPO2 pin

This value controls the General-Purpose output pin GPO2.

The voltage applied to the PVDD pin determines the "High" level output.

D1	Function	Remarks
0	"LOW" output from the GPO2 pin	
1	"High" output from the GPO2 pin	

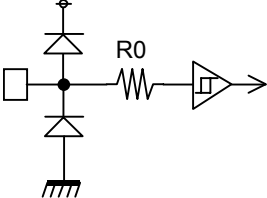
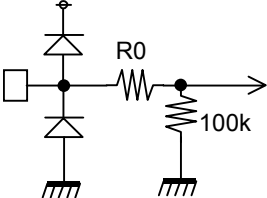
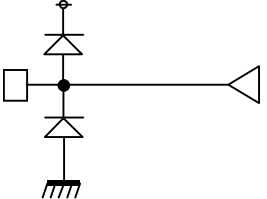
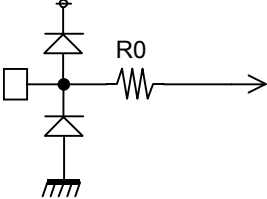
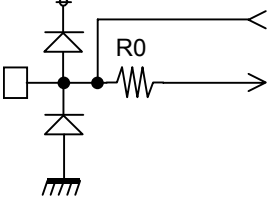
GPO1: The state of the GPO1 pin

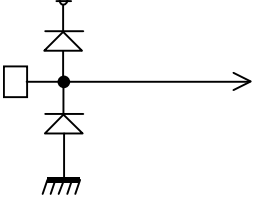
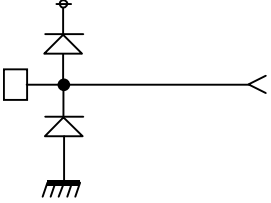
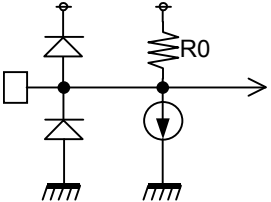
This value controls the General-Purpose output pin GPO1.

The voltage applied to the PVDD pin determines the "High" level output.

D0	Function	Remarks
0	"LOW" output from the GPO1 pin	
1	"High" output from the GPO1 pin	

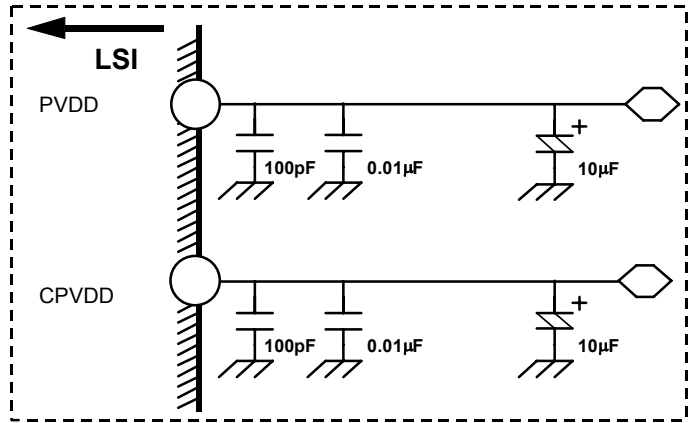
11. IC Interface Schematic

No.	Name	I/O	R0(Ω)	Cur(μA)	Function
4	LE	I	300		Digital input pins 
5	DATA	I	300		
6	CLK	I	300		
8	PDN2	I	300		
9	PDN1	I	300		
2	TEST3	I	300		Digital input pins Pull-Down 
3	TEST1	I	300		
11	TEST2	I	300		
7	LD	O			Digital output pin 
12	GPO1	O			
13	GPO2	O			
10	REFIN	I	300		Analog input pin 
15	VREF	IO	300		Analog I/O pin 
19	BIAS	IO	300		
22	CPZ	IO	300		

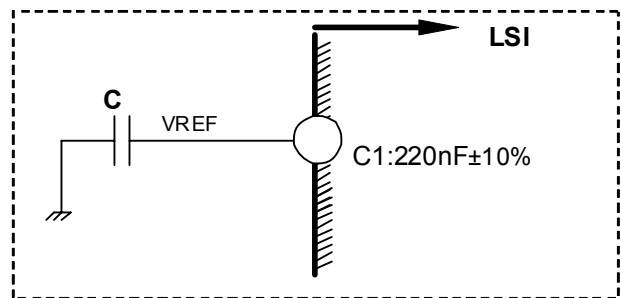
No.	Name	I/O	R0(Ω)	Cur(μA)	Function
23	SWIN	I			<p>Analog input pin</p> 
21	CP	O			<p>Analog output pin</p> 
16	RFINN	I	12k	20μA	<p>Analog input pin(RF signal input)</p> 
17	RFINP	I	12k	20μA	

12. Recommended Schematic for Off-Chip Component

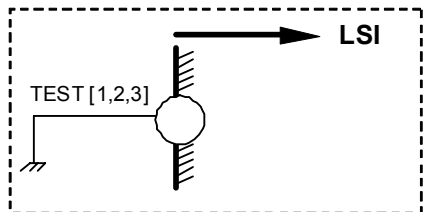
1. PVDD, CPVDD



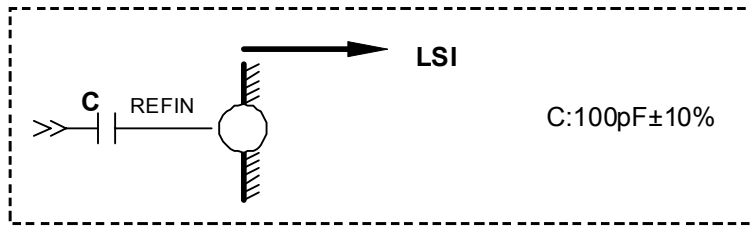
2. VREF



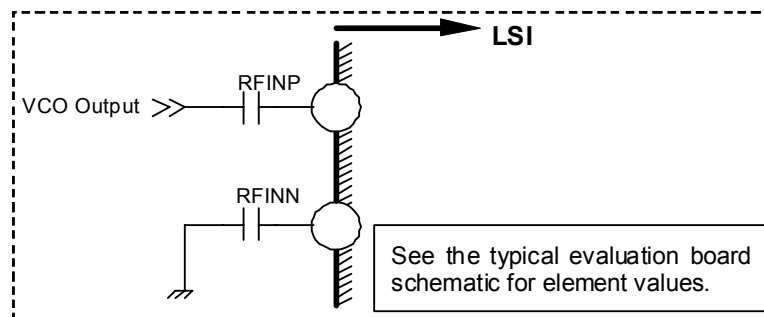
3. TEST [1,2,3]



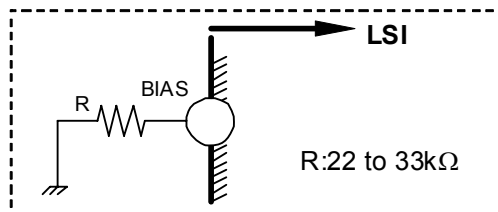
4. REFIN



5. RFINP, RFINN



6. BIAS



13. Power-up Sequence

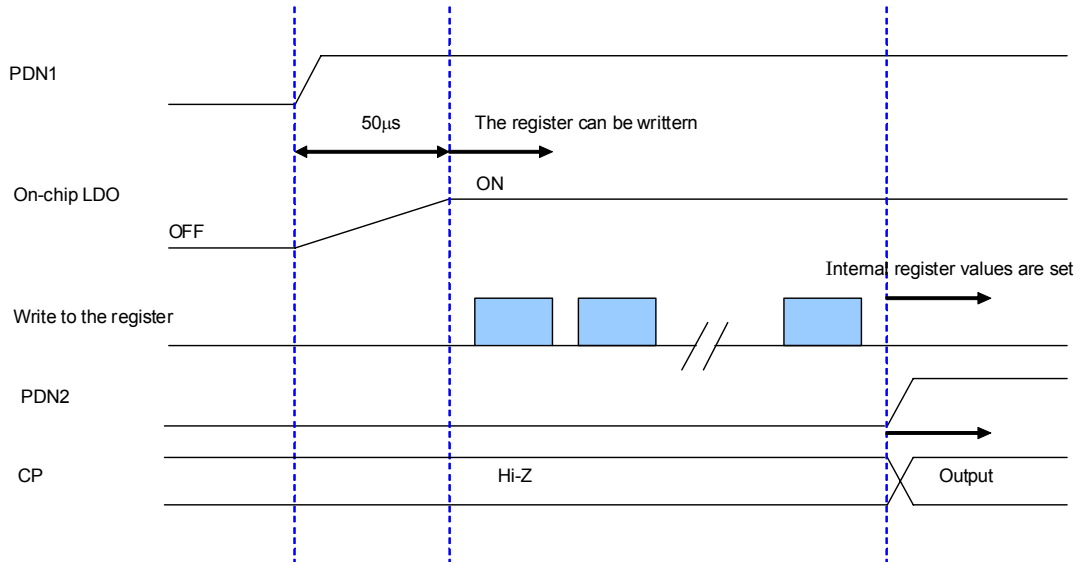


Fig. 12 Recommended Power Sequence

Note 1) The initial register values are not defined. Therefore, even after [PDN1] is set to "High", each bit value remains undefined. In order to set all register values, it is required to write the data in all addresses of the register.

14. Typical Evaluation Board Schematic

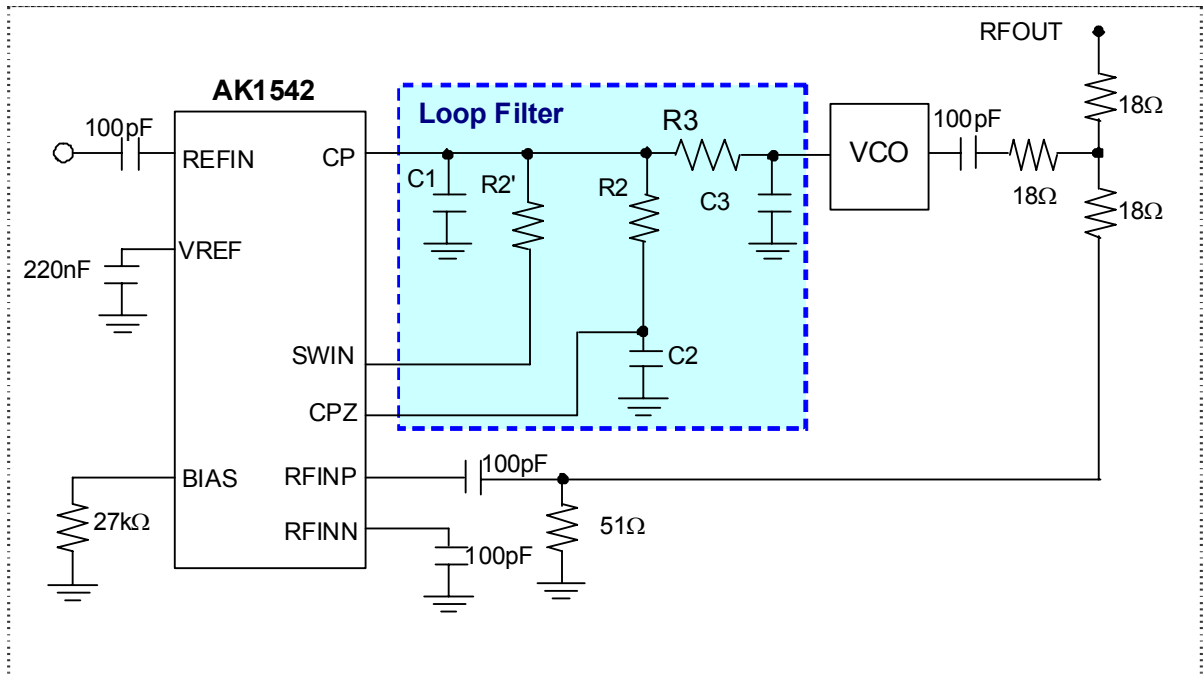


Fig. 13 Typical Evaluation Board Schematic

The input voltage from the [CPZ] pin is used in the internal circuit. The [CPZ] pin must not be open even when the fast lockup feature is unused. For the output destination from the [CPZ] pin, see “P.14 Fig.5 Loop Filter Schematic”. The [SWIN] pin could be open even when the first lockup feature is not used.

15. Block Diagram by Power Supply

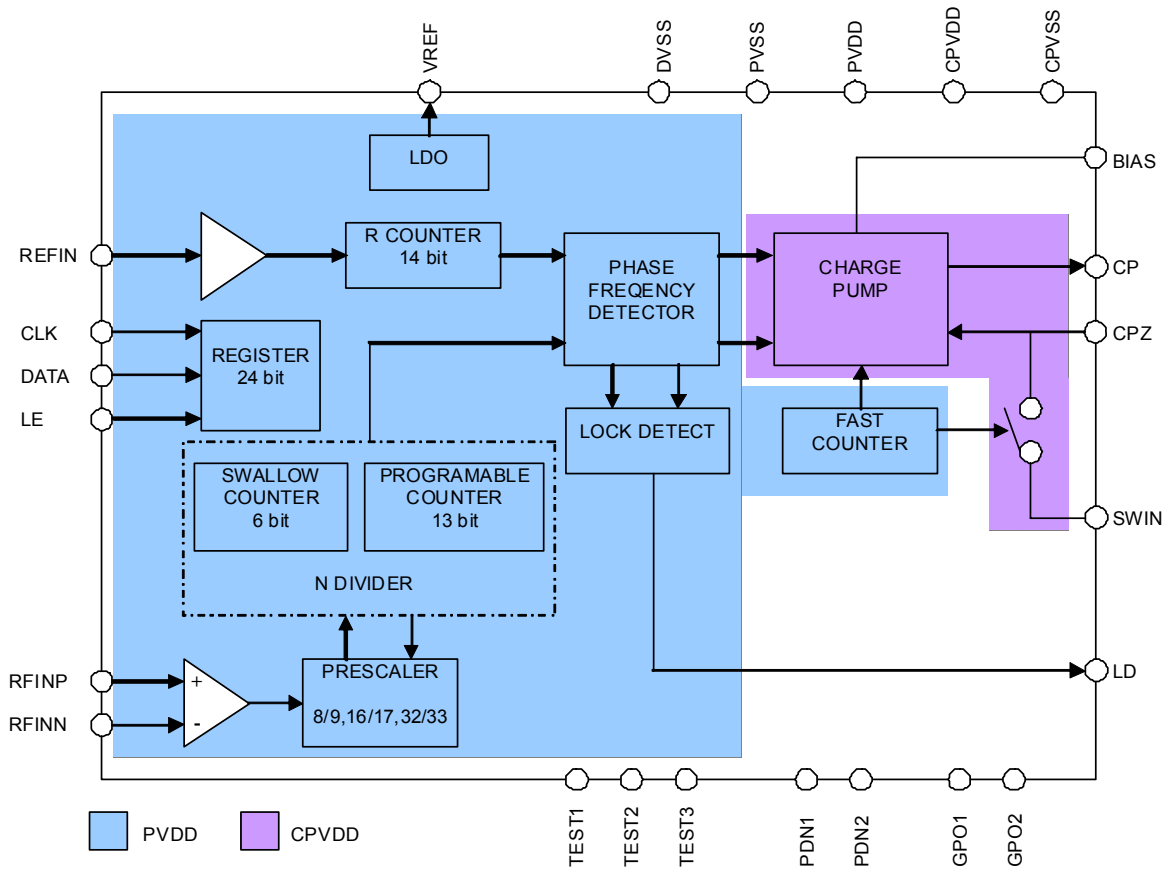


Fig. 14 Power Supply Block Diagram

16. Outer Dimensions

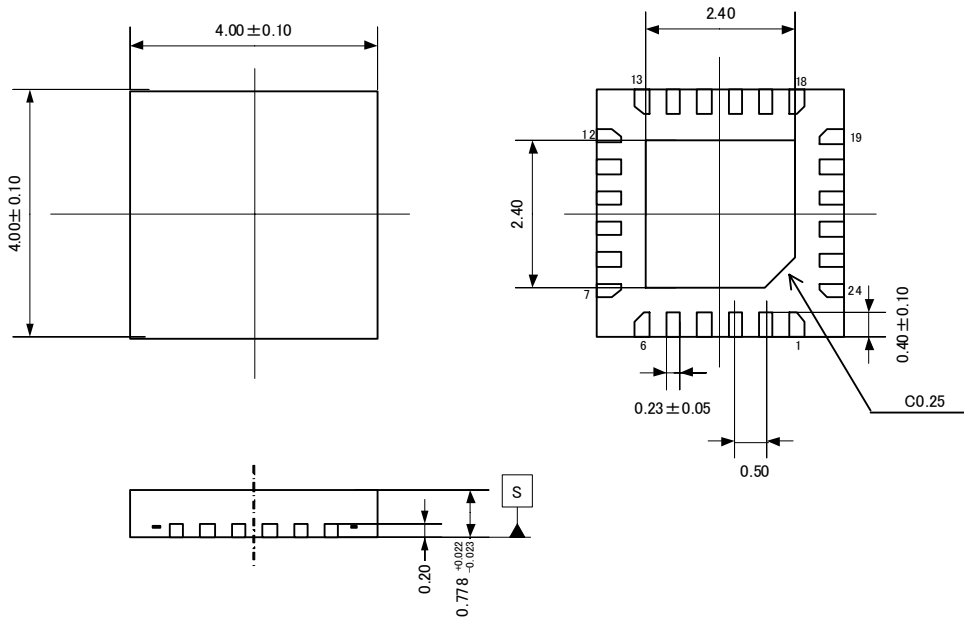
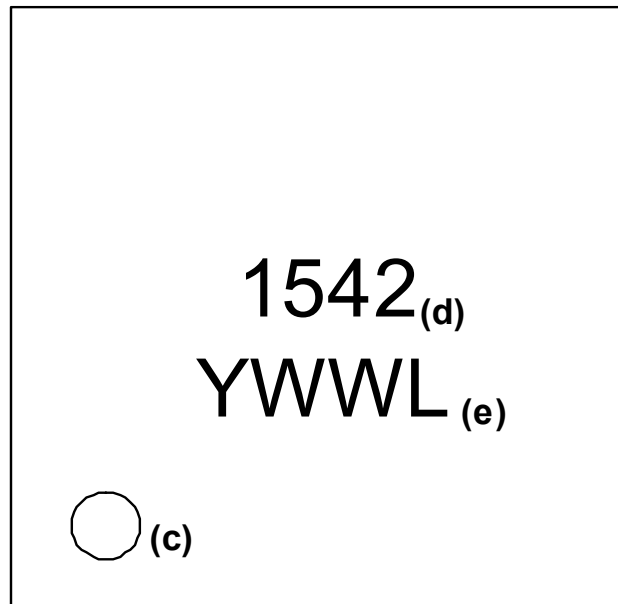


Fig. 15 Package Outer Dimensions

Note) It is recommended to connect the exposed pad on the center (at the back of the package) to the ground, although it will not make any impact on the electrical characteristics if the pad is open.

17. Marking

- (a) Style : QFN
(b) Number of pins : 24
(c) 1 pin marking: : ○
(d) Product number : 1542
(e) Date code : YWWL (4 digits)
- Y : Lower 1 digit of calendar year (Year 2009 → 9, 2010 → 0 ...)
WW : Week
L : Lot identification, given to each product lot which is made in a week
→ LOT ID is given in alphabetical order (A, B, C...).

**Fig. 16 Marking**

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