

**AsahiKASEI**  
ASAHI KASEI EMD

**AK4254**

**Capacitor-less Video Amp with 7:2 Video Switch**

**GENERAL DESCRIPTION**

The AK4254 is a 2ch Video AMP with 7:2 video switch, input clamp circuit, LPF and charge pump circuit. The integrated charge pump circuit can generate the negative power supply and remove the output coupling capacitor. The AK4254 suits Car Navigation system. The AK4254 is offered in a space saving 30pin VSOP package.

**FEATURES**

**1. Video Section**

- Composite Signal Inputs/Output
- Selector for 7 inputs and 2 outputs
- Video Driver for Composite Signal Output (+6dB)
- On-Chip Sync-tip Clamp Circuit
- 6MHz Low Pass Filter
- Charge pump circuit for negative power supply
- Parallel I/F or Serial  $\mu$ P I/F (I<sup>2</sup>C, 3-wires serial)

**2. Power Supply: 2.7V ~ 3.6V**

**3. Ta=-40 ~ +85°C**

**4. Package: 30pin VSOP**

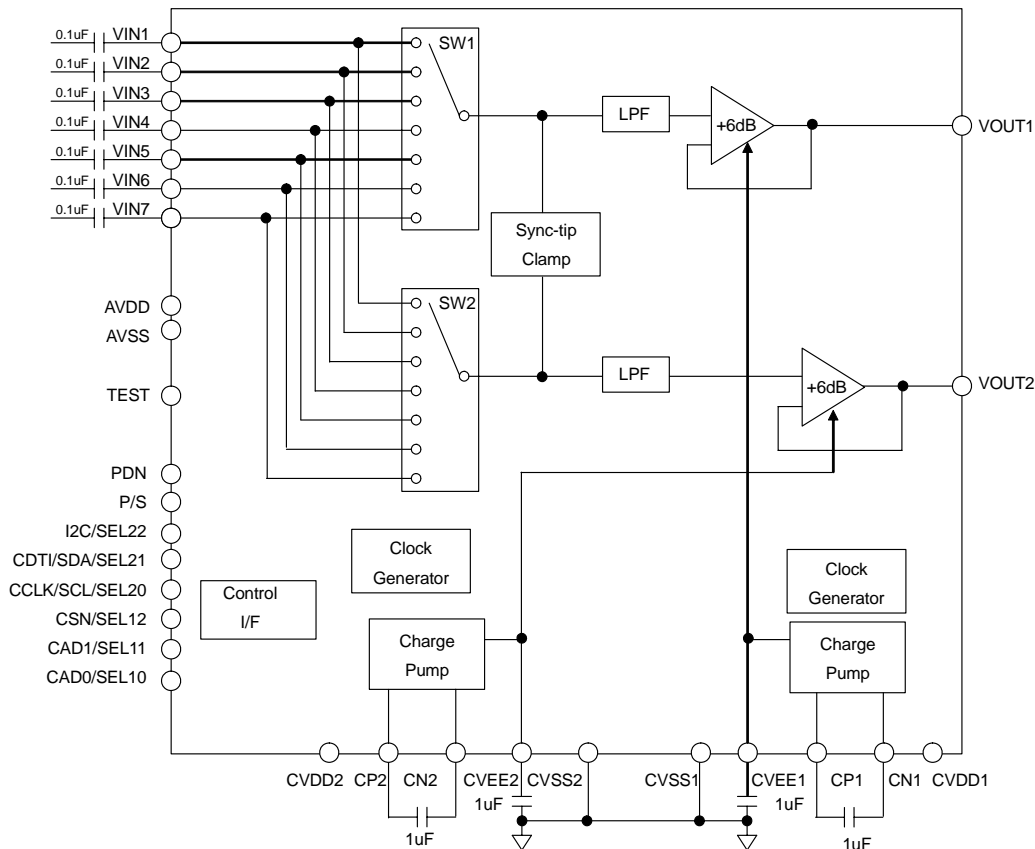


Figure 1. Block Diagram



## PIN/FUNCTION

No.	Pin Name	I/O	Function
1	CVDD1	-	Charge Pump Power Supply pin, 2.7V~3.6V
2	CP1	O	Positive Charge Pump Capacitor Terminal 1 Pin. Connect to CN1 with a 1.0 $\mu$ F capacitor that has the low ESR (Equivalent Series Resistance) over all temperature range. When this capacitor has the polarity, the positive polarity pin should be connected to the CP pin. Non polarity capacitors can also be used.
3	CN1	I	Negative Charge Pump Capacitor Terminal 1 Pin Connect to CP1 with a 1.0 $\mu$ F capacitor that has the low ESR (Equivalent Series Resistance) over all temperature range. When this capacitor has the polarity, the positive polarity pin should be connected to the CP pin. Non polarity capacitors can also be used.
4	CVSS1	-	Charge Pump Ground Pin, 0V Connect to VEE1 with a 1.0 $\mu$ F capacitor that has the low ESR (Equivalent Series Resistance) over all temperature range. When this capacitor has the polarity, the positive polarity pin should be connected to the CVSS1 pin. Non polarity capacitors can also be used.
5	CVEE1	O	Negative Voltage Output Pin for Video Amplifier 1 Connect to CVSS1 with a 1.0 $\mu$ F capacitor that has the low ESR (Equivalent Series Resistance) over all temperature range. When this capacitor has the polarity, the positive polarity pin should be connected to the CVSS1 pin. Non polarity capacitors can also be used.
6	VOUT1	O	Video Output #1 Pin
7	AVDD	-	Analog Power Supply Pin, 2.7V~3.6V
8	AVSS	-	Analog Ground Pin, 0V
9	TEST	I	Test Pin This pin should be connected to AVSS.
10	P/S	I	Parallel/Serial Control Mode Pin “L”: Serial Control Mode, “H”: Parallel Control Mode
11	VIN1	I	Video Input #1 Pin
12	VIN2	I	Video Input #2 Pin
13	VIN3	I	Video Input #3 Pin
14	VIN4	I	Video Input #4 Pin
15	VIN5	I	Video Input #5 Pin
16	VIN6	I	Video Input #6 Pin
17	VIN7	I	Video Input #7 Pin
18	CAD0	I	Chip Address 0 in Serial Control Mode
	SEL10	I	Input Selector 1 Control #0 Pin in Parallel Control Mode
19	CAD1	I	Chip Address 1 in Serial Control Mode
	SEL11	I	Input Selector 1 Control #1 Pin in Parallel Control Mode
20	CSN	I	Chip Select Pin in Serial Control Mode, I2C pin = “L” This pin should be connected to AVSS in Serial Control Mode. I2C pin = “H”
	SEL12	I	Input Selector 1 Control #2 Pin in Parallel Control Mode.
21	CCLK	I	Control Data Clock Pin in Serial Control Mode, I2C pin = “L”
	SCL	I	Control Data Clock Pin in Serial Control Mode, I2C pin = “H”
	SEL20	I	Input Selector 2 Control #0 Pin in Parallel Control Mode
22	CDTI	I	Control Data Input Pin in Serial Control Mode, I2C pin = “L”
	SDA	I/O	Control Data Pin in Serial Control Mode, I2C pin = “H”
	SEL21	I	Input Selector 2 Control #1 Pin in Parallel Control Mode.
23	I2C	I	Control Mode Select Pin in Serial Control Mode “L”: 3-wire Serial Mode, “H”: I <sup>2</sup> C Bus mode
	SEL22	I	Input Selector 2 Control #2 Pin in Parallel Control Mode

No.	Pin Name	I/O	Function
24	PDN	I	Power-Down Mode Pin When at “L”, the AK4254 is in the power-down mode and held in reset, the AK4254 must always be reset upon power-up in Serial Control Mode (P/S pin= “L”).
25	VOUT2	O	Video Output #2 Pin.
26	CVEE2	O	Negative Voltage Output Pin for Video Amplifier 2 Connect to CVSS2 with a 1.0μF capacitor that has the low ESR (Equivalent Series Resistance) over all temperature range. When this capacitor has the polarity, the positive polarity pin should be connected to the CVSS2 pin. Non-polarity capacitors can also be used.
27	CVSS2	-	Charge Pump Ground Pin, 0V Connect to CVEE2 with a 1.0μF capacitor that has the low ESR (Equivalent Series Resistance) over all temperature range. When this capacitor has the polarity, the positive polarity pin should be connected to the CVSS2 pin. Non-polarity capacitors can also be used.
28	CN2	I	Negative Charge Pump Capacitor Terminal 2 Pin Connect to CP2 with a 1.0μF capacitor that has the low ESR (Equivalent Series Resistance) over all temperature range. When this capacitor has the polarity, the positive polarity pin should be connected to the CP2 pin. Non polarity capacitors can also be used.
29	CP2	O	Positive Charge Pump Capacitor Terminal 2 Pin Connect to CN2 with a 1.0μF capacitor that has the low ESR (Equivalent Series Resistance) over all temperature range. When this capacitor has the polarity, the positive polarity pin should be connected to the CP2 pin. Non polarity capacitors can also be used.
30	CVDD2	-	Charge Pump Power Supply Pin, 2.7V~3.6V

Note: All digital input pins (CADO/SEL10, CADT/SEL11, CSN/SEL12, CCLK/SCL/SEL20, CDTI/SDA/SEL21, I2C/SEL22) must not be left floating.

### ■ Handling of Unused Pin

The unused I/O pins should be processed appropriately as below.

Classification	Pin Name	Setting
Analog	VIN1-7	These pins should be open.
Digital	CSN/SEL12	These pins should be connected to AVDD or AVSS.

**ABSOLUTE MAXIMUM RATINGS**

(AVSS=CVSS1=CVSS2=0V; Note: 1)

Parameter	Symbol	min	max	Units
Power Supply (Note: 2)	AVDD	-0.3	4.0	V
	CVDD1	-0.3	4.0	V
	CVDD2	-0.3	4.0	V
Input Current (any pins except for supplies)	IIN	-	±10	mA
Input Voltage (Note: 3) (VIN1-7, I2C/SEL22, CDTI/SDA/SEL21, CCLK/SCL/SEL20, CSN/SEL12, CAD1/SEL11, CAD0/SEL10, PDN, P/S pins)	VIN	-0.3	AVDD+0.3 or 4.0	V
Ambient Operating Temperature	Ta	-40	85	°C
Storage Temperature	Tstg	-65	150	°C

Note: 1. All voltages are with respect to ground.

Note: 2. AVSS, CVDD1 and CVDD2 must be connected to the same analog ground plane.

Note: 3. The external pull-up resistors at the SDA and SCL pins should be connected to the maximum voltage or less.

Max is smaller value between AVDD+0.3V and 4.0V.

The voltage must not be applied to the CN1 and CN2 pins.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.

Normal operation is not guaranteed at these extremes.

**RECOMMENDED OPERATING CONDITIONS**

(AVSS=CVSS1=CVSS2=0V; Note: 1)

Parameter	Symbol	Min	Typ	max	Units
Power Supply (Note: 4)	AVDD	2.7	3.0	3.6	V
	CVDD1, CVDD2		AVDD		V

Note: 4. AVDD, CVDD1 and CVDD2 must be the same voltage.

\*AKEMD assumes no responsibility for the usage beyond the conditions in this datasheet.

**DIGITAL CHARACTERISTICS**

(Ta = -40~85°C; AVDD=CVDD1=CVDD2=2.7V~3.6V)

Parameter	Symbol	min	typ	max	Units
High-Level Input Voltage	VIH	70%AVDD	-	-	V
Low-Level Input Voltage	VIL	-	-	30%AVDD	V
Low-Level Output Voltage (SDA pin: Iout= 3mA)	VOL	-	-	0.4	V
Input Leakage Current	Iin	-	-	± 10	μA

**ANALOG CHARACTERISTICS**

(Ta = 25°C; AVDD=CVDD1=CVDD2=3.0V; unless otherwise specified. Note: 5, Note: 6)

Parameter	Conditions	min	typ	max	Units
Gain	Input=0.3Vp-p, 100kHz	5.3	6	6.7	dB
Frequency Response Input=0.3Vpp, Sin Wave (0dB at 100kHz)	Response at 6MHz	-2.0		+2.0	dB
	Response at 27MHz		-40	-20	dB
Group Delay Distortion	GD3MHz - GD6MHz		10	100	ns
Dynamic Output Signal	f=100kHz, maximum with distortion < 1.0%.	2.52			Vpp
Inter channel Isolation	f=4.43MHz, 1Vp-p input	-	65	-	dB
S/N	Reference Level = 0.7Vp-p, BW= 100kHz to 6MHz.	-	65	-	dB
Differential Gain	0.7Vpp 5steps modulated staircase. Chrominance & burst are 280mVpp, 4.43MHz.	-	+0.4	-	%
Differential Phase	0.7Vpp 5steps modulated staircase. Chrominance & burst are 280mVpp, 4.43MHz.	-	+2.5	-	Degree
Load Resistance	R1+R2 (Note: 9)	140	150	-	Ω
Load Capacitance	C1 (Note: 9)			400	pF
	C2 (Note: 9)			15	pF
<b>Power Supply Current</b>					
Normal Operation (PDN pin = "H", Note: 7)	AVDD+CVDD1+CVDD2		20	30	mA
Power-Down Mode (PDN pin = "L", Note: 8)	AVDD+CVDD1+CVDD2		10	100	μA

Note: 5. Video analog characteristics are measured at the pin directly.

Note: 6. Input Sync Tip Level=-0.43V~-0.14V (It is the difference with Pedestal Level and Sync Tip Level.)

Horizontal Line Sync Pulse=4.0μs ~5.4μs, Equalizing Pulse=2.0μs ~2.7μs, Serration Pulse=4.0μs ~5.4μs

Note: 7. VIN Black level input, no load

Note: 8. All digital input pins (P/S, I2C/SEL22, CDTI/SDA/SEL21, CCLK/SCL/SEL20, SN/SEL12, CAD1/SEL11, CAD0/SEL10) are held at AVSS.

Note: 9. Refer to the Figure 2.

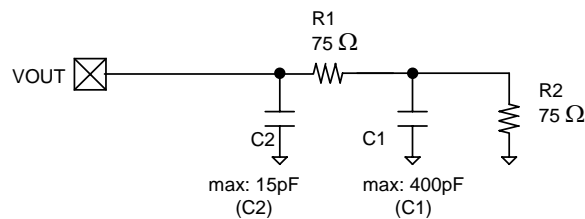


Figure 2. Load Resistance R1+R2 and Load Capacitance C1/C2

<b>SWITCHING CHARACTERISTICS</b>
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(Ta = -40~85°C; AVDD=CVDD1=CVDD2=2.7V~3.6V; CL = 20pF)

Parameter	Symbol	Min	typ	max	Units
<b>Control Interface Timing (3-wire Serial mode)</b>					
PDN “↑” to CSN “↓”	tPDCS	150			ns
CCLK Period	tCCK	200			ns
CCLK Pulse Width Low	tCCKL	80			ns
Pulse Width High	tCCKH	80			ns
CDTI Setup Time	tCDS	40			ns
CDTI Hold Time	tCDH	40			ns
CSN “H” Time	tCSW	150			ns
CSN “↓” to CCLK “↑”	tCSS	50			ns
CCLK “↑” to CSN “↑”	tCSH	50			ns
<b>Control Interface Timing (I<sup>2</sup>C Bus mode):</b>					
SCL Clock Frequency	fSCL	-		400	kHz
PDN “↑” to SDA “↓” @SCL = “H”	tPDS	1.3		-	μs
Bus Free Time Between Transmissions	tBUF	1.3		-	μs
Start Condition Hold Time (Prior to first clock pulse)	tHD:STA	0.6		-	μs
Clock Low Time	tLOW	1.3		-	μs
Clock High Time	tHIGH	0.6		-	μs
Setup Time for Repeated Start Condition	tSU:STA	0.6		-	μs
SDA Hold Time from SCL Falling (Note: 10)	tHD:DAT	0		-	μs
SDA Setup Time from SCL Rising	tSU:DAT	0.1		-	μs
Rise Time of Both SDA and SCL Lines	tR	-		0.3	μs
Fall Time of Both SDA and SCL Lines	tF	-		0.3	μs
Setup Time for Stop Condition	tSU:STO	0.6		-	μs
Pulse Width of Spike Noise Suppressed by Input Filter	tSP	0		50	ns
Capacitive load on bus	Cb	-		400	pF
<b>Reset Timing</b>					
PDN Pulse Width (Note: 11)	tPD	150			ns

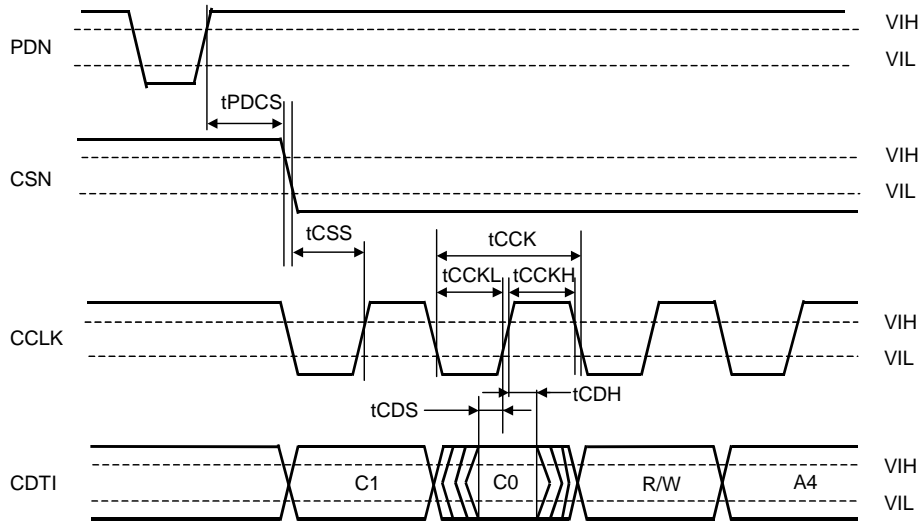
Note: 10. Data must be held for sufficient time to bridge the 300 ns transition time of SCL.

Note: 11. In Serial Control Mode (P/S pin= “L”), it is recommended that the AK4254 is powered up at the PDN pin=“L”.

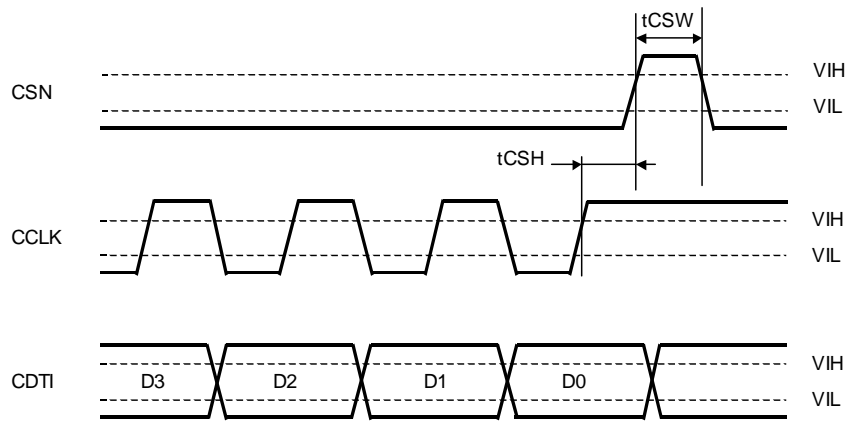
In Parallel Control Mode, resetting by the PDN pin = “L” is not needed when power up.

Note: 12. I<sup>2</sup>C is a registered trademark of Philips Semiconductors.

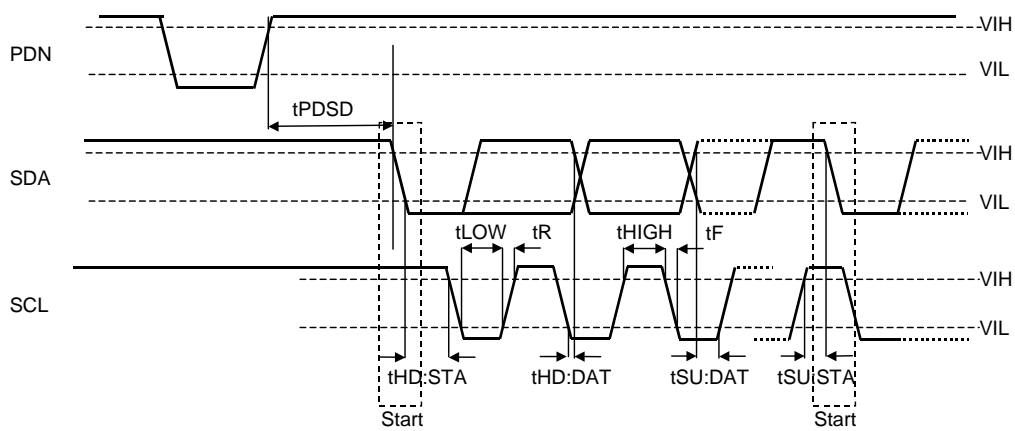
■ Timing Diagram



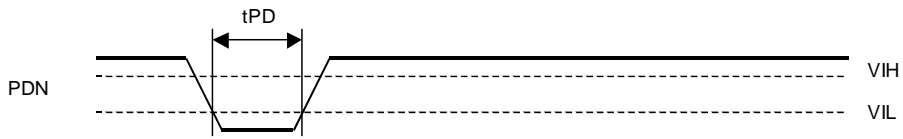
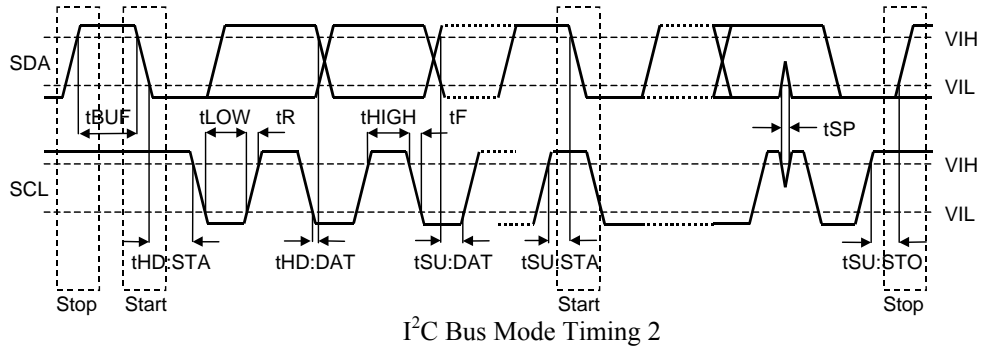
WRITE Command Input Timing (3-wire Serial mode)



WRITE Data Input Timing (3-wire Serial mode)



I<sup>2</sup>C Bus Mode Timing 1



Power down & Reset timing

**OPERATION OVERVIEW**

■ **System Reset**

In Serial Control Mode (P/S pin= “L”), it is recommended that AK4254 is powered up when the PDN pin= “L”. If the AK4254 is powered up when the PDN pin = “H”, the AK4254 should be reset by the PDN pin = “L” after power up. The control registers are initialized to their default values by resetting. In Parallel Control Mode, resetting by the PDN pin = “L” is not needed when power up.

■ **Parallel Control Mode (P/S pin = “H”)**

The AK4524 is in Parallel Control Mode at P/S pin = “H”. When the AK4524 is in Parallel Control Mode, all registers can not be accessed.

Mode	PDN pin	SEL12-10 pin	CVEE1 pin	VOUT1 pin
Power Down mode	L	x	GND	GND
Normal mode	H	“LLL”	GND	GND
	H	Except for “LLL”	-CVDD1	Video signal output

(x: Don’t Care)

Table 1. VOUT1 mode setting (Parallel Control Mode)

Mode	PDN pin	SEL22-20 pin	CVEE2 pin	VOUT2 pin
Power Down mode	L	x	GND	GND
Normal mode	H	“LLL”	GND	GND
	H	Except for “LLL”	-CVDD1	Video signal output

(x: Don’t Care)

Table 2. VOUT2 mode setting (Parallel Control Mode)

**(a) Power Down mode (PDN pin= “L”)**

The AK4524 is in Power Down mode at the PDN pin = “L”. When the AK4524 is in the Power Down mode, the VOUT1-2 outputs are “GND”.

**(b) Normal mode (PDN pin= “H”)**

The AK4524 have 7:2 video switches. In Parallel Control Mode, the each input of VOUT1-2 is set by SEL12-10 pins and SEL22-20 pins.

SEL12 pin	SEL11 pin	SEL10 pin	VOUT1 pin
L	L	L	Off Note: 13)
L	L	H	VIN1
L	H	L	VIN2
L	H	H	VIN3
H	L	L	VIN4
H	L	H	VIN5
H	H	L	VIN6
H	H	H	VIN7

Note: 13. When the input setting is “Off”, VOUT1 output is “GND”.

Table 3. Input Selector 1 (Parallel Control Mode)

SEL22 pin	SEL21 pin	SEL20 pin	VOUT2 pin
L	L	L	Off Note: 14)
L	L	H	VIN1
L	H	L	VIN2
L	H	H	VIN3
H	L	L	VIN4
H	L	H	VIN5
H	H	L	VIN6
H	H	H	VIN7

Note: 14. When the input setting is “Off”, VOUT2 output is “GND”.

Table 4. Input Selector 2 (Parallel Control Mode)

■ **Serial Control Mode (P/S pin = “L”)**

The AK4524 is in Serial Control Mode at P/S pin = “L”.

Mode	PDN pin	SEL 12-10 bit	CVEE1 pin	VOUT1 pin
Power Down mode	L	x	GND	GND
Normal mode	H	“000”	GND	GND
	H	Except for “000”	-CVDD1	Video signal output

(x: Don’t Care)

Table 5. VOUT1 mode setting (Serial Control Mode)

Mode	PDN pin	SEL 22-20 bit	CVEE2 pin	VOUT2 pin
Power Down mode	L	x	GND	GND
Normal mode	H	“000”	GND	GND
	H	Except for “000”	-CVDD1	Video signal output

(x: Don’t Care)

Table 6. VOUT2 mode setting (Serial Control Mode)

**(a) Power Down mode (PDN pin= “L”)**

When PDN pin = “L”, the register is reset and the AK4254 is in Power Down mode. When the AK4524 is in the Power Down mode, the VOUT1-2 outputs are “GND”.

**(b) Normal mode (PDN pin= “H”)**

The AK4524 have 7:2 video switches. In the Serial Control Mode, the each input of VOUT1-2 is set by SEL12-10 bits and SEL22-20 bits.

SEL12 bit	SEL11 bit	SEL10 bit	VOUT1 pin
0	0	0	Off Note: 15)
0	0	1	VIN1
0	1	0	VIN2
0	1	1	VIN3
1	0	0	VIN4
1	0	1	VIN5
1	1	0	VIN6
1	1	1	VIN7

(default)

Note: 15. When the input setting is “Off”, VOUT1 output is “GND”.

Table 7. Input Selector 1 (Serial Control Mode)

SEL22 bit	SEL21 bit	SEL20 bit	VOUT2 pin
0	0	0	Off Note: 16)
0	0	1	VIN1
0	1	0	VIN2
0	1	1	VIN3
1	0	0	VIN4
1	0	1	VIN5
1	1	0	VIN6
1	1	1	VIN7

Note: 16. When the input setting is "Off", VOUT2 output is "GND".

Table 8. Input Selector 2 (Serial Control Mode)

■ Video Block

The Video Amp has drivability for a load resistance of 150Ω. The AK4254 has composite input and output with low pass filter (LPF). Internal negative power supply circuit supplies the negative voltage to the video amp and the video amp 0V output is used for a pedestal level. Therefore, the output coupling capacitor can be removed.

The negative power supply circuit needs capacitors of Ca and Cb with 1.0μ, which should have the low ESR (Equivalent Series Resistance). When those capacitors have the polarity, each positive polarity pins should be connected to CP and VSS side.

The negative power supply circuit generates the negative voltage to use the clock that corresponds to the input video signal. When there is no video input signal and the negative voltage is insufficient (CVEE > -0.8V) in case of low quality input signal (Note: 17), the negative power supply circuit generates the negative voltage by using the internal oscillator circuit. The VOUT outputs -0.6V(typ) when there is no video signal input.

Note: 17. Low quality video signal has the following characteristics.

Input Sync Tip Level= -0.43V~ -0.14V (from the pedestal voltage)

Horizontal Line Sync Pulse=4.0μs ~5.4μs, Equalizing Pulse=2.0μs ~2.7μs, Serration Pulse=4.0μs ~5.4μs

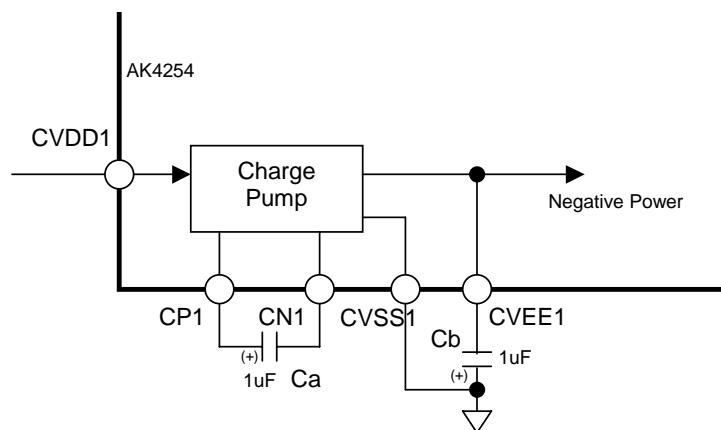


Figure 3. Negative Power Supply Circuit

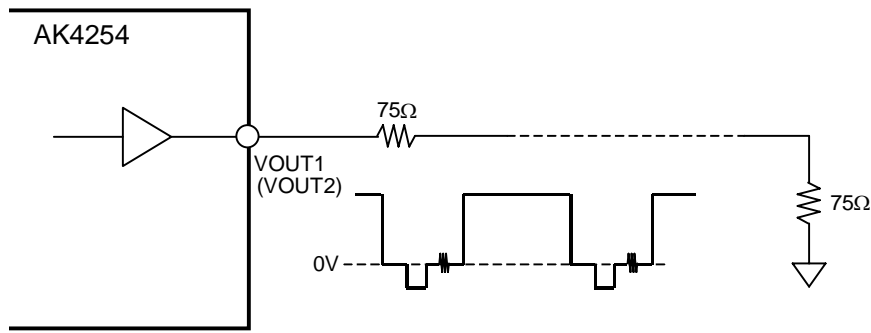


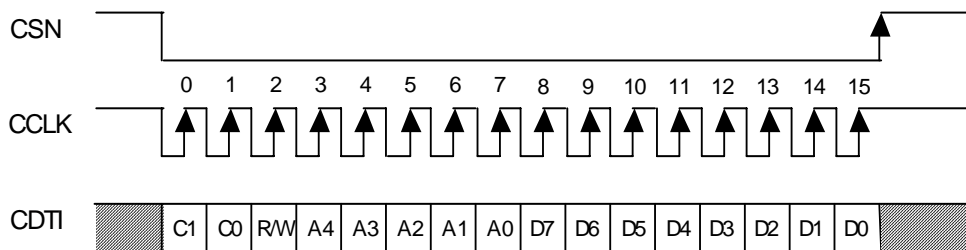
Figure 4. Video Signal Output

■ Serial Interface

The AK4254 can select 3-wire Serial mode (I2C pin = “L”) or I<sup>2</sup>C Bus mode (I2C pin = “H”).

1.3-wire Serial mode (I2C pin = “L”)

Internal registers may be written by using the 3-wire  $\mu$ P interface pins (CSN, CCLK and CDTI pins). The data on this interface consists of a 2-bit Chip address (C1 and C2 are set by CAD1, CAD0pin), Read/Write (Fixed to “1”), Register address (MSB first, 5bits) and Control data (MSB first, 8bits). If the Chip address matches the setting of the CAD1 pin and CAD0pin, the AK4254 operation is executed. Each bit is clocked in on the rising edge (“ $\uparrow$ ”) of CCLK. Address and data are latched on the 16th CCLK rising edge (“ $\uparrow$ ”) after CSN falling edge (“ $\downarrow$ ”). CSN should be set to “H” once after 16 CCLKs for each address. Clock speed of CCLK is 5MHz (max). The value of internal registers are initialized by the PDN pin = “L”.



C1,C0: Chip Address: (C1= CAD1, C0 = CAD0)  
 R/W: READ/WRITE (Fixed to “1”: WRITE)  
 A4-A0: Register Address  
 D7-D0: Control Data

Figure 5. 3-wire Serial mode I/F timing

## 2. I<sup>2</sup>C Bus mode

The AK4254 supports the fast-mode I2C-bus (max: 400kHz).

### 2-1. WRITE operations

Figure 6 shows the data transfer sequence for the I2C-bus mode. All commands are preceded by a START condition. A HIGH to LOW transition on the SDA line while SCL is HIGH indicates the START condition (Figure 12). After the START condition, a slave address is sent. This address is 7 bits long followed by the eighth bit that is a data direction bit (R/W). The most significant six bits of the slave address are fixed as “00100”. The next bits are CAD0-1 (device address bit). This bit identifies the specific device on the bus. The hard-wired input pin (CAD0-1 pins) sets these device address bits(Figure 7). If the slave address matches that of the AK4254, the AK4254 generates an acknowledge and the operation is executed. The master must generate the acknowledge-related clock pulse and release the SDA line (HIGH) during the acknowledge clock pulse (Figure 13). A R/W bit value of “1” indicates that the read operation is to be executed. A “0” indicates that the write operation is to be executed.

The second byte consists of the control register address of the AK4254. The format is MSB first, and those most significant 7-bits are fixed to zeros (Figure 8). The data after the second byte contains control data. The format is MSB first, 8bits (Figure 9). The AK4254 generates an acknowledge after each byte has been received. A data transfer is always terminated by a STOP condition generated by the master. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition (Figure 12).

The AK4254 can perform more than one byte write operation per sequence. After receipt of the third byte the AK4254 generates an acknowledge and awaits the next data. The master can transmit more than one byte instead of terminating the write cycle after the first data byte is transferred. After receiving each data packet the internal 1-bit address counter is incremented by one, and the next data is automatically taken into the next address.

The data on the SDA line must remain stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW (Figure 14) except for the START and STOP conditions.

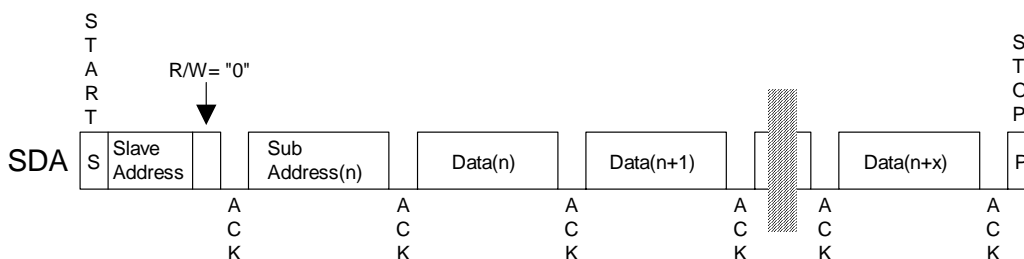


Figure 6. Data Transfer Sequence at the I<sup>2</sup>C-Bus Mode

0	0	1	0	0	CAD1	CAD0	R/W
---	---	---	---	---	------	------	-----

Figure 7. The First Byte (Those CAD1/0 should match with CAD1/0 pins)

0	0	0	0	0	0	0	A0
---	---	---	---	---	---	---	----

Figure 8. The Second Byte

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

Figure 9. Byte Structure after the Second Byte

2-2. READ Operations

(2)-2. READ Operations

Set the R/W bit = "1" for the READ operation of the AK4254. After transmission of data, the master can read the next address's data by generating an acknowledge instead of terminating the write cycle after the receipt of the first data word. After receiving each data packet the internal 2-bit address counter is incremented by one, and the next data is automatically taken into the next address. If the address exceeds 01H prior to generating a stop condition, the address counter will "roll over" to 00H and the previous data will be overwritten.

The AK4254 supports two basic read operations: CURRENT ADDRESS READ and RANDOM ADDRESS READ.

2-2-1. CURRENT ADDRESS READ

The AK4254 contains an internal address counter that maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either a read or write) were to address n, the next CURRENT READ operation would access data from the address n+1. After receipt of the slave address with R/W bit set to "1", the AK4254 generates an acknowledge, transmits 1-byte of data to the address set by the internal address counter and increments the internal address counter by 1. If the master does not generate an acknowledge to the data but instead generates a stop condition, the AK4254 ceases transmission.

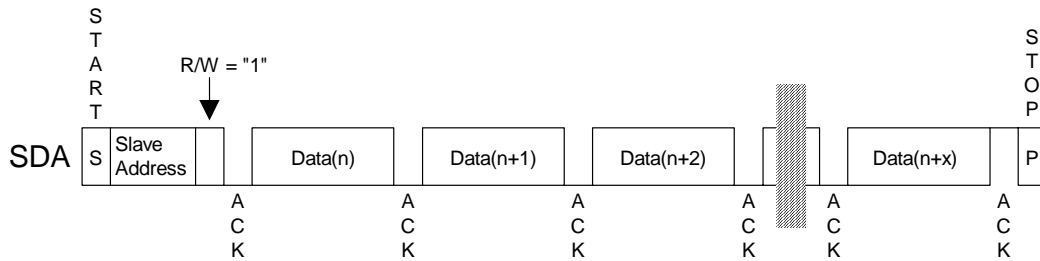


Figure 10. CURRENT ADDRESS READ

2-2-2. RANDOM ADDRESS READ

The random read operation allows the master to access any memory location at random. Prior to issuing the slave address with the R/W bit set to "1", the master must first perform a "dummy" write operation. The master issues a start request, a slave address (R/W bit = "0") and then the register address to read. After the register address is acknowledged, the master immediately reissues the start request and the slave address with the R/W bit set to "1". The AK4254 then generates an acknowledge, 1 byte of data and increments the internal address counter by 1. If the master does not generate an acknowledge to the data but instead generates a stop condition, the AK4254 ceases transmission.

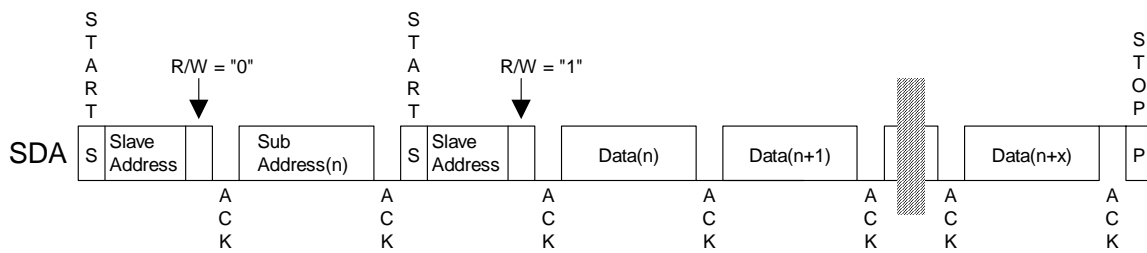


Figure 11. RANDOM ADDRESS READ

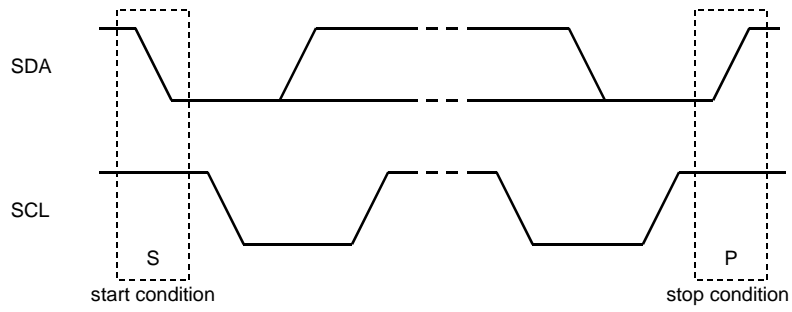


Figure 12. START and STOP Conditions

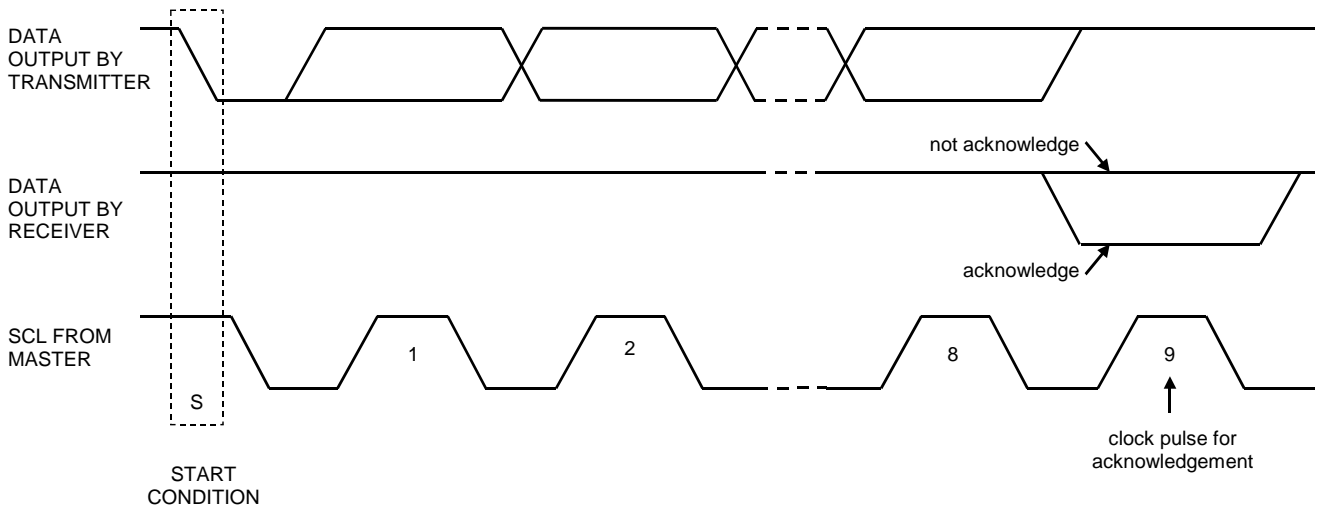


Figure 13. Acknowledge on the I<sup>2</sup>C-Bus

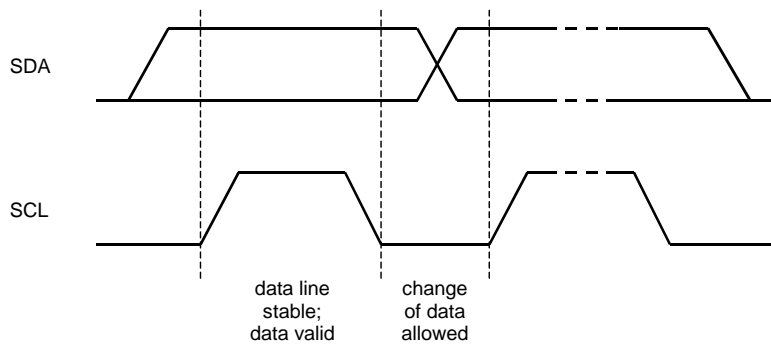


Figure 14. Bit Transfer on the I<sup>2</sup>C-Bus

## ■ Register Map

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Input Selector Control	0	SEL22	SEL21	SEL20	0	SEL12	SEL11	SEL10
01H	(Reserved)	0	0	0	0	0	0	0	0

The PDN pin = “L” resets the all registers to their default values.

(Note: 18) “The “0” register should be written “0”, the “1” register should be written “1” data.

(Note: 19) Do not write any data to the register except 00H.

## ■ Register Definitions

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Input Selector Control	0	SEL22	SEL21	SEL20	0	SEL12	SEL11	SEL10
	Default	0	0	0	0	0	0	0	0

SEL12-10: Input Selector 1 Control (Table 7)  
The default is “000” (VOUT1 output is “GND”).

SEL22-20: Input Selector 2 Control (Table 8)  
The default is “000” (VOUT2 output is “GND”).

**SYSTEM DESIGN**

Figure 15~Figure 17 show the system connection diagram. An evaluation board (AKD4254) is available in order to allow an easy study on the layout of a surrounding circuit.

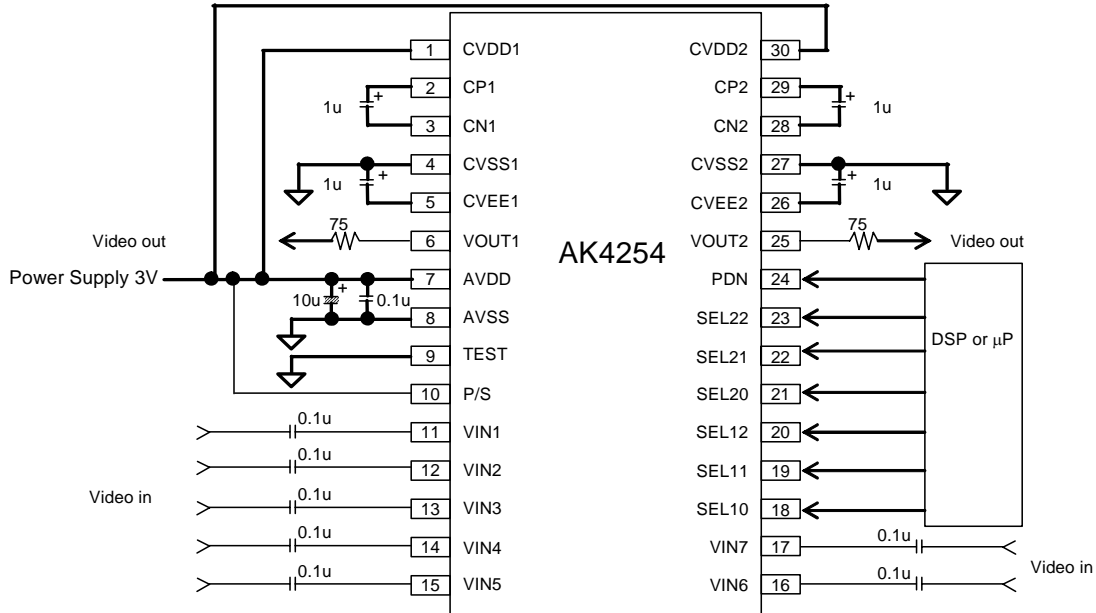


Figure 15. Typical Connection Diagram (Parallel Control Mode)

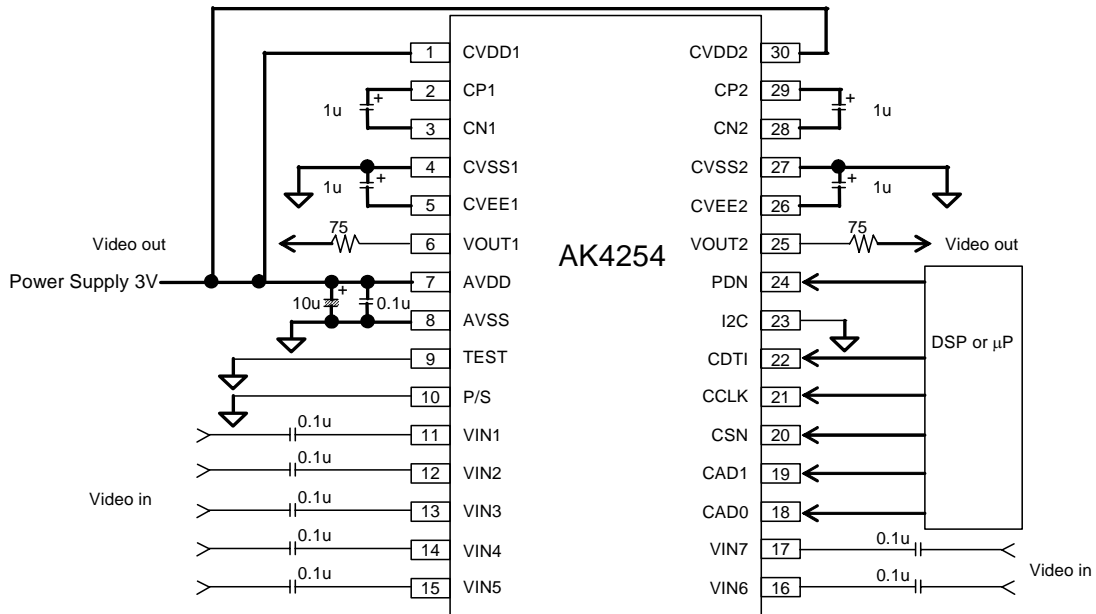


Figure 16. Typical Connection Diagram (Serial Control Mode: 3-wire Serial mode)

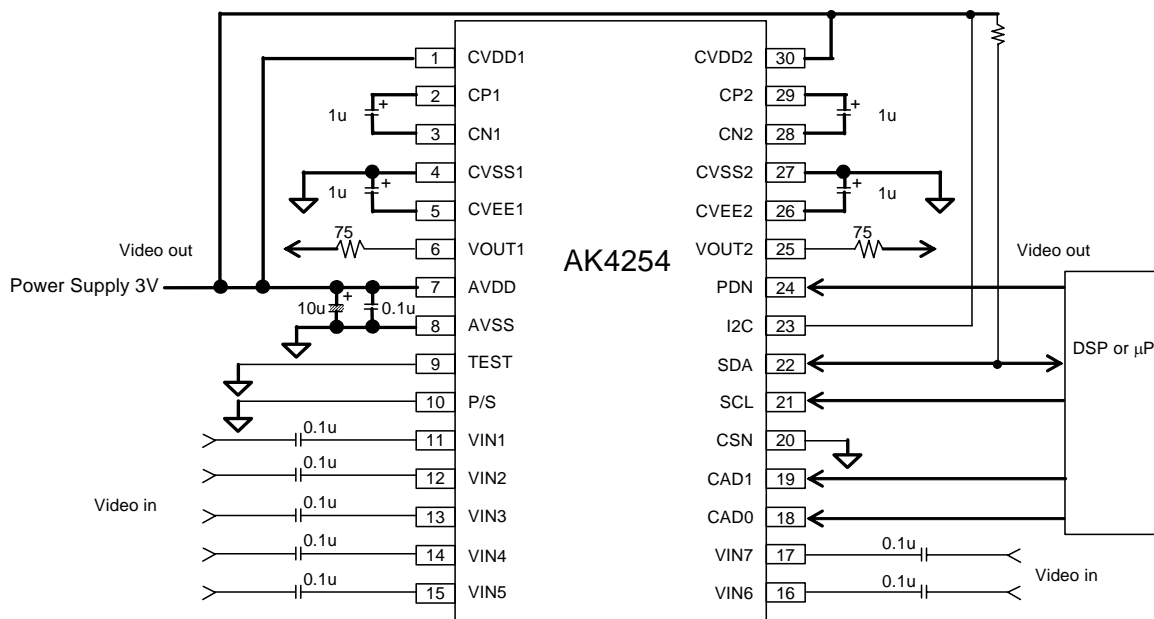


Figure 17. Typical Connection Diagram (Serial Control Mode: I<sup>2</sup>C Bus mode)

### 1. Grounding and Power Supply Decoupling

The AK4254 requires careful attention to power supply and grounding arrangements. AVDD, CVDD1 and CVDD2 are usually supplied from the system’s analog supply. AVSS, CVSS1 and CVSS2 of the AK4254 should be connected to the analog ground plane. System analog ground and digital ground should be connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitors should be as near to the AK4254 as possible, with the small value ceramic capacitor being the nearest.

### 2. Analog Inputs

Usually the input signal is AC coupled using 0.1µF capacitor (Figure 15, Figure 16, Figure 17).

### 3. The notes for drawing the board

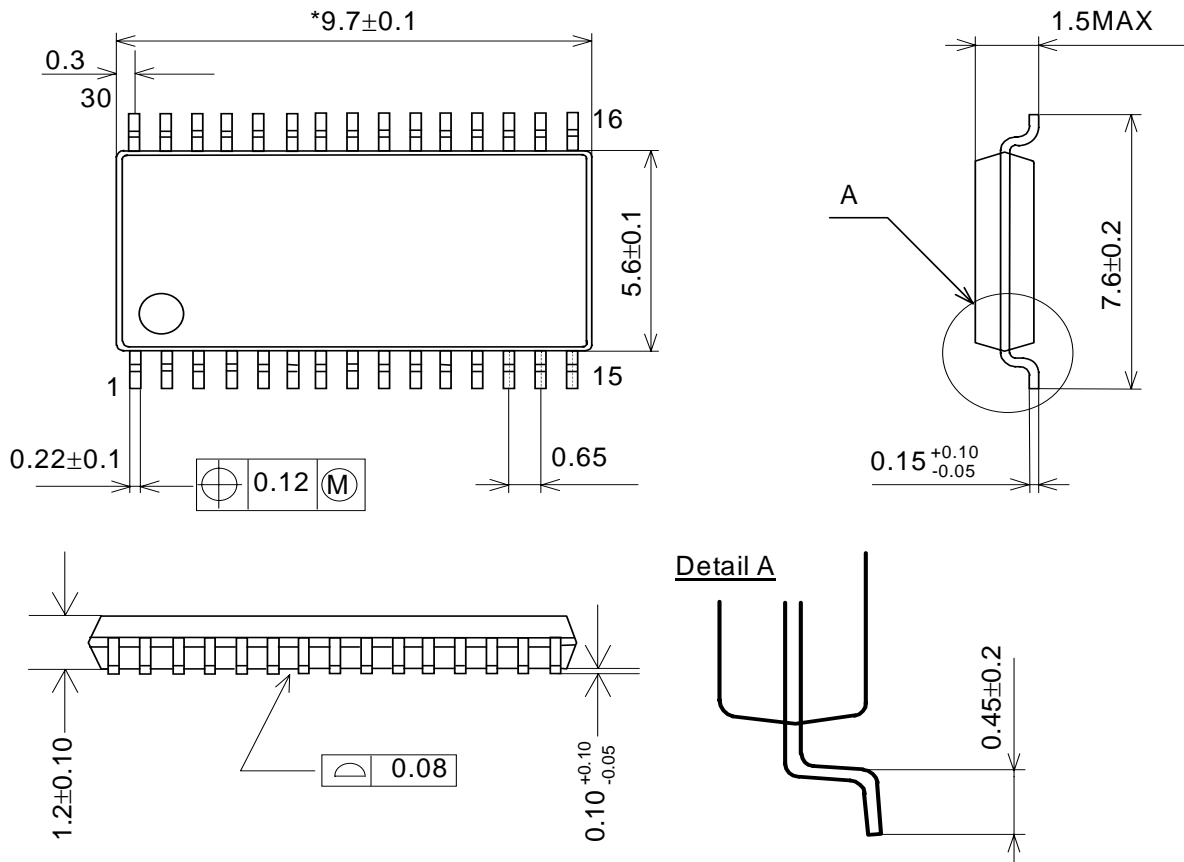
Analog input and output pins should be as short as possible in order to avoid unwanted coupling into the AK4254. The unused pins should be open.

### 4. Video Output

The AK4254 are on-chip 2ch video amp for drive 150Ω resistance. The gain of each amp is +6dB (typ) (Figure 1).

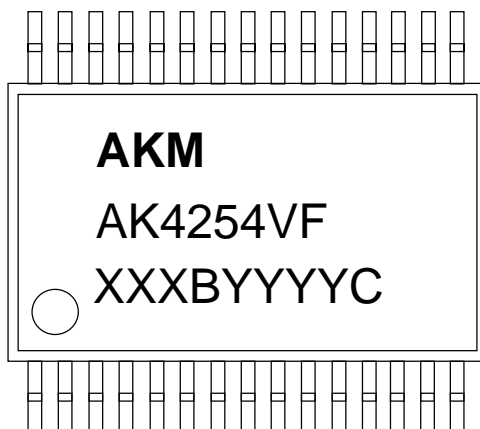
**PACKAGE**

**30pin VSOP (Unit: mm)**



NOTE: Dimension "\*" does not include mold flash.

**MARKING**



XXXXYYYYC    Date code identifier

XXXXB: Lot number (X: Digit number, B: Alpha character)  
YYYYC: Assembly date (Y: Digit number, C: Alpha character)

**REVISION HISTORY**

Date (YY/MM/DD)	Revision	Reason	Page	Contents
07/02/20	00	First Edition		
07/08/10	01	Spec change	6	Interchannel Isolation: typ.50dB → typ.65dB
		Spec change	7	Switching characteristics PDN “↑” to CSN “↓”: tPDCS was added PDN “↑” to SDA “↓” @SCL = “H”: tPDSD was added
		Spec change	8	Timing diagram WRITE command input timing was changed. (tPDCS was added) I <sup>2</sup> C Bus mode timing1 was added. (tPDSD was added)
		Error correct	18, 19	System design Figure15, Figure16, Figure17 were revised. (CVSS1 and CVSS2 were connected to GND)

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