	<h1 style="margin: 0;">AKD4388A-SA</h1> <h2 style="margin: 0;">AK4388A Evaluation board Rev.0</h2>
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General Description

The AKD4388A-SA is an evaluation board for AK4388A, which is 192kHz sampling 24Bit $\Delta\Sigma$ DAC. The AKD4388A-SA includes a LPF which can add differential analog outputs from the AK4388A and also has a digital interface. Therefore, it is easy to evaluate the AK4388A.

■ **Ordering Guide**

AKD4388A-SA --- Evaluation board for AK4388A

Function

- On-board Analog output buffer circuit
- On-board digital audio interface. (AK4113)

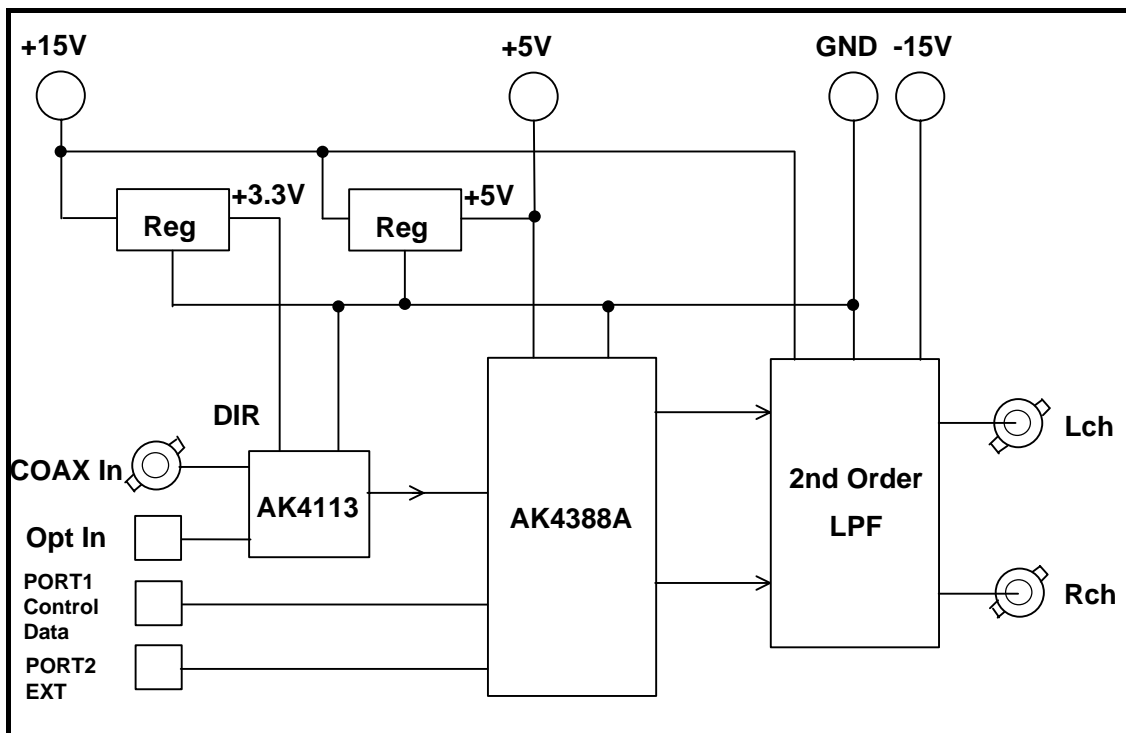


Figure 1. AKD4388A-SA Block diagram

* Circuit diagram are attached at the end of this manual.

COAX is recommended for an evaluation of the Sound quality.

■ Operation sequence

1) Set up the power supply lines. (See “Other jumpers set-up”.)

Name	Color	Voltage	Comments	Attention
+15V	Green	+12~+15V	For regulator and op-amps.	This jack should be always connected to power supply.
-15V	Blue	-12~-15V	For op-amps.	This jack should be always connected to power supply.
+5V	Red	+4.75~+5.25V	For AK4388A.	This jack should be always connected to power supply.
AGND	Black	0V	GND	This jack should be always connected to power supply.

Table 1. Set up of power supply lines

Each supply line should be distributed from the power supply unit.

- 2) Set-up the jumper pins
- 3) Set-up the DIP switches. (See the followings.)
- 4) Power on

The AK4388A should be reset once by bringing SW4 (PDN) “L” upon power-up.

■ Evaluation mode

1. DIR (COAX) (default)

It is possible to evaluate the AK4388A by using CD disk. The DIR generates MCLK, BICK, LRCK and SDATA from the received data through RCA connector (J3). Setting of jumper is shown below.

COAX is recommended for an evaluation of the Sound quality.

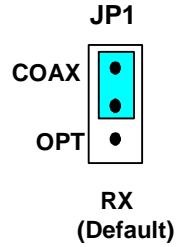


Figure 2. Jumper setting, when using DIR

2. DIR (Optical Link)

It is possible to evaluate the AK4388A by using CD disk. The DIR generates MCLK, BICK, LRCK and SDATA from the received data through optical connector (PORT3: TORX173). Setting of jumper is shown below.

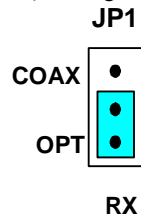


Figure 3. Jumper setting, when using DIR

3. All clocks are fed through the PORT2.

- R1, R2, R3, R4 : open
- R26, R27, R28, R30 : 100Ω or short (0Ω)

■ DIP Switch setting

[SW1]: AK4388A setting

No.	Pin	SW1 OFF	SW1 ON	Default
1	SMUTE	Soft Mute : “Disable”	Soft Mute : “Enable”	OFF
2	P/S	Always ON for Parallel Control mode only		ON
3	ACKS	Manual setting mode	Auto setting mode	ON
4	DIF0	Audio Data Formats Refer to Table7		OFF

Table 2. SW1 setting

[SW2]: AK4388A setting

No.	Pin		Default
1	-	NC	OFF
2	-	NC	OFF
3	DEM	De-emphasis Control setting Refer to Table6	OFF
4	DIF1	Audio Data Formats Refer to Table7	ON

Table 3. SW2 setting

[SW3]: AK4113 setting

No.	Pin	OFF	ON	Default
1	OCKS1	AK4113 Master Clock setting Refer to Table 5.		ON
2	OCKS0			OFF

Table 4. SW3 setting

The frequency of the master clock output is set by OCKS0 and OCKS1 as shown in Table 5.

OCKS1	OCKS0	MCLK Frequency	Default
0	0	256fs @fs=88.2/96kHz	
1	0	512fs @32/44.1/48kHz	
1	1	128fs @176.4/192kHz	

Table 5. MCLK Clock

The digital de-emphasis filter is set by DEM pin as follows.

DEM SW	DEM pin state	De-emphasis Filter	Default
OFF	1	ON	
ON	0	OFF	

Table 6. De-emphasis Filter Control

Data is shifted in via the SDTI pin using BICK and LRCK inputs. The DIF0-1 as shown in Table 7 can select four serial data modes.

Mode	DIF1 SW	DIF0 SW	DIF1 pin state	DIF0 pin state	SDTI Format	BICK	Default
0	ON	ON	0	0	16bit LSB justified	≥32fs	
1	ON	OFF	0	1	24bit LSB justified	≥48fs	
2	OFF	ON	1	0	24bit MSB justified	≥48fs	
3	OFF	OFF	1	1	16/24bit I ² S Compatible	≥48fs or 32fs	

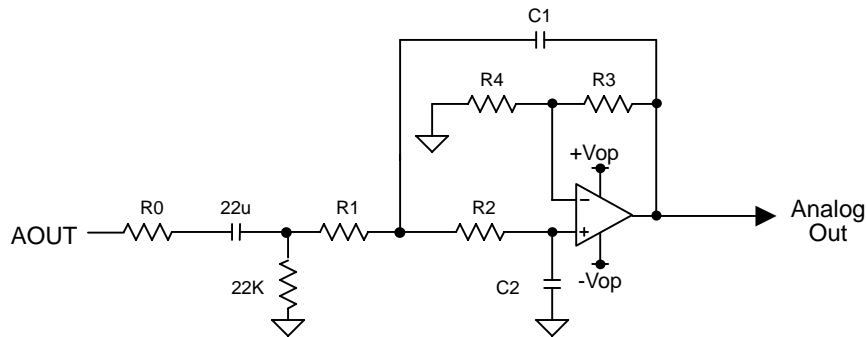
Table 7. Audio Data Formats

■ **Toggle switch setting**

[SW4](PDN): Reset of AK4388A. Select “H” during operation.

■ External Analog Circuit

The 2nd order LPF ($f_c=125.6\text{kHz}$, $Q=0.753$) which adds differential outputs of the AK4388A is implemented on the board. When the further attenuation of the out-band noise is needed, some additional LPF is required. Analog signal is output through BNC connectors on the board. And the output level of the AK4388A is $5.67\text{Vpp}@5\text{V}$.



$f_c=125.6\text{kHz}$, $Q=0.753$, $g=0.060\text{dB}$ at 40kHz

Figure 4. External Analog Filter

R_0	R_1	R_2	R_3	R_4	C_1	C_2
910	1.8k	3.9k	3.3k	3.9k	390p	390p

Table 8. The value of R,C on this board

f_{in}	20kHz	40kHz	80kHz
Frequency Response	0.023dB	0.060dB	-0.288dB

Table 9. Frequency Response of LPF

<Calculation>

$$\text{Amplitude} = 20 \log \frac{K}{\sqrt{[1-(f/f_c)^2]^2 + [(1/Q)(f/f_c)]^2}} \text{ [dB]},$$

$$K = \frac{R_3 + R_4}{R_4},$$

$$f_c = \frac{\omega_0}{2\pi},$$

$$\omega_0 = \frac{1}{\sqrt{C_1 C_2 R_1 R_2}},$$

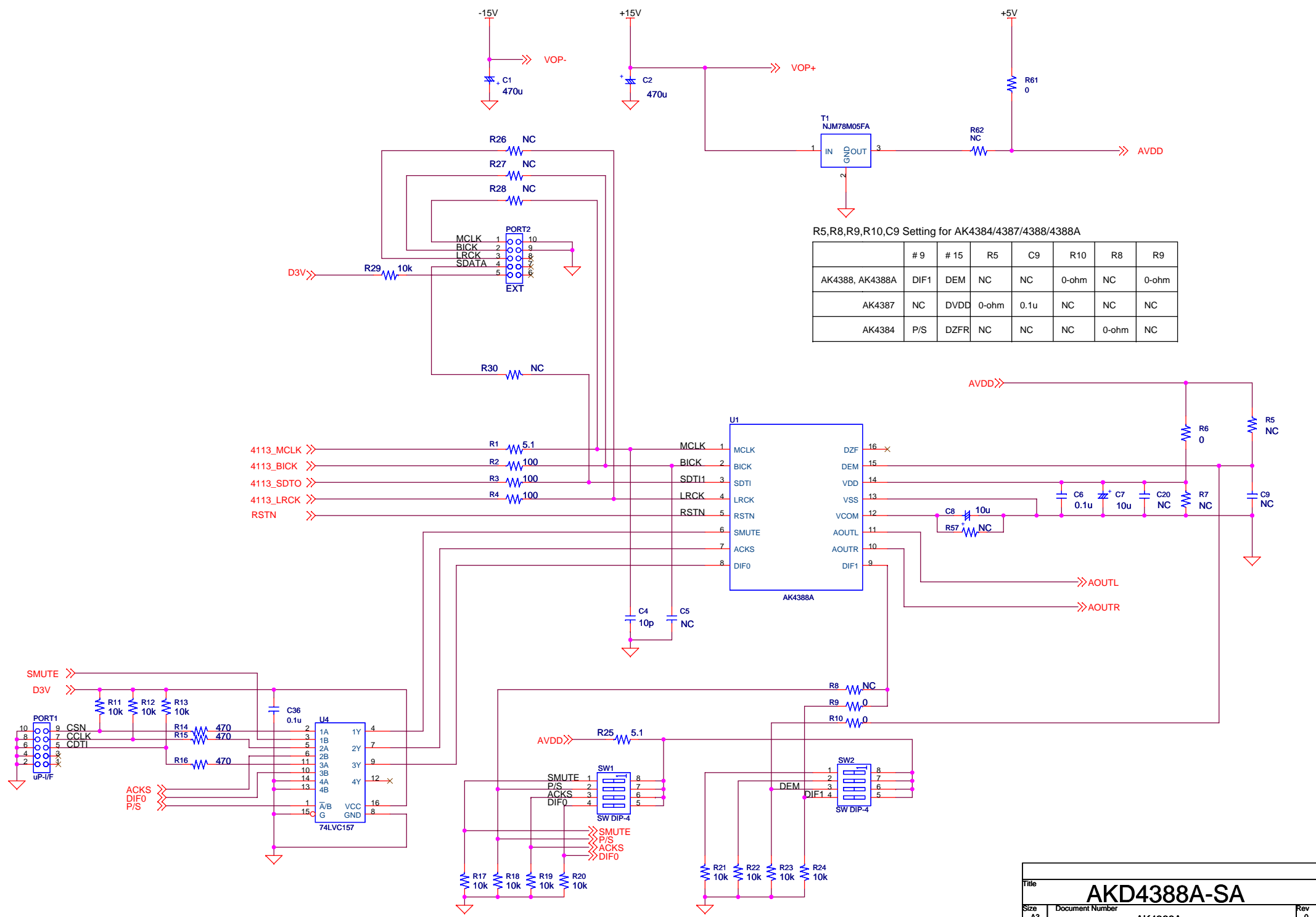
$$Q = 2\pi f_c \frac{1}{\frac{1}{C_1 R_1} + \frac{1}{C_1 R_2} + \frac{1-k}{C_2 R_2}}$$

REVISION HISTORY

Date (YY/MM/DD)	Manual Revision	Board Revision	Reason	Page	Contents
08/06/20	KM095600	0	First Edition		

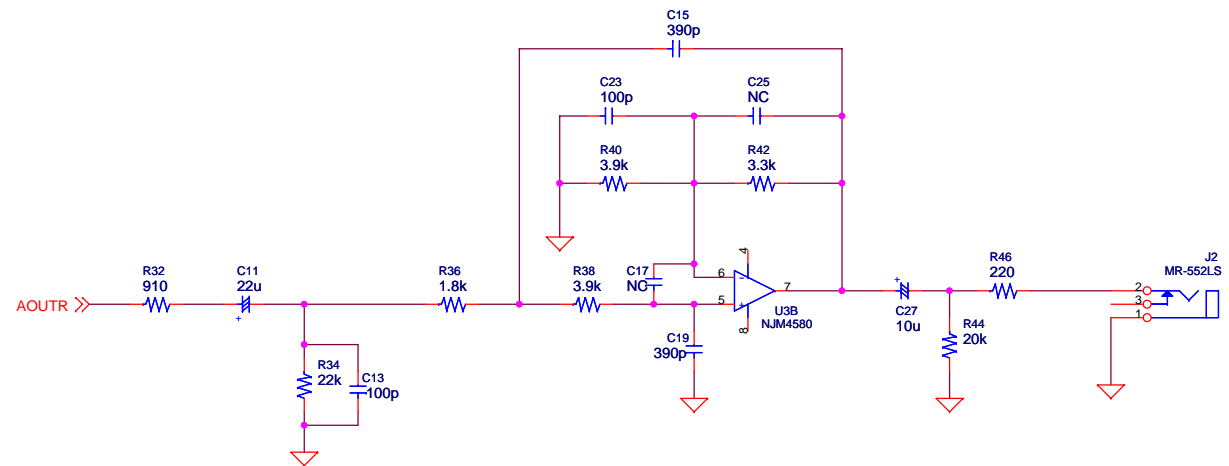
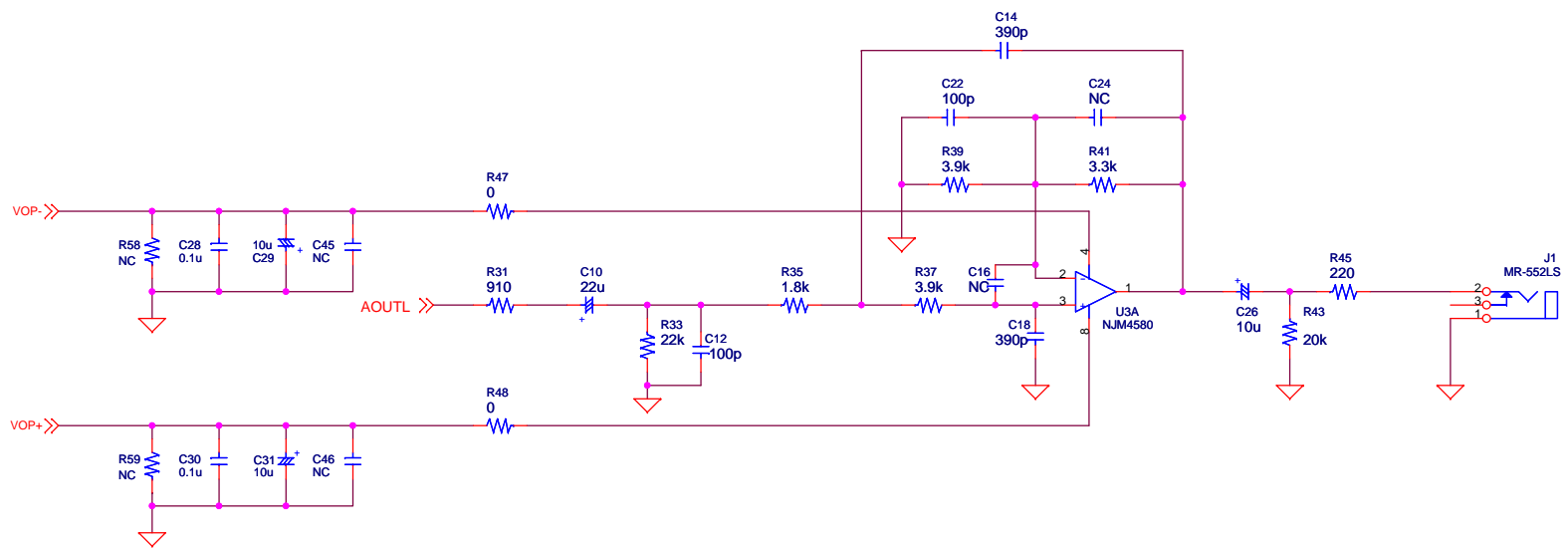
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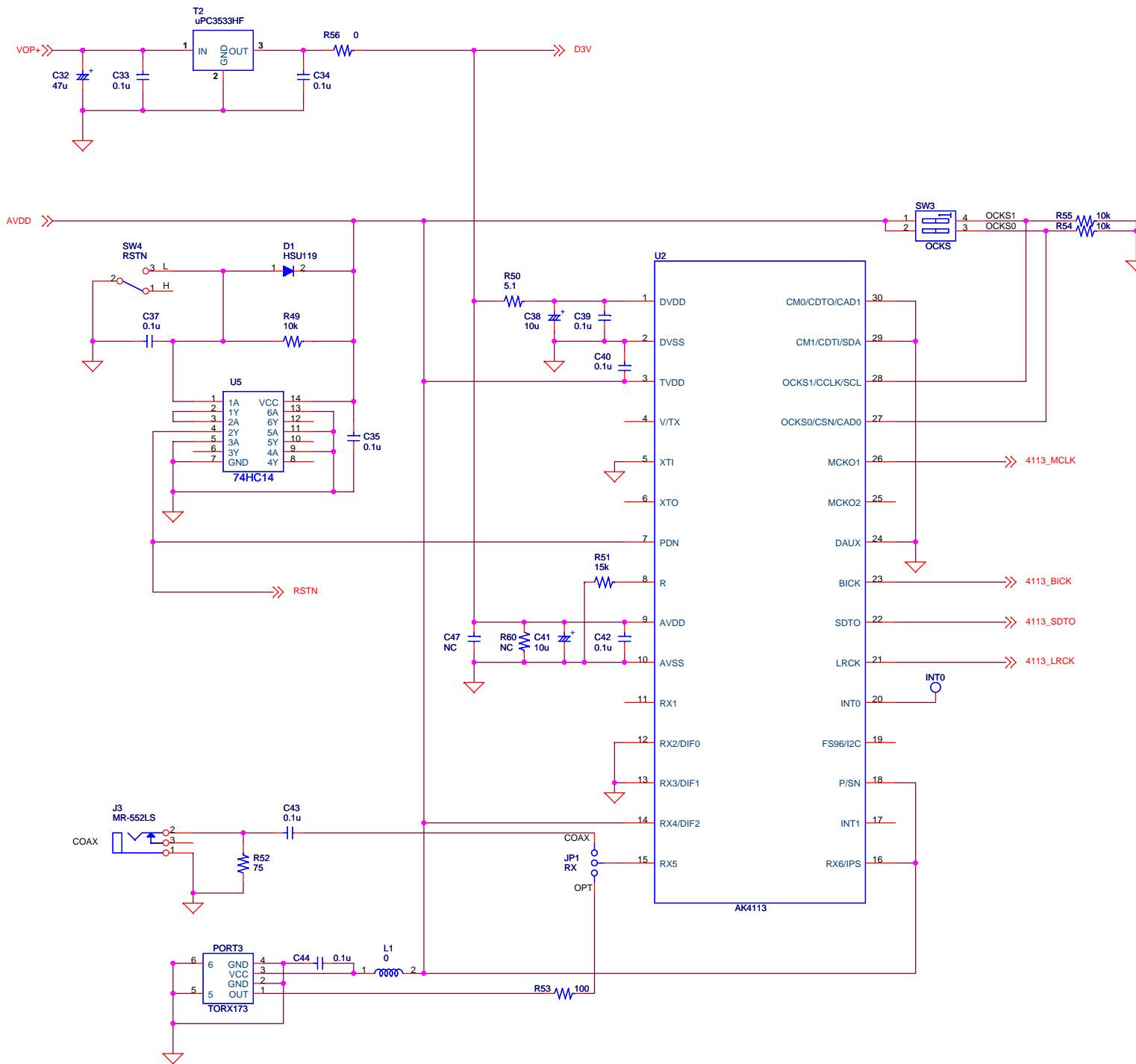


R5,R8,R9,R10,C9 Setting for AK4384/4387/4388/4388A

	# 9	# 15	R5	C9	R10	R8	R9
AK4388, AK4388A	DIF1	DEM	NC	NC	0-ohm	NC	0-ohm
AK4387	NC	DVDD	0-ohm	0.1u	NC	NC	NC
AK4384	P/S	DZFR	NC	NC	NC	0-ohm	NC



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S3

OCKS1	OCKS0	Master Clock
H	L	512fs@fs=32k/44.1k/48kHz
L	L	256fs@fs=88.2k/96kHz
H	H	128fs@fs=176.4k/192kHz