AKD4629-A
Evaluation board Rev.1 for AK4629

GENERAL DESCRIPTION

The AKD4629-A is an evaluation board for the AK4629, a single chip CODEC that includes four channels of ADC and six channels of DAC. The AKD4629-A also has the digital audio interface and can achieve the interface with digital audio systems via opt-connector or BNC connector.

■ Ordering guide

AKD4629-A --- AK4629 Evaluation Board
(Cable for connecting with printer port of IBM-AT compatible PC and control software are packed with this.) This control software can't operate on Windows NT.

FUNCTION

- **On-board analog output buffer circuit**
- **Compatible with 2 types of interface**
  - **AK4118 (DIT&DIR) with optical output/input and BNC output/input**
  - **Direct interface with AC3 decoder by 10pin header**
- **10pin header for serial control interface**

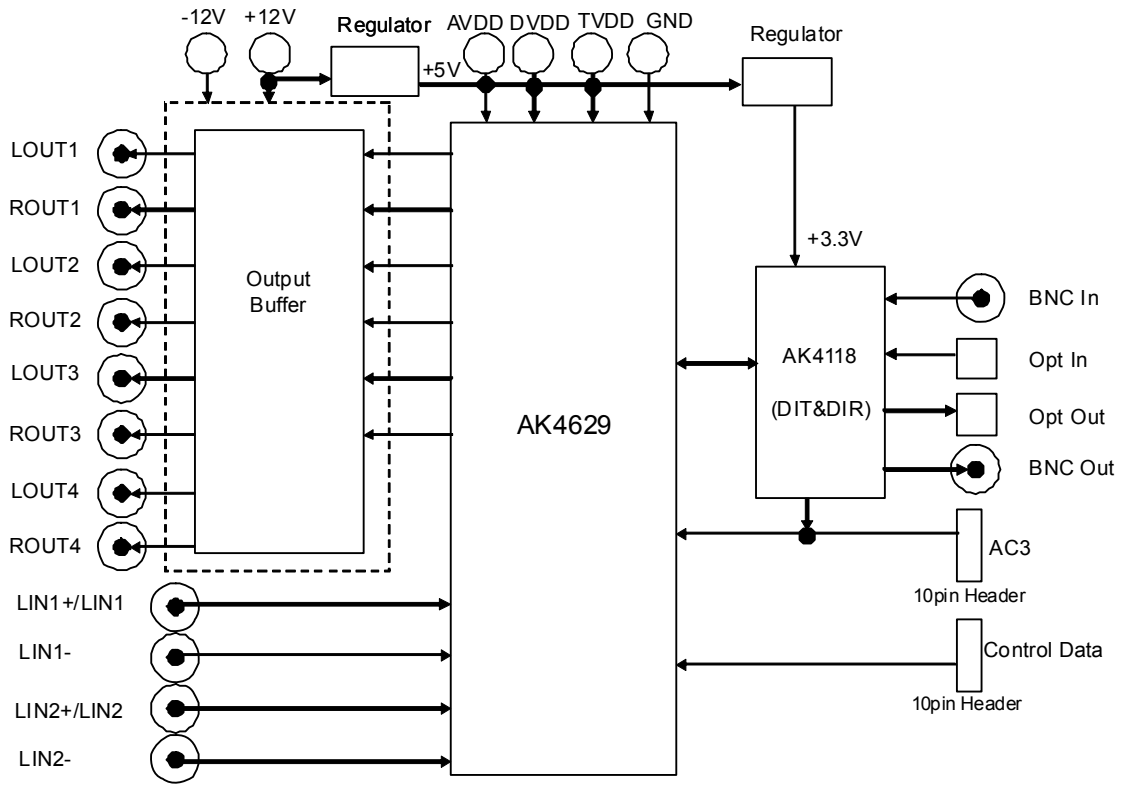


Figure 1 AKD4629-A Block Diagram

*Circuit diagram and PCB layout are attached at the end of this manual.

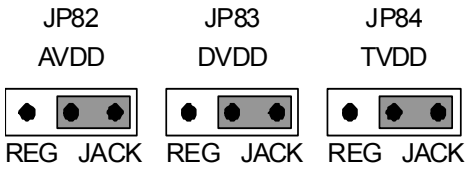
Evaluation Board Manual

■ Operation sequence

1) Set up the power supply lines.

(1-1) In case of using separate power supply lines <Default>

Set up the jumper pins.



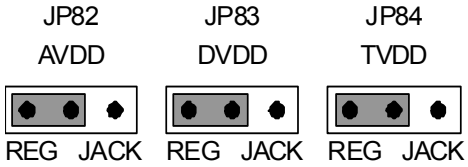
Set up the power supply lines.

Name	Color	Voltage	Comments	Attention
+12V	Red	+12V	Regulator, Power Supply for Op-amp	Should be connected.
-12V	Red	-12V	Power Supply for Op-amp	Should be connected.
AVDD	Orange	+5V	Power supply for AVDD of the AK4629	Should be connected.
DVDD	Orange	+5V	Power supply for DVDD of the AK4629	Should be connected.
TVDD	Orange	+5V	Power supply for TVDD of the AK4629	Should be connected.
AGND	Black	0V	Analog ground	Should be connected.
DGND	Black	0V	Digital ground	Should be connected.

Table 1 Set up of power supply lines

(1-2) In case of using the regulator

Set up the jumper pins.



Set up the power supply lines.

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+12V	Red	+12V	Regulator, Power Supply for Op-amp	Should be connected.
-12V	Red	-12V	Power Supply for Op-amp	Should be connected.
AVDD	Orange	+5V	Power supply for AVDD of the AK4629	Should be open.
DVDD	Orange	+5V	Power supply for DVDD of the AK4629	Should be open.
TVDD	Orange	+5V	Power supply for TVDD of the AK4629	Should be open.
AGND	Black	0V	Analog ground	Should be connected.
DGND	Black	0V	Digital ground	Should be connected.

Table 2 Set up of power supply lines

2) Set up the evaluation mode, jumper pins. (See the followings)

3) Power on.

The AK4629 and AK4118 should be reset once bringing SW1 "L" upon power-up.

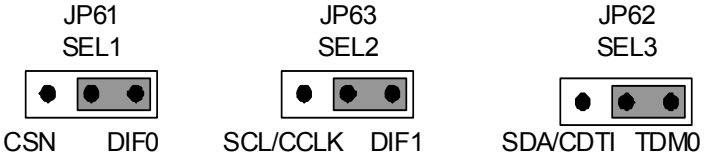
■ Control mode

(1) Parallel control mode <Default>

(1-1) Set up Parallel/Serial select pin

Set up SW2-6 (PS) to "H". (See Table 3)

(1-2) Set up the jumper pins

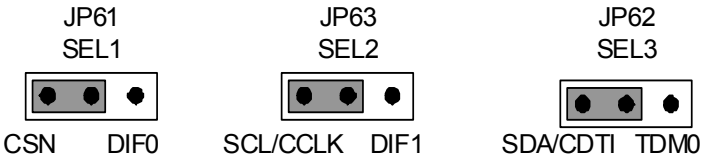


(2) Serial control mode

(1-1) Set up Parallel/Serial select pin

Set up SW2-6 (PS) to "L". (See Table 3)

(1-2) Set up the jumper pins



■ Audio I/F evaluation mode

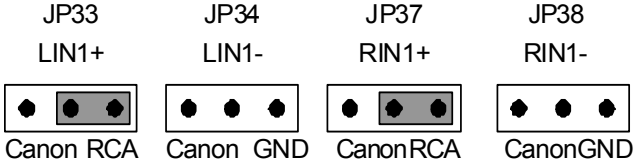
(1) Evaluation of ADC using DIT of AK4118

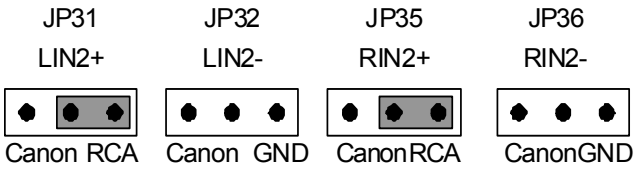
(1-1) Set up analog inputs

(1-1-1) Evaluation of ADC using DIT of AK4118 when single-ended inputs

PORT2 (DIT) or J2 (BNC_TX) is used. Nothing should be connected to PORT4 (AC3).
Set up SW2-2 (SGL) to H (See Table 3).

Set up the jumper pins.

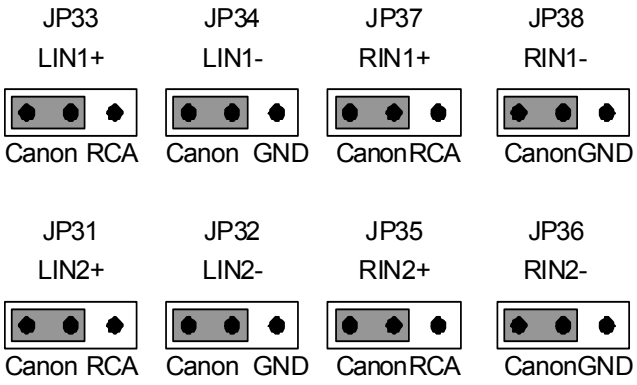




(1-1-2) Evaluation of ADC using DIT of AK4118 when differential inputs <Default>

PORT2 (DIT) or J2 (BNC_TX) is used. Nothing should be connected to PORT4 (AC3).
Set up SW2-2 (SGL) to L (See Table 3).

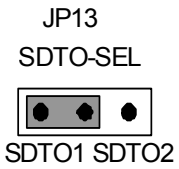
Set up the jumper pins.



(1-2) Set up the digital output

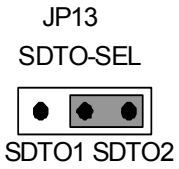
(1-2-1) In case of selecting SDTO1 <Default>

Set up the jumper pin.



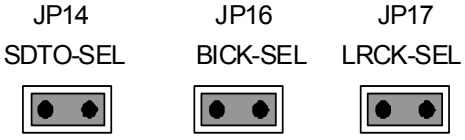
(1-2-2) In case of selecting SDTO2

Set up the jumper pin.



(1-3) Set up the audio interface.

Set up the jumper pins.



(2) Evaluation of DAC using DIR of AK4118 <Default>

J1 (BNC_RX) or PORT1 (DIR) is used. Nothing should be connected to PORT4 (AC3).

(2-1) Set up the digital inputs

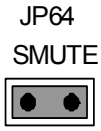
Set up the jumper pins (When SDTI1, SDTI2, SDTI3, SDTI4 are selected at the same time).

(2-2) Set up the audio interface

Set up the jumper pins.

(2-3) Set up the SMUTE pin

Set up the jumper pin.



When JP64 (SMUTE) is open, soft mute cycle is initialized.
When JP64 (SMUTE) is short, the output mute releases.

■ DIP Switch set up

[SW2] (MODE1): Mode settings for AK4629.
About the TDM mode of AK4629, please refer to Page 18 of AK4629's datasheet.

No.	Name	"H"	"L"	Default
1	TDM0	TDM Mode	Normal Mode	L
2	SGL	ADC Single-ended Input Mode	ADC Differential Input Mode	L
3	I2C	I2C Bus	3-wire Serial	L
4	DFS0	Double Speed	Normal Speed	L
5	DZFE	Zero Input Detect. Refer to the datasheet P23 of the AK4629.		L
6	PS	Parallel Control mode	Serial Control mode	H
7	CAD1	Chip Address Select. Refer to Table 9		L
8	CAD0			L

Table 3 Mode Setting for AK4629

[SW3] (AK4118 Mode_setting): Mode setting for AK4118.

No.	Name	"H"	"L"	Default
1	DIF2	AK4118's Audio Data Format Settings, and AK4629's Audio Data Format Settings when Parallel Control Mode. See Table 5 and Table 6		H
2	DIF1			L
3	DIF0			L
4	OCKS1	AK4118's Master Clock Settings. See Table 7		H
5	OCKS0			L
6	CM1	AK4118's Clock Operation Mode Select. See Table 8		L
7	CM0			L

Table 4 Mode Setting for AK4118

AK4118's audio data format and AK4629's audio data format are set up at the same time by settings of SW3-1 (DIF2), SW3-2 (DIF1) and SW3-3 (DIF0) when AK4629 is on Parallel Control Mode.

SW3-1 DIF2	SW3-2 DIF1	SW3-3 DIF0	AK4629 DIF1	AK4629 DIF0	AK4118 DAUX	AK4118 SDTO	LRCK		BICK		
0	1	0	0	0	24bit, Left justified	20bit, Right justified	H/L	O	64fs	O	
0	1	1	0	1	24bit, Left justified	24bit, Right justified	H/L	O	64fs	O	
1	0	0	1	0	24bit, Left justified	24bit, Left justified	H/L	O	64fs	O	(Default)
1	0	1	1	1	24bit, I^2S	24bit, I^2S	L/H	O	64fs	O	

Table 5 AK4114's Audio Data Format (Parallel control mode <Default>)

Both of settings of DIF1-0 bits of AK4629's registers and settings of SW3-1 (DIF2), SW3-2 (DIF1), SW3-3 (DIF0) are necessary when AK4629 is on Serial Control Mode.

Mode	DIF1 bit	DIF0 bit	SDTO1-2	SDTI1-3	
0	0	0	24bit, Left justified	20bit, Right justified	
1	0	1	24bit, Left justified	24bit, Right justified	
2	1	0	24bit, Left justified	24bit, Left justified	(Default)
3	1	1	24bit, I^2S	24bit, I^2S	

Table 6 AK4629's Audio data formats (Serial control mode)

AK4118 supplies AK4629's Master Clock with MCKO1.

No.	OCKS1	OCKS0	MCKO1	MCKO2	X'tal	fs (max)	
0	0	0	256fs	256fs	256fs	96 kHz	
1	0	1	256fs	128fs	256fs	96 kHz	
2	1	0	512fs	256fs	512fs	48 kHz	(default)
3	1	1	128fs	64fs	128fs	192 kHz	

Table 7 AK4118's Master Clock Frequency Select (Stereo mode)

Mode	CM1	CM0	PLL	X'tal	Clock source	SDTO	
0	0	0	ON	ON	PLL	RX	(default)
1	0	1	OFF	ON	X'tal	DAUX	
2	1	0	ON	ON	PLL	RX	
			ON	ON	X'tal	DAUX	
3	1	1	ON	ON	X'tal	DAUX	

ON: Oscillation (Power-up), OFF: STOP (Power-Down)

Table 8 AK4118's Clock Operation Mode select

■ Other jumper pins set up

1. JP81 (GND) : Connection between AGND and DGND.
   OPEN : AGND and DGND are separated on the board.
   SHORT : AGND and DGND are connected on the board. <Default>

2. JP11 (RX3) : Digital input connector selection for AK4118.
   OPT : Optical connector (PORT1) is used, except when Quad Speed Mode for DAC evaluation.
   BNC : BNC Jack (J1) is used. <Default>

3. JP12 (TX) : Digital output connector selection for AK4118.
   OPT : Optical connector (PORT2) is used.
   BNC : BNC Jack (J2) is used. <Default>

4. JP15 (MCLK_SEL): This jumper pin is fixed to SHORT. <Default>

■ The function of the toggle SW

[SW1] (PDN): Power down of AK4629 and AK4118. Keep "H" during normal operation.

■ The indication content for LED

[LE1] Monitor DZF1 pin of the AK4629.
[LE2] Monitor DZF2 pin of the AK4629.

About zero detection of AK4629, please refer to Page 23 of AK4629's datasheet.

■ Serial Control

The AK4629 can be controlled via the printer port (parallel port) of IBM-AT compatible PC. Connect PORT3 (CTRL) with PC by 10 wire flat cable packed with the AKD4629-A.

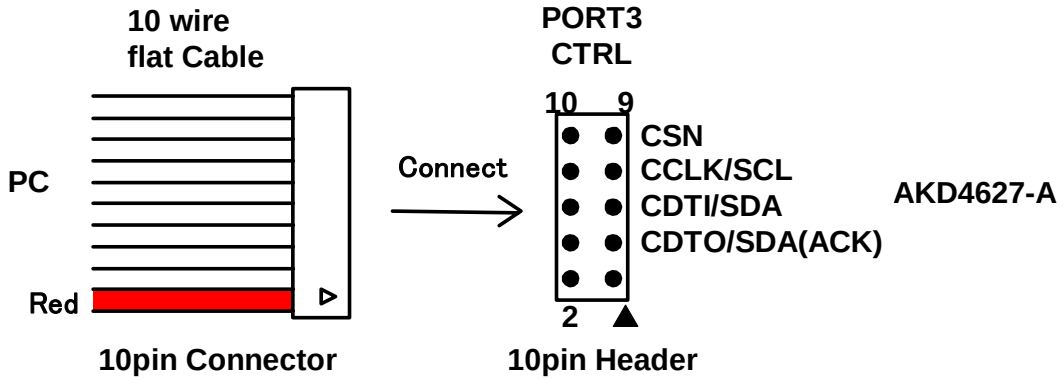


Figure 2 Connect of 10 wire flat cable

The AK4629 supports 3-wire serial control mode and I2C-bus control mode (fast-mode, max : 400kHz).
Please set the jump pins: JP61 (SEL1), JP63 (SEL2) and JP62 (SEL3), referred to (2) Serial Control Mode.

Mode	Chip Address	SW2-7 (CAD1)	SW2-8 (CAD0)	R/W	
3-wire	00	0	0	Write only	(default)
	01	0	1	Write only	
	10	1	0	Write only	
	11	1	1	Write only	
I2C	00	0	0	R/W	
	01	0	1	R/W	
	10	1	0	R/W	
	11	1	1	R/W	

Table 9 Select Interface and Chip Address

■ Analog Input/Output Circuits

1. Analog Input Circuits

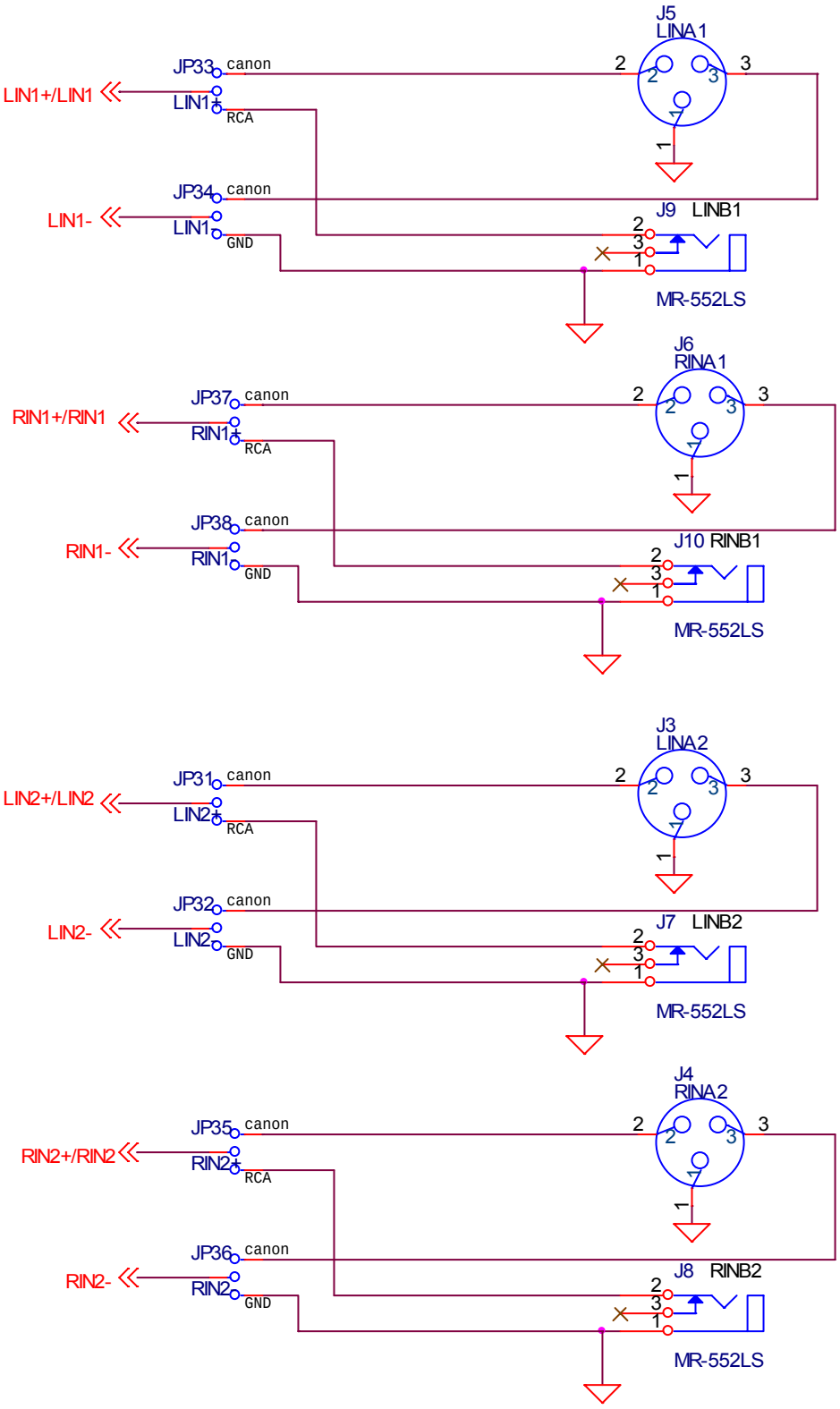


Figure 3 AKD4629-A Analog Input Circuits

2. Analog Output Circuits

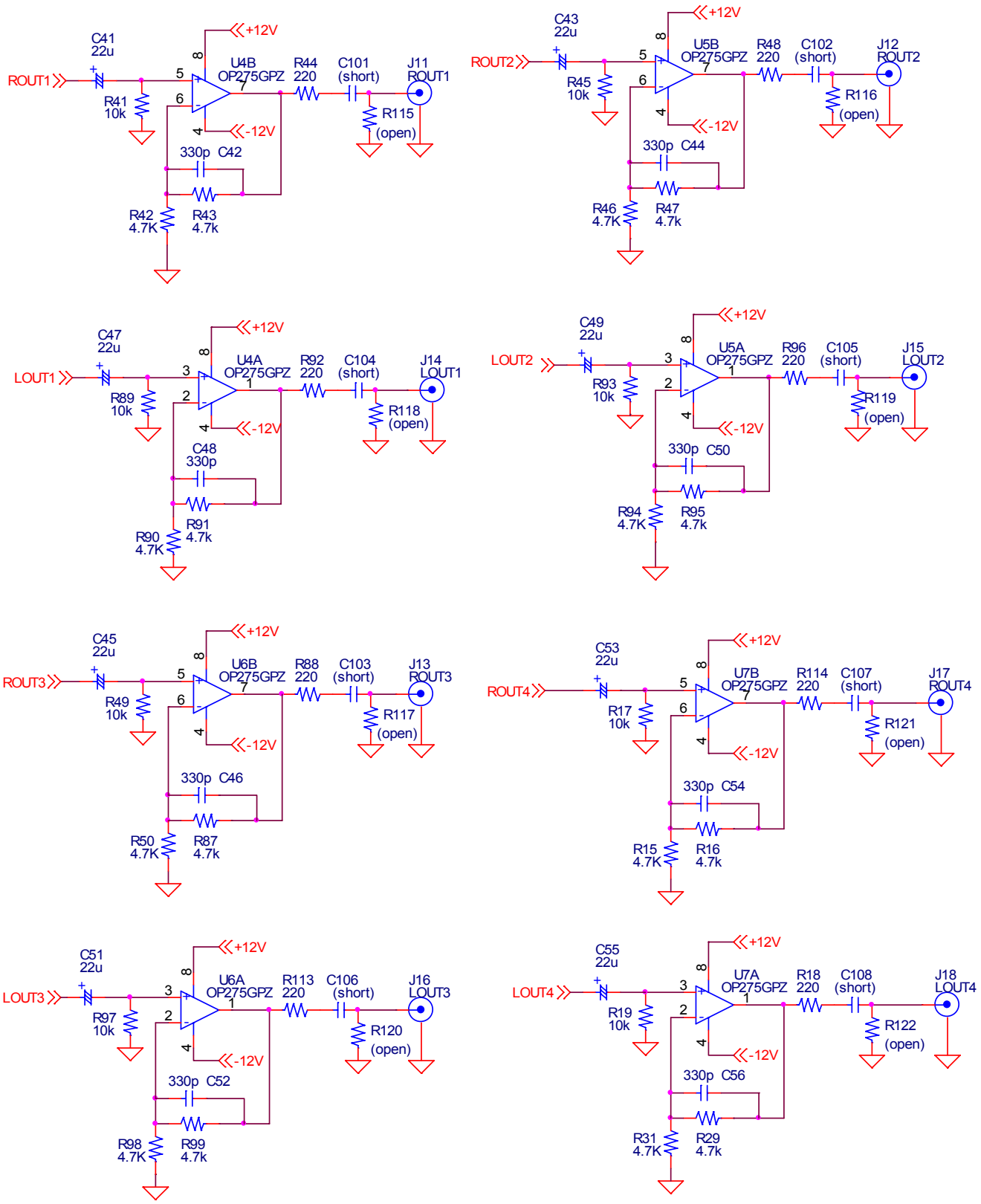


Figure 4 AKD4629-A Analog Output Circuits

Control Soft Manual

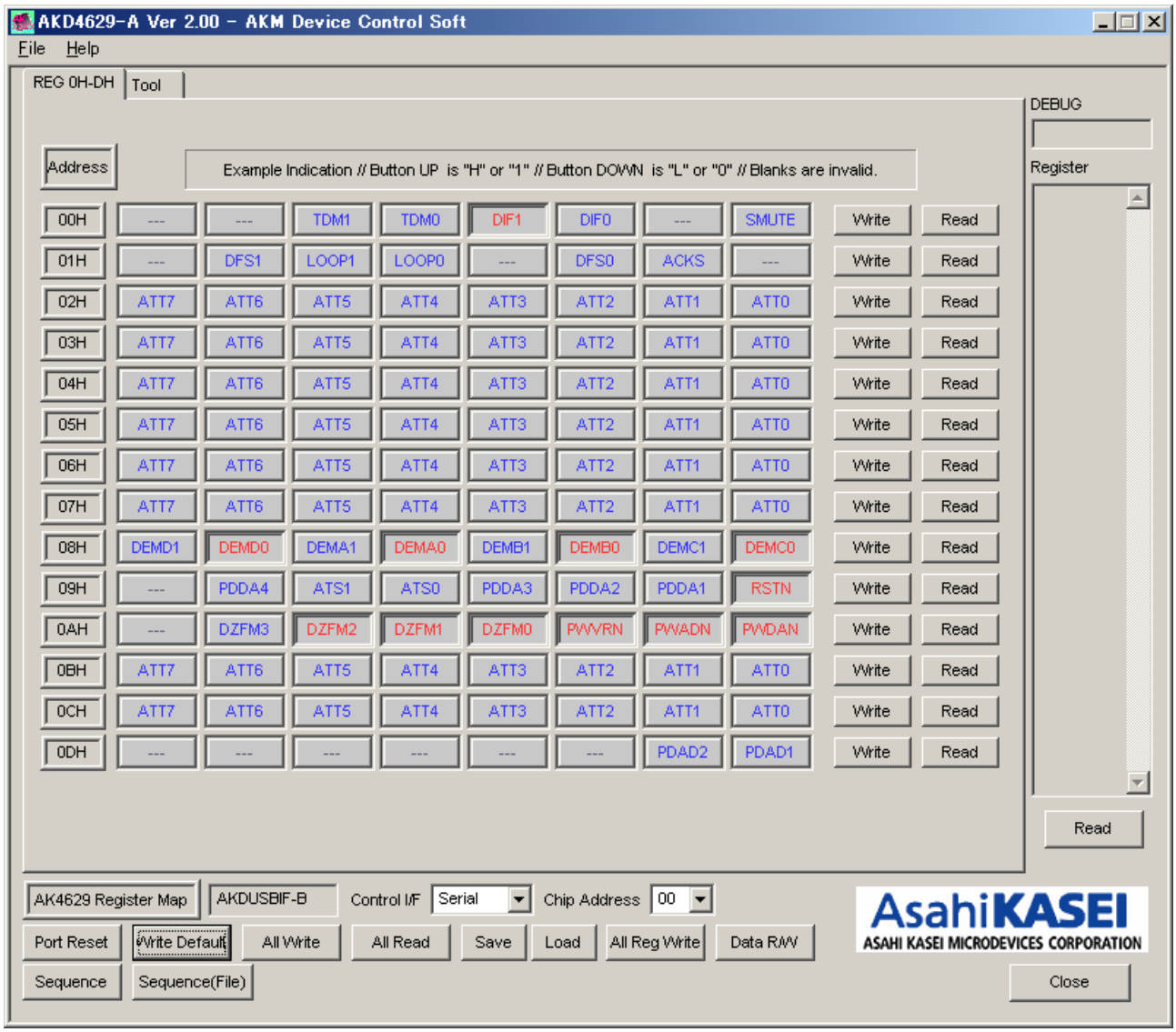
■ Evaluation Board and Control Soft Settings

1. Set an evaluation board properly.
2. Connect the evaluation board to an IBM PC/AT compatible PC by a 10 wire flat cable. Be aware of the direction of the 10pin header. When running this control soft on the Windows 2000/XP, the driver which is included in the CD must be installed. Refer to the "Driver Control Install Manual for AKM Device Control Software" for installing the driver. When running this control soft via an AKDUSBIF-B interface board, driver installing is not necessary.
3. Continue the evaluation by following the process below.

■ Operation Screen

1. Start up the control program following the process above.

The operation screen is shown below.



■ Operation Overview

Register map and testing tool can be controlled by this control soft. These controls are selected by upper tabs.

Buttons which are frequently used such as register initializing button “Write Default”, are located outside of the switching tab window. Refer to the “Dialog Boxes” for details of each dialog box setting.

1. [Port Reset]: For when connecting to USB I/F board (AKDUSBIF-A/B)
   Click this button after the control soft starts up when connecting USB I/F board (AKDUSBIF-A/B).

2. [Write Default]: Register Initializing
   When the device is reset by a hardware reset, use this button to initialize the registers.

3. [All Write]: Executing write commands for all registers displayed.

4. [All Read]: Executing read commands for all registers displayed.

5. [Save]: Saving current register settings to a file.

6. [Load]: Executing data write from a saved file.

7. [All Reg Write]: “All Reg Write” dialog box is popped up.

8. [Data R/W]: “Data R/W” dialog box is popped up.

9. [Sequence]: “Sequence” dialog box is popped up.

10. [Sequence(File)]: “Sequence(File)” dialog box is popped up.

11. [Read]: Reading current register settings and display on to the Register area (on the right of the main window).
    This is different from [All Read] button, it does not reflect to a register map, only displaying hexadecimal.

1. [REG]: Register Map

This tab is for a register writing and reading.

Each bit on the register map is a push-button switch.
Button Down indicates “H” or “1” and the bit name is in red (when read only it is in deep red).
Button Up indicates “L” or “0” and the bit name is in blue (when read only it is in gray)

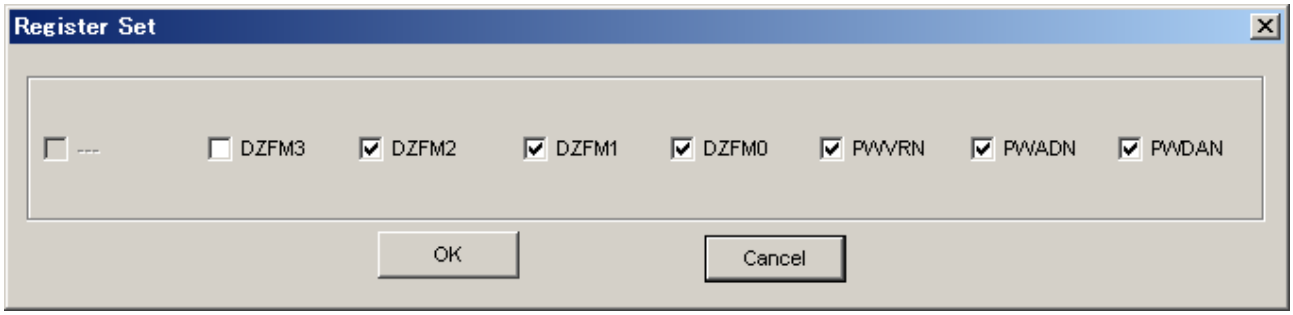
The registers which is not defined in the datasheet are indicated as “---”.

[Write]: Data Writing Dialog

It is for when changing two or more bits on the same address at the same time.

Click [Write] button located on the right of the each corresponded address for a pop-up dialog box.

When checking the checkbox, the register will be “H” or “1”, when not checking the register will be “L” or ”0”.
Click [OK] to write setting value to the registers, or click [Cancel] to cancel this setting.



[Read]: Data Read

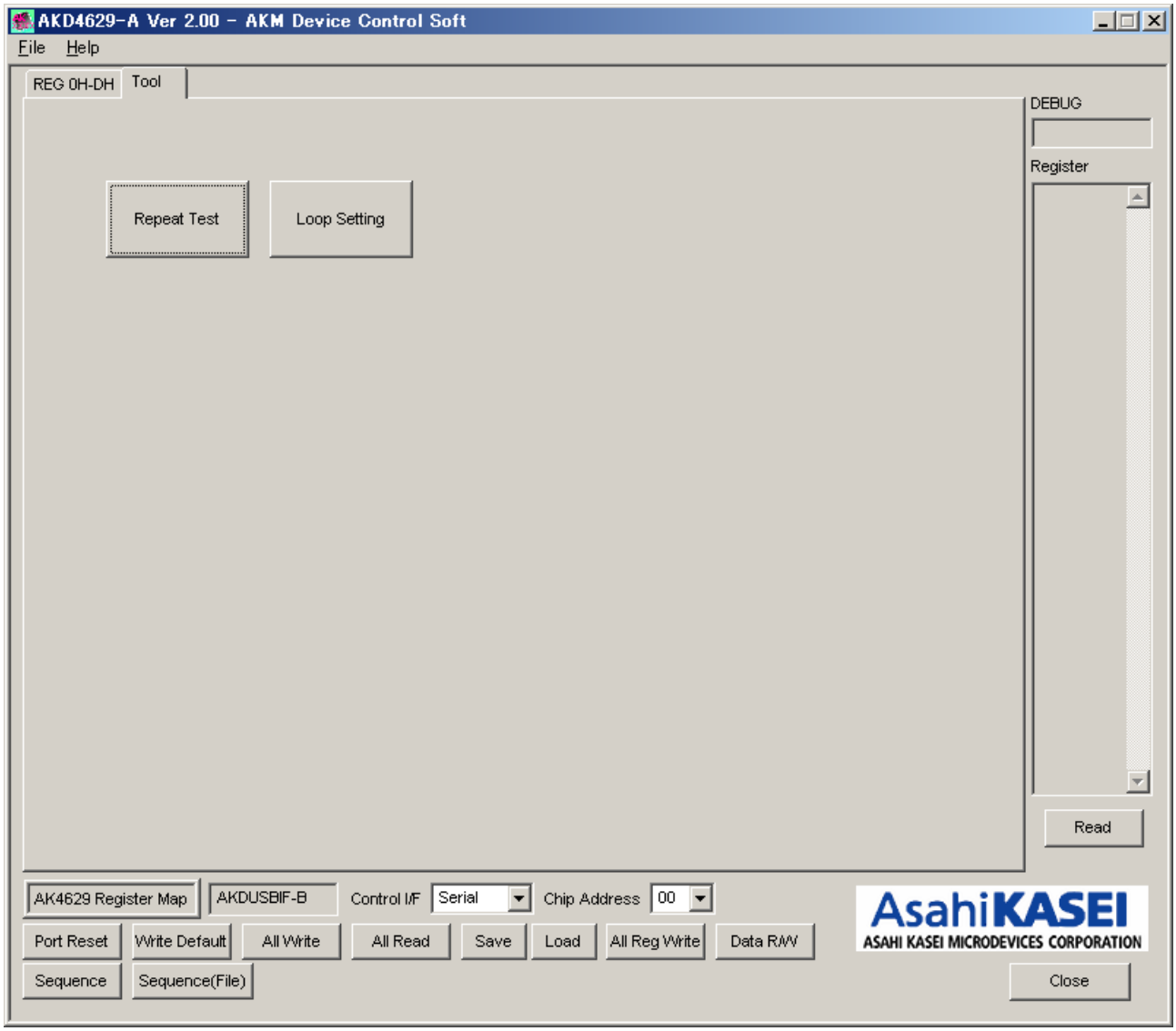
Click [Read] button located on the right of the each corresponded address to execute register reading.

After register reading, the display will be updated regarding to the register status.
Button Down indicates “H” or “1” and the bit name is in red (when read only it is in deep red).
Button Up indicates “L” or “0” and the bit name is in blue (when read only it is in gray)

Please be aware that button statuses will be changed by Read command.

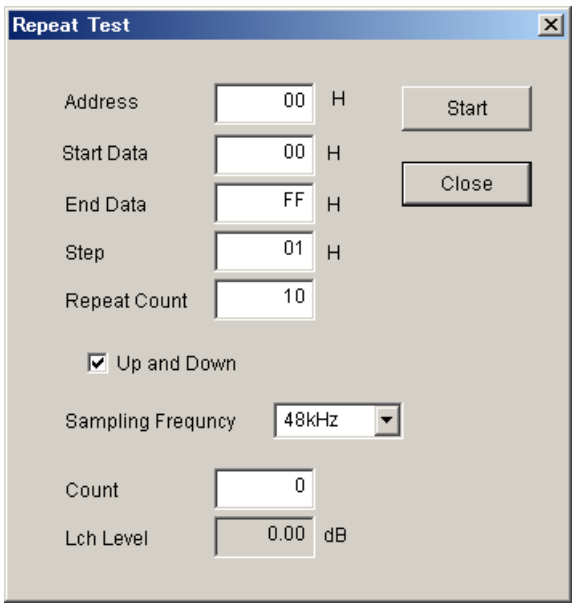
2. [Tool]: Testing Tools

This tab screen is for evaluation testing tool.
Click buttons for each testing tool.



2-1. [Repeat Test]: Repeat Test Dialog

Click [Repeat Test] button in the Test tab to open the repeat test dialog shown below.
Repeat writing test can be executed by this dialog.



[Start] Button : Starts the repeat test.
A dialog for saving a file of the test result will open when clicking this button.
Name the file.
Test will start after specifying a saving file.
[Close] Button : Closes this dialog and finishes the process.
[Address] Box : Data writing address in hexadecimal numbers.
[Start Data] Box : Start data in hexadecimal numbers.
[End Data] Box : End data in hexadecimal numbers.
[Step] Box : Data write step interval.
[Repeat Count] Box : Repeat count of the test writing.
[Up and Down] Box : Data write flow is changed as below.

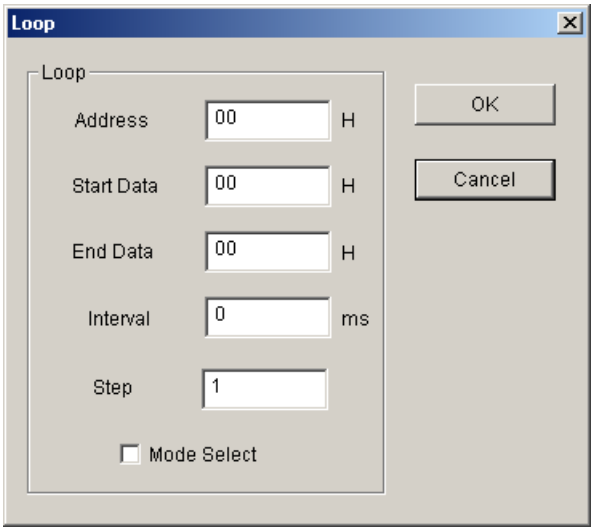
- Checked: Writes in step interval from the start data to the end data and turn back from the end data to the start data.
  [Example] Start Data = 00, End Data = 05, Step = 1, [ ]…for 1 count.
  Data flow: [00→01→02→03→04→05→05→04→03→02→01→00] x Repeat Count Number

- Not checked: Writes in step interval from the start data to the end data and finishes writing.
  [Example] Start Data = 00, End Data = 05, Step = 1, [ ]…for 1 count.
  Data flow: [00→01→02→03→04→05] x Repeat Count Number

[Sampling Frequency] Box: Selects sampling frequency 44.1kHz/48kHz
[Count] Box : Indicates the count number during a repeat test.
[Lch Level] Box : Indicates the Lch Level during a repeat test.

2-2. [Loop Setting]: Loop Dialog

Click [Loop Setting] button in the Tool tab to open the loop setting dialog as shown below.
Writing test can be executed.



[OK] Button : Starts the test.
[Cancel] Button : Closes the dialog and finishes the process.
[Address] Box : Data writing address in hexadecimal numbers.
[Start Data] Box : Start data in hexadecimal numbers.
[End Data] Box : End data in hexadecimal numbers.
[Interval] Box : Data write interval time.
[Step] Box : Data write step interval.
[Mode Select] Box : Mode select check box.

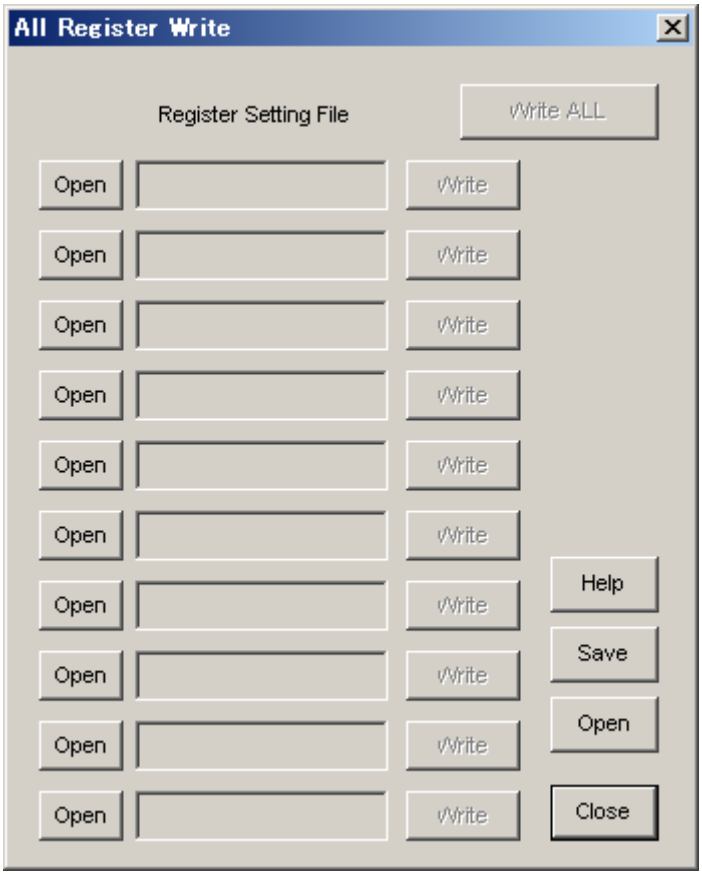
- Checked: Writes in step interval from the start data to the end data and turn back from the end data to the start data.
  [Example] Start Data = 00, End Data = 05, Step = 1
  Data flow: 00→01→02→03→04→05→05→04→03→02→01→00

- Not Checked: Writes in step interval from the start data to the end data and finishes writing.
  [Example] Start Data = 00, End Data = 05, Step = 1
  Data flow: 00→01→02→03→04→05

■ Dialog Boxes

1. [All Reg Write]: All Register Write dialog box

Click [All Reg Write] button in the main window to open register setting files.
Register setting files saved by [SAVE] button can be applied.



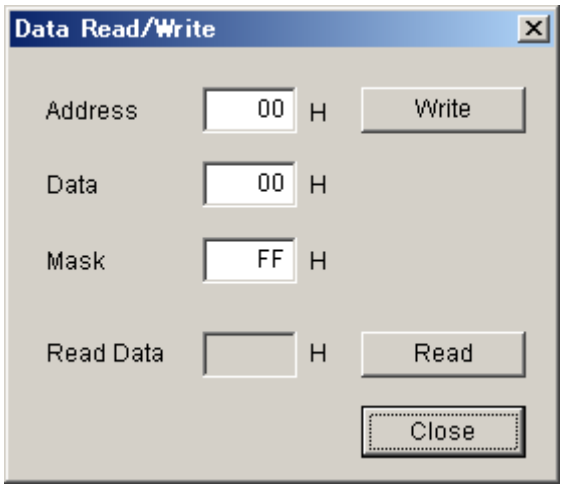
[Open (left)]: Selecting a register setting file (*.akr).
[Write]: Executing register writing.
[Write All]: Executing all register writings.
Writings are executed in descending order.

[Help]: Help window is popped up.
[Save]: Saving the register setting file assignment. The file name is "*.mar".
[Open (right)]: Opening a saved register setting file assignment "*. mar".
[Close]: Closing the dialog box and finish the process.

*Operating Suggestions
(1) Those files saved by [Save] button and opened by [Open] button on the right of the dialog "*.mar" should be stored in the same folder.
(2) When register settings are changed by [Save] button in the main window, re-read the file to reflect new register settings.

2. [Data R/W]: Data R/W Dialog Box

Click the [Data R/W] button in the main window for data read/write dialog box.
Data write is available to specified address.



Address Box: Input data address in hexadecimal numbers for data writing.
Data Box: Input data in hexadecimal numbers.
Mask Box: Input mask data in hexadecimal numbers.
This is “AND” processed input data.

[Write]: Writing to the address specified by “Address” box.

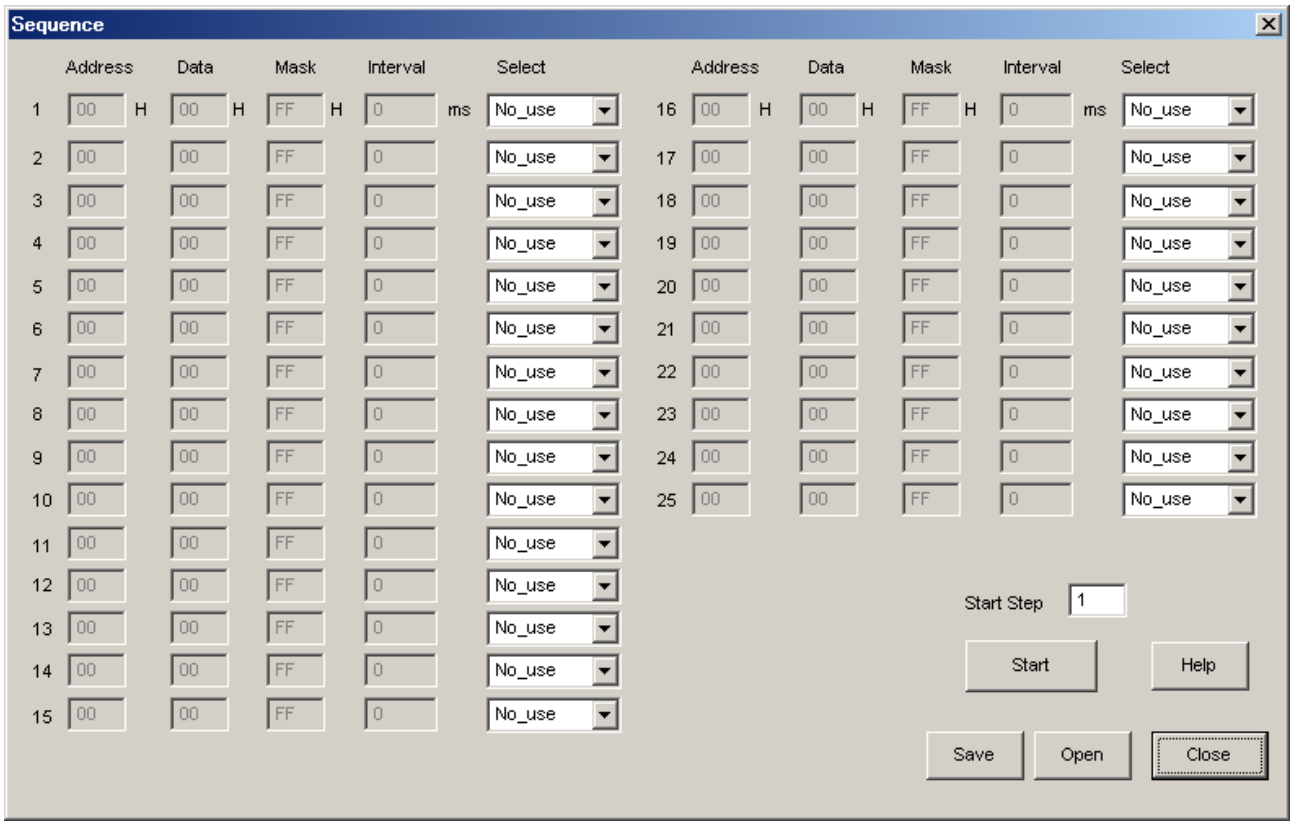
[Read]: Reading from the address specified by “Address” box.
The result will be shown in the Read Data Box in hexadecimal numbers.

[Close]: Closing the dialog box and finish the process.
Data writing can be cancelled by this button instead of [Write] button.

*The register map will be updated after executing [Write] or [Read] commands.

3. [Sequence]: Sequence Dialog Box

Click [Sequence] button to open register sequence setting dialog box.
Register sequence can be set in this dialog box.



Sequence Setting

Set register sequence by following process bellow.

(1)Select a command

Use [Select] pull-down box to choose commands.
Corresponding boxes will be valid.

< Select Pull-down menu >

- · No_use: Not using this address
- · Register: Register writing
- · Reg(Mask): Register writing (Masked)
- · Interval: Taking an interval
- · Stop: Pausing the sequence
- · End: Finishing the sequence

(1) Input sequence

[Address]: Data address
[Data]: Writing data
[Mask]: Mask

[Data] box data is ANDed with [Mask] box data. This is the actual writing data.
When Mask = 0x00, current setting is hold.

When Mask = 0xFF, the 8bit data which is set in the [Data] box is written.

When Mask =0x0F, lower 4bit data which is set in the [Data] box is written.
Upper 4bit is hold to current setting.

[Interval]: Interval time

Valid boxes for each process command are shown bellow.

· No_use: None
· Register: [Address], [Data], [Interval]
· Reg(Mask): [Address], [Data], [Mask], [Interval]
· Interval: [Interval]
· Stop: None
· End: None

Control Buttons

The function of Control Button is shown bellow.

[Start]: Executing the sequence

[Help]: Opening a help window
[Save]: Saving sequence settings as a file. The file name is "*.aks".
[Open]: Opening a sequence setting file "*.aks".
[Close]: Closing the dialog box and finish the process.

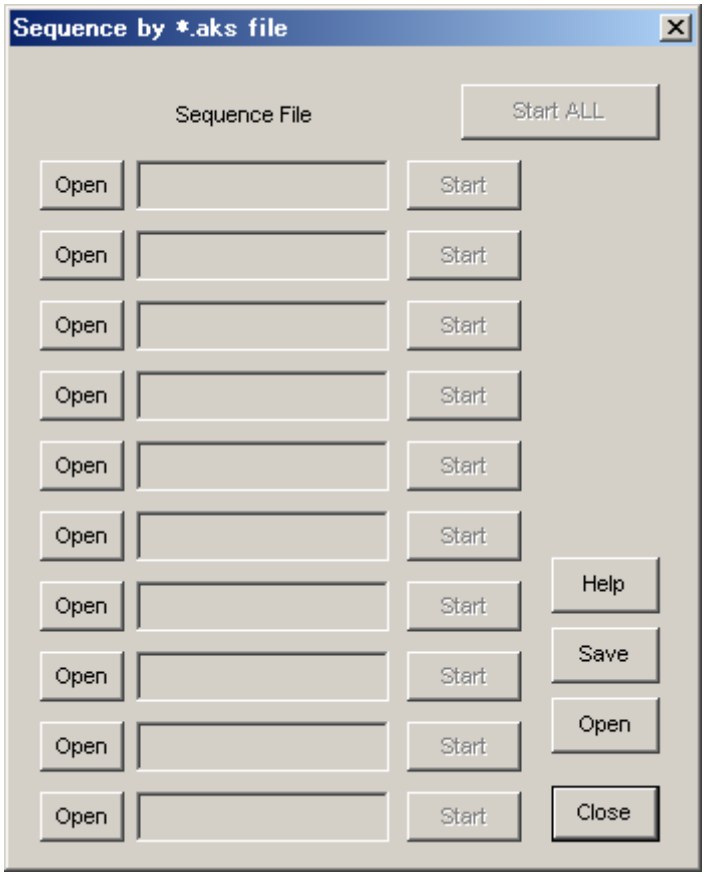
Stop of the sequence

When "Stop" is selected in the sequence, processing is paused and it starts again when [Start] button is clicked. Restarting step number is shown in the "Start Step" box. When finishing the process until the end of sequence, "Start Step" will return to "1".

The sequence can be started from any step by writing the step number to the "Start Step" box.
Write "1" to the "Start Step" box and click [Start] button, when restarting the process from the beginning.

4. [Sequence(File)]: Sequence Setting File Dialog Box

Click [Sequence(File)] button to open sequence setting file dialog box.
Those files saved in the "Sequence setting dialog" can be applied in this dialog.



[Open (left)]: Opening a sequence setting file (*.aks).
[Start]: Executing the sequence setting.
[Start All]: Executing all sequence settings.
Sequences are executed in descending order.

[Help]: Pop up the help window.
[Save]: Saving sequence setting file assignment. The file name is "*.mas".
[Open(right)]: Opening a saved sequence setting file assignment "*. mas".
[Close]: Closing the dialog box and finish the process.

*Operating Suggestions

(1) Those files saved by [Save] button and opened by [Open] button on the right of the dialog "*.mas" should be stored in the same folder.
(2) When "Stop" is selected in the sequence the process will be paused and a pop-up message will appear. Click "OK" to continue the process.

MEASUREMENT RESULTS

1) ADC part

[Measurement condition]

- Measurement unit : Audio Precision, System two, Cascade
- MCLK : 512fs at 48kHz, 256fs at 96kHz
- BICK : 64fs
- fs : 48kHz, 96kHz
- BW : 20Hz~20kHz at fs=48kHz, 20Hz~40kHz at 96kHz
- Bit : 24bit
- Power Supply : AVDD=DVDD= TVDD=5V
- Interface : DIT (AK4118)
- Temperature : Room

a) Single-ended Inputs

fs=48kHz

Parameter	Input signal	Measurement filter	LIN1	RIN1	Units
S/(N+D)	1kHz, -0.5dBFS	20kHz LPF	95.7	96.3	dB
DR	1kHz, -60dBFS	20kHz LPF+A-weighted	102.7	102.6	dB
S/N	No signal	20kHz LPF+A-weighted	103.0	103.0	dB

fs=96kHz

Parameter	Input signal	Measurement filter	LIN1	RIN1	Units
S/(N+D)	1kHz, -0.5dBFS	40kHz LPF	91.6	92.3	dB
DR	1kHz, -60dBFS	40kHz LPF+A-weighted	105.0	105.0	dB
S/N	No signal	40kHz LPF+A-weighted	105.2	105.2	dB

b) Differential Inputs

fs=48kHz

Parameter	Input signal	Measurement filter	LIN1	RIN1	Units
S/(N+D)	1kHz, -0.5dBFS	20kHz LPF	96.9	96.7	dB
DR	1kHz, -60dBFS	20kHz LPF+A-weighted	103.2	103.1	dB
S/N	No signal	20kHz LPF+A-weighted	103.5	103.5	dB

fs=96kHz

Parameter	Input signal	Measurement filter	LIN1	RIN1	Units
S/(N+D)	1kHz, -0.5dBFS	40kHz LPF	93.5	94.5	dB
DR	1kHz, -60dBFS	40kHz LPF+A-weighted	105.9	105.7	dB
S/N	No signal	40kHz LPF+A-weighted	106.2	106.2	dB

2) DAC part

[Measurement condition]

- Measurement unit : Audio Precision, System two, Cascade
- MCLK : 512fs at 48kHz, 256fs at 96kHz, 128fs at 192kHz
- BICK : 64fs
- fs : 48kHz, 96kHz, 192kHz
- BW : 20Hz~20kHz at fs=48kHz, 20Hz~40kHz at 96kHz, 20Hz~40kHz at 192kHz
- Bit : 24bit
- Power Supply : AVDD=DVDD= TVDD=5V
- Interface : DIR (AK4118)
- Temperature : Room

fs=48kHz

Parameter	Input signal	Measurement filter	LOUT1	ROUT1	Units
S/(N+D)	1kHz, 0dBFS	20kHz Brick-wall LPF	100.5	97.0	dB
DR	1kHz, -60dBFS	20kHz Brick-wall LPF A-weighted	105.5	105.5	dB
S/N	No signal	20kHz Brick-wall LPF A-weighted	105.5	105.6	dB

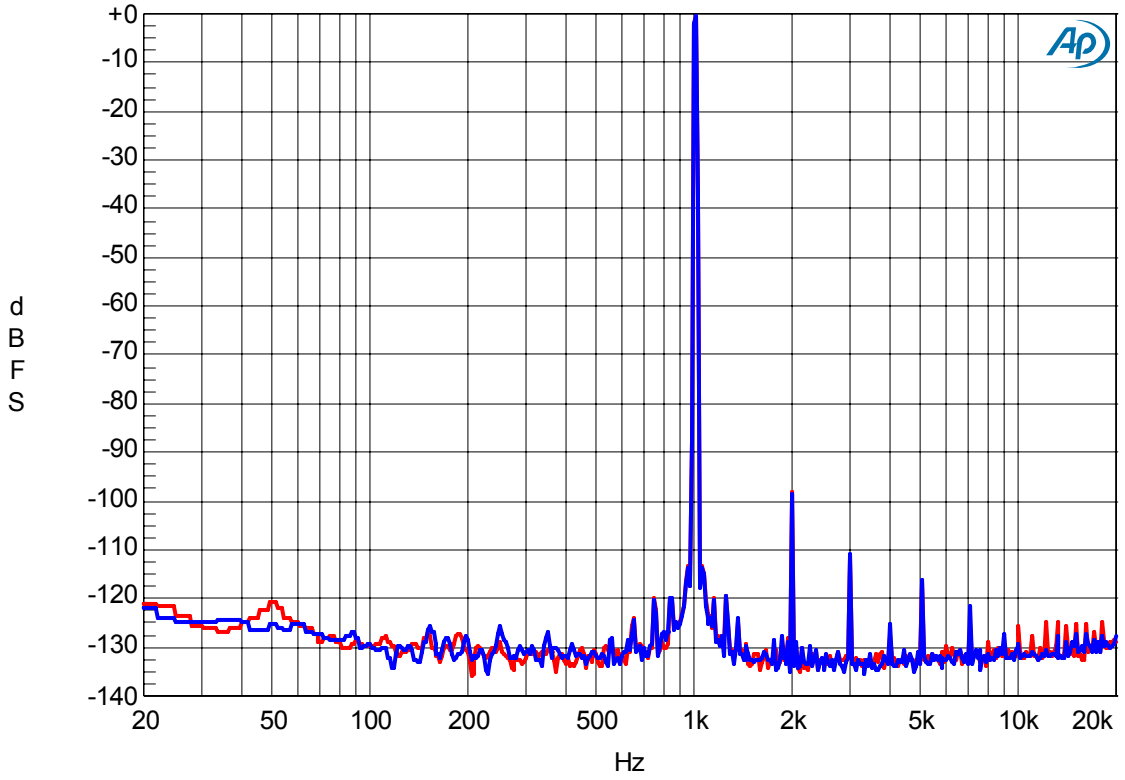
fs=96kHz

Parameter	Input signal	Measurement filter	LOUT1	ROUT1	Units
S/(N+D)	1kHz, 0dBFS	40kHz Brick-wall LPF	98.6	95.9	dB
DR	1kHz, -60dBFS	40kHz Brick-wall LPF A-weighted	105.3	105.4	dB
S/N	No signal	40kHz Brick-wall LPF A-weighted	105.3	105.4	dB

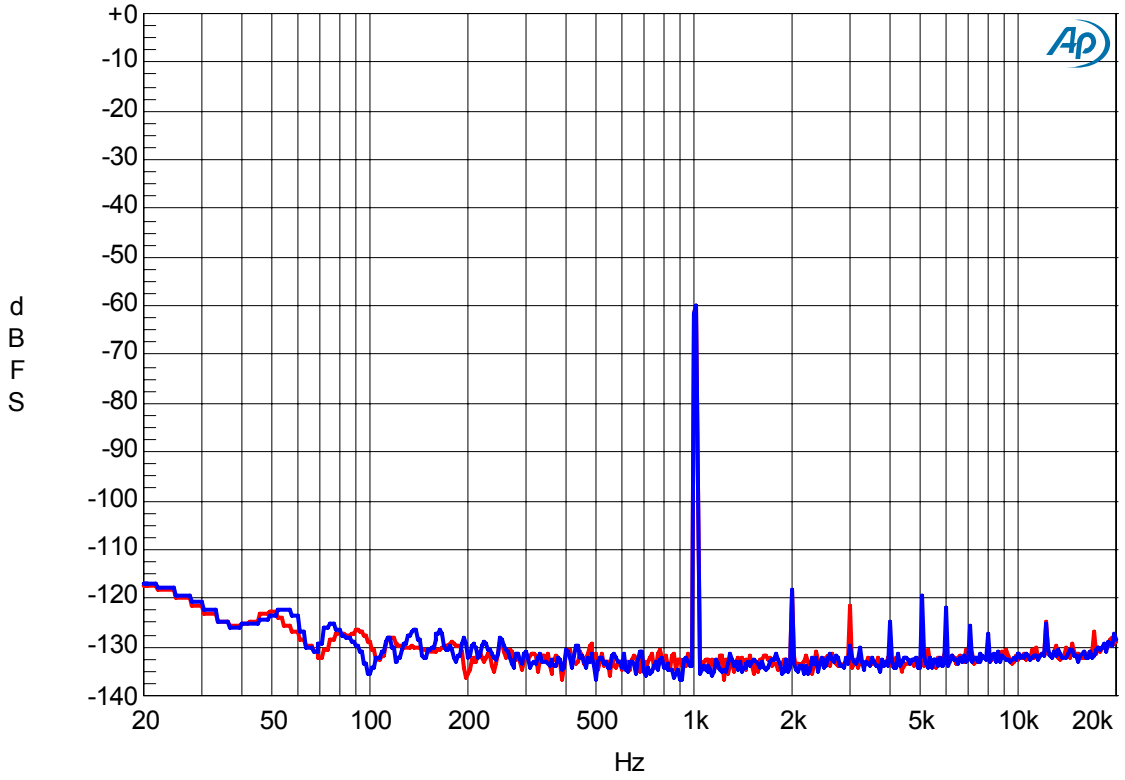
fs=192kHz

Parameter	Input signal	Measurement filter	LOUT1	ROUT1	Units
S/(N+D)	1kHz, 0dBFS	40kHz Brick-wall LPF	97.6	95.8	dB
DR	1kHz, -60dBFS	40kHz Brick-wall LPF A-weighted	105.3	105.4	dB
S/N	No signal	40kHz Brick-wall LPF A-weighted	105.4	105.5	dB

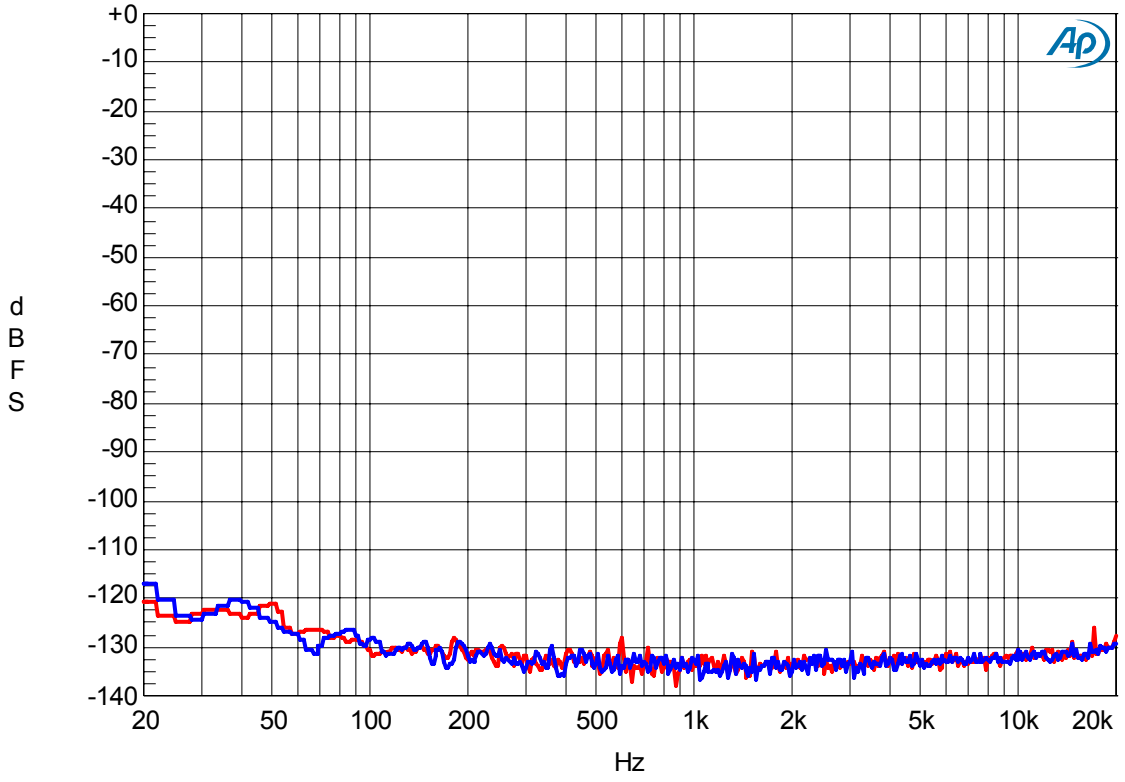
1.1.1 ADC (fs=48kHz, Single-ended Inputs)



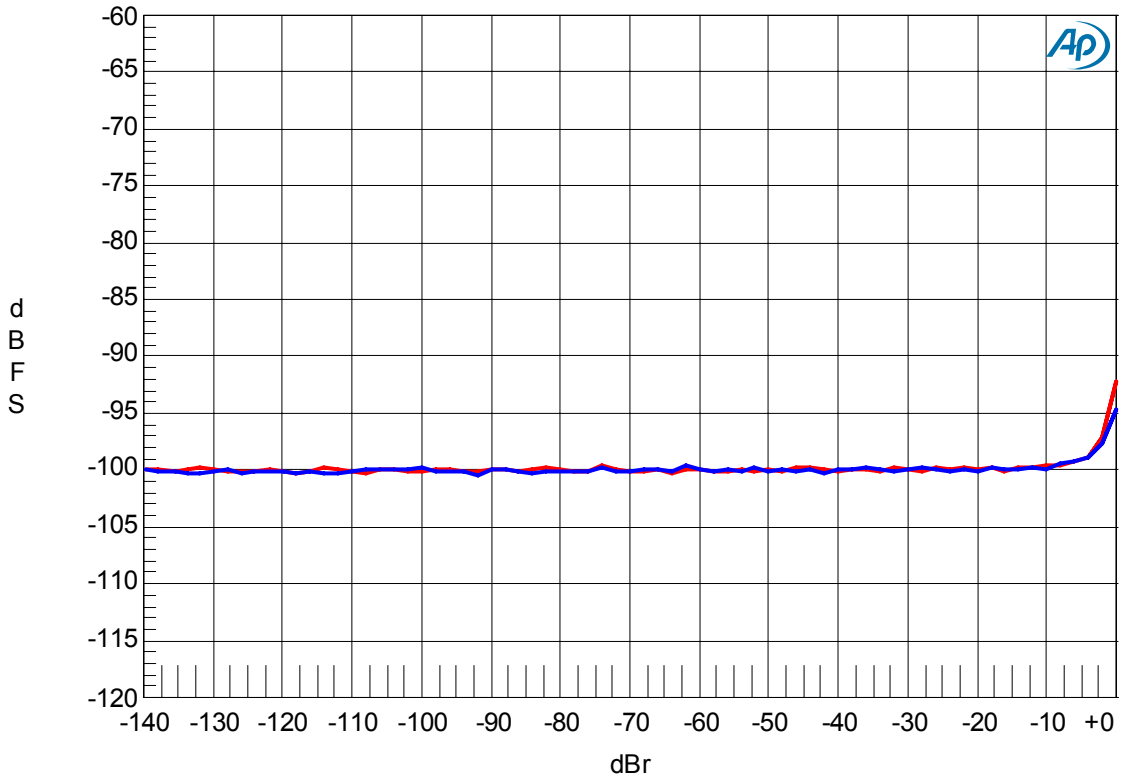
FFT (Input=-0.5dBr, fin=1kHz)



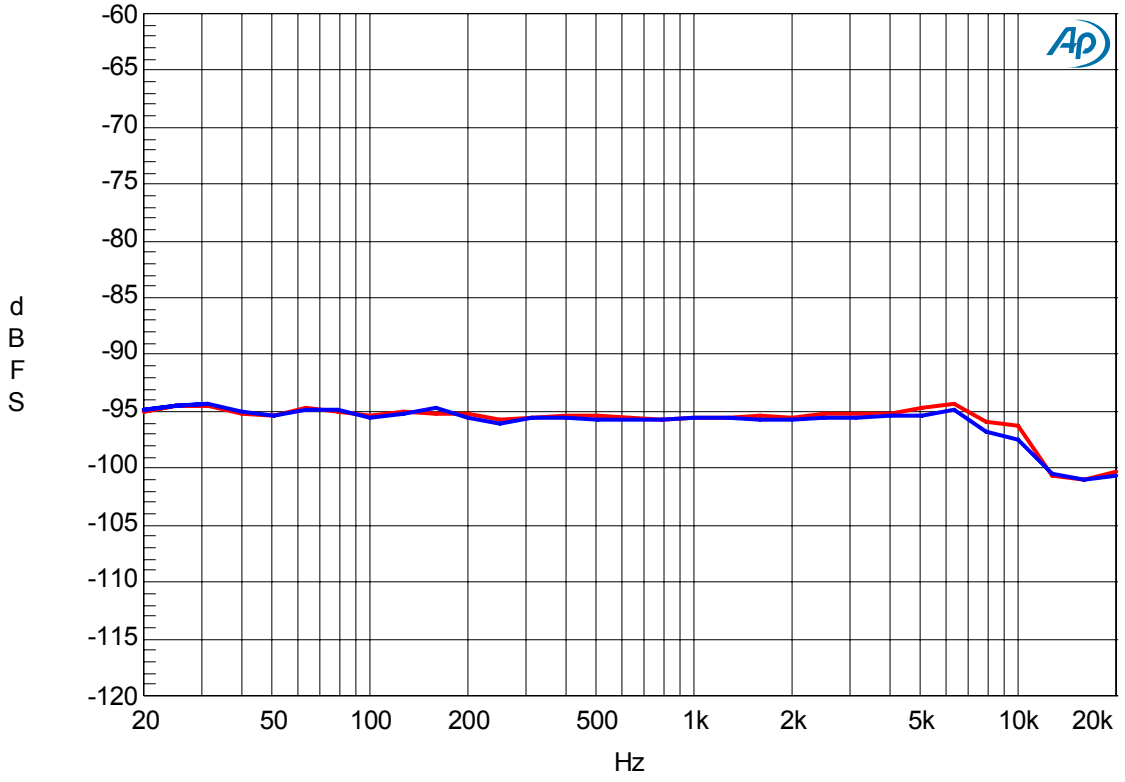
FFT (Input=-60dBr, fin=1kHz)



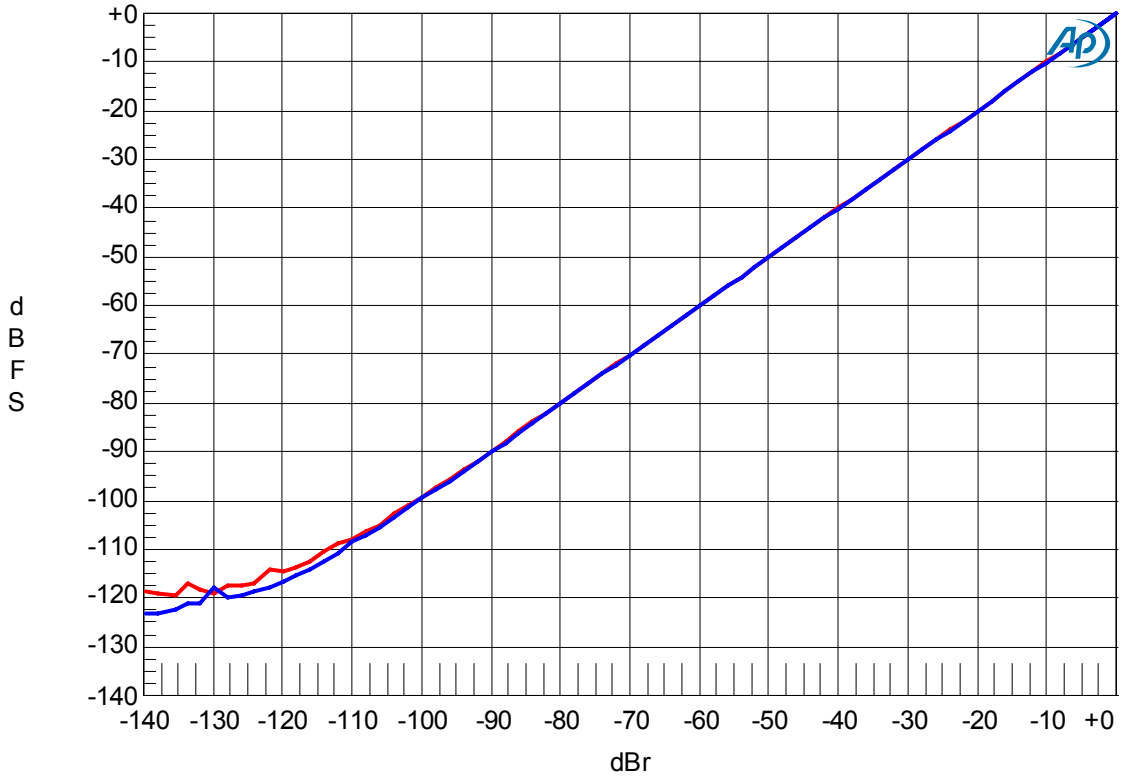
FFT (noise floor)



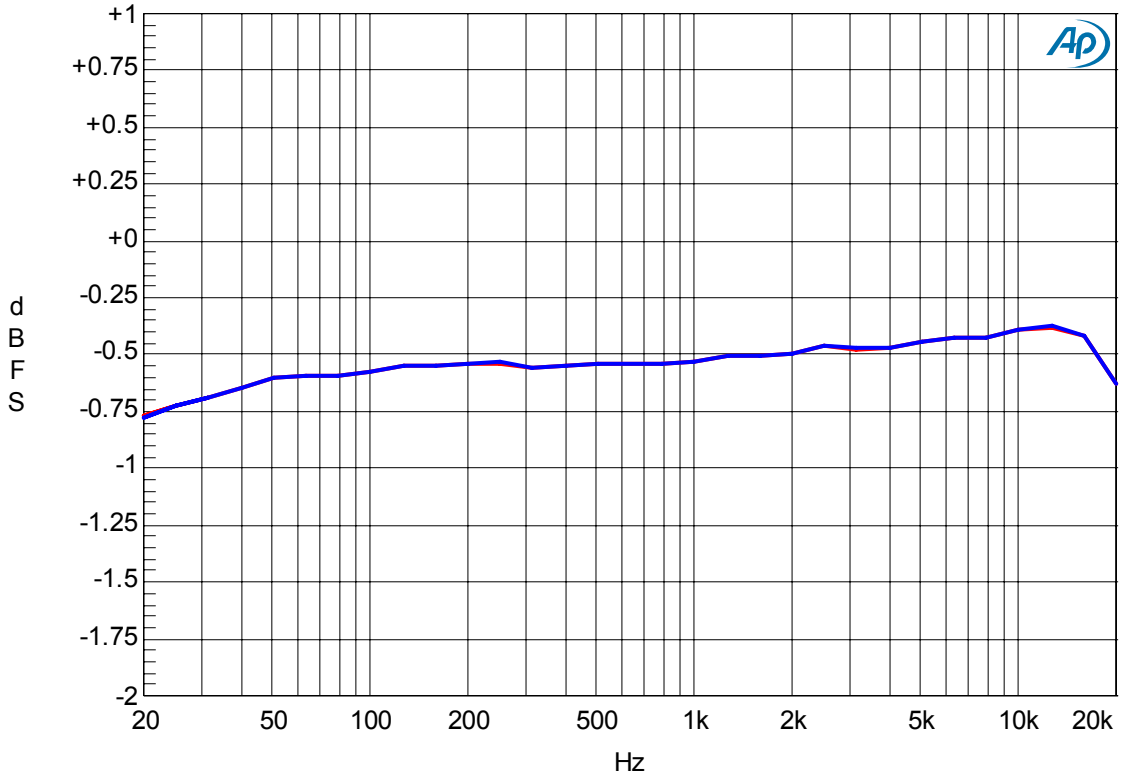
THD + N vs. Input Level (fin=1kHz)



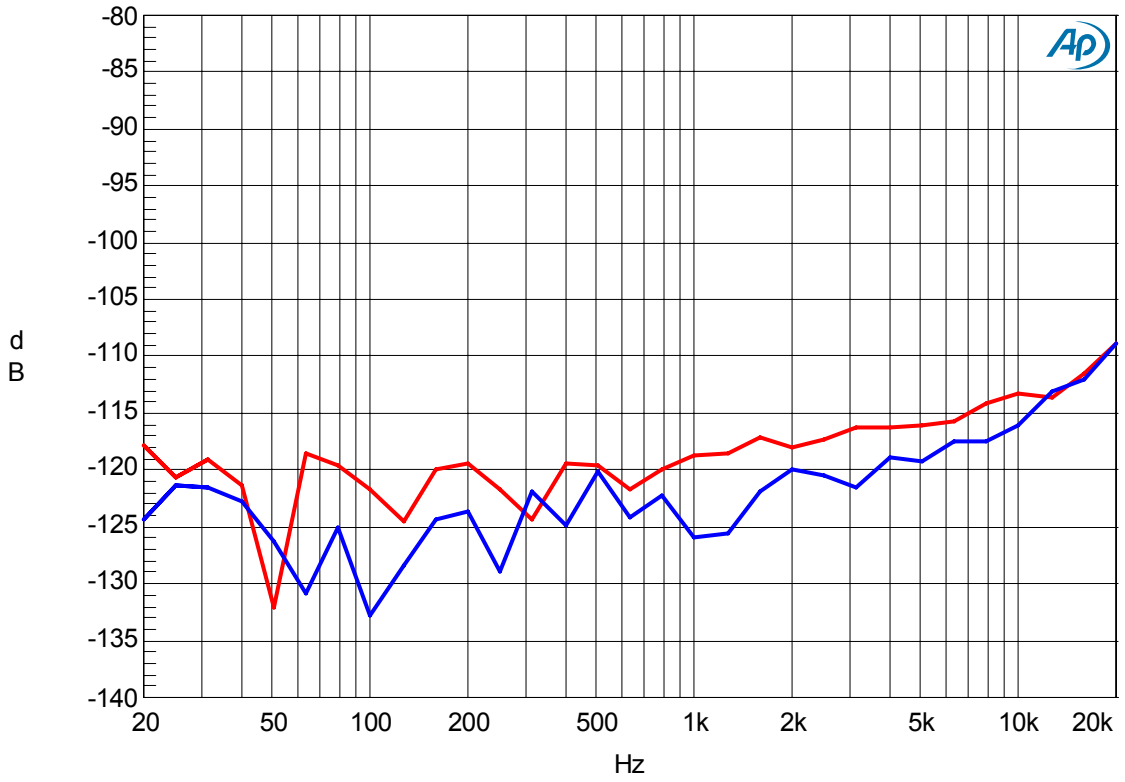
THD + N vs. Input Frequency (Input=-0.5dBr)



Linearity (fin=1kHz)

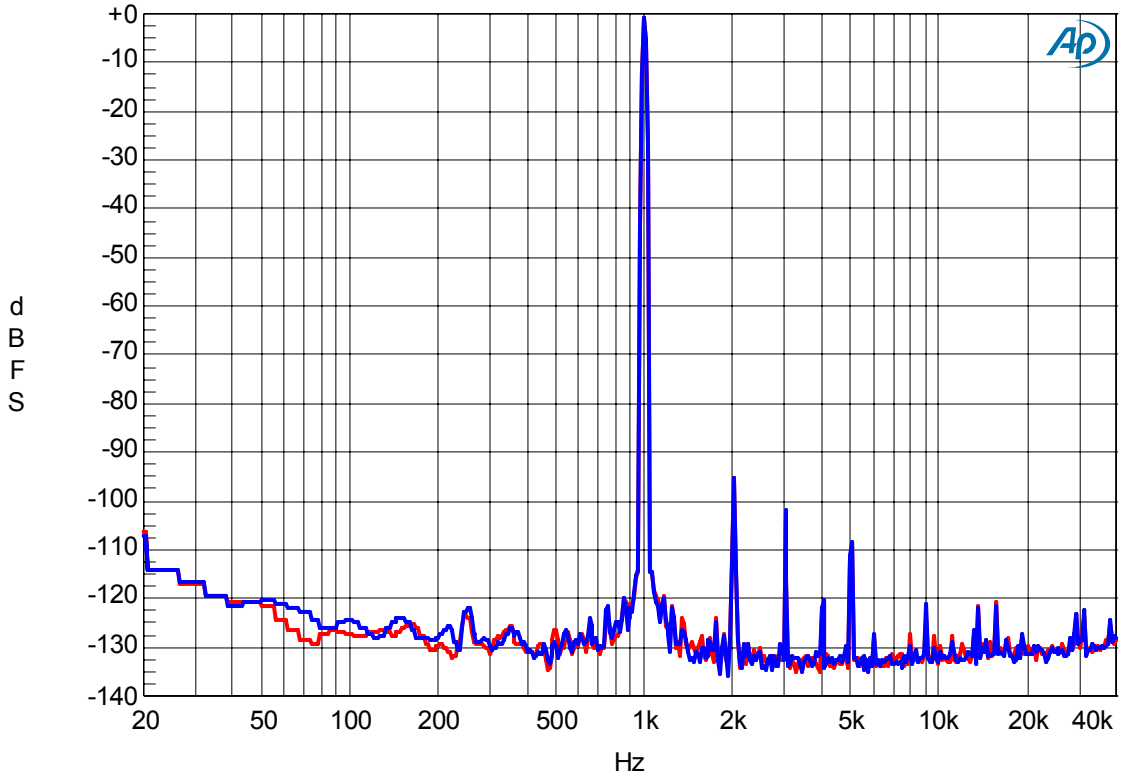


Frequency Response (Input Level=-0.5dBr)

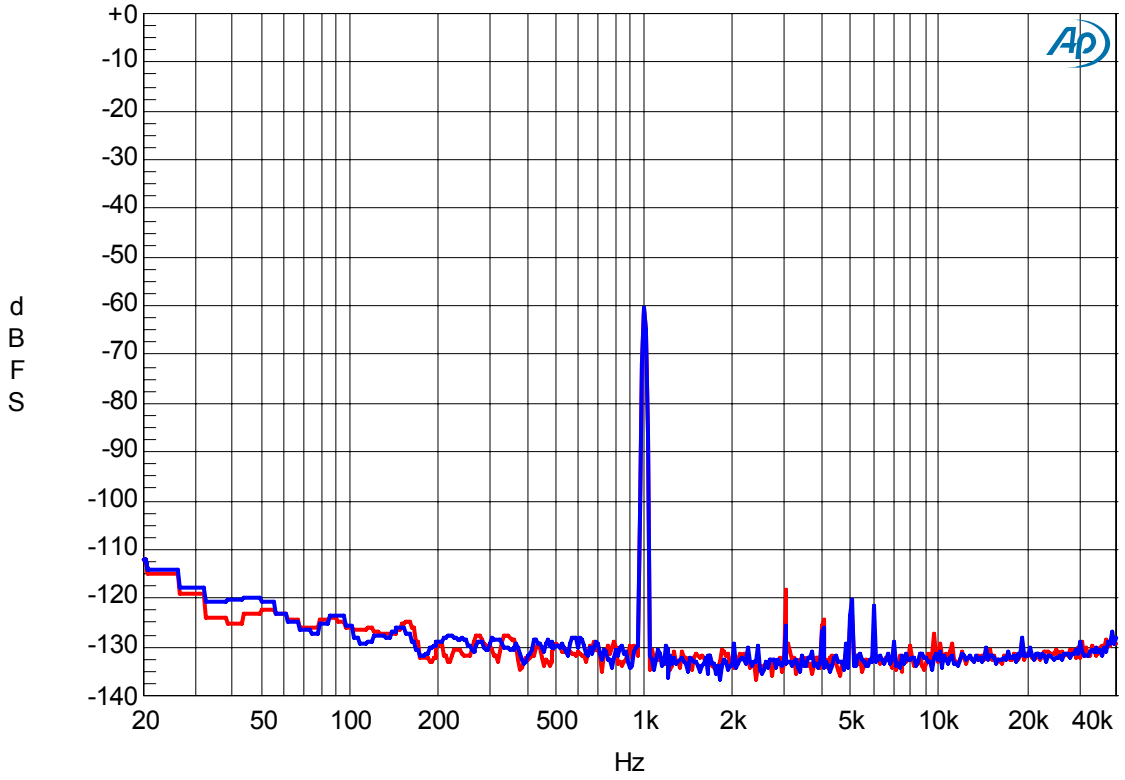


Crosstalk (Input Level=-0.5dBr)

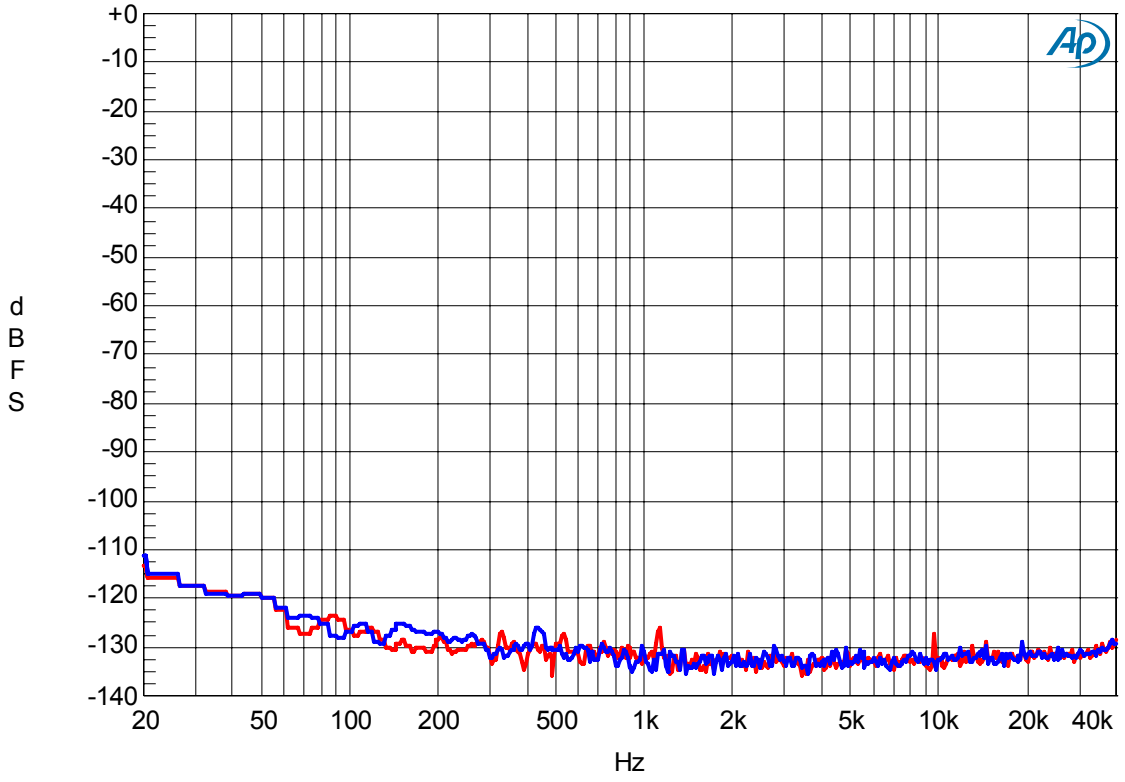
1.1.2 ADC (fs=96kHz, Single-ended Inputs)



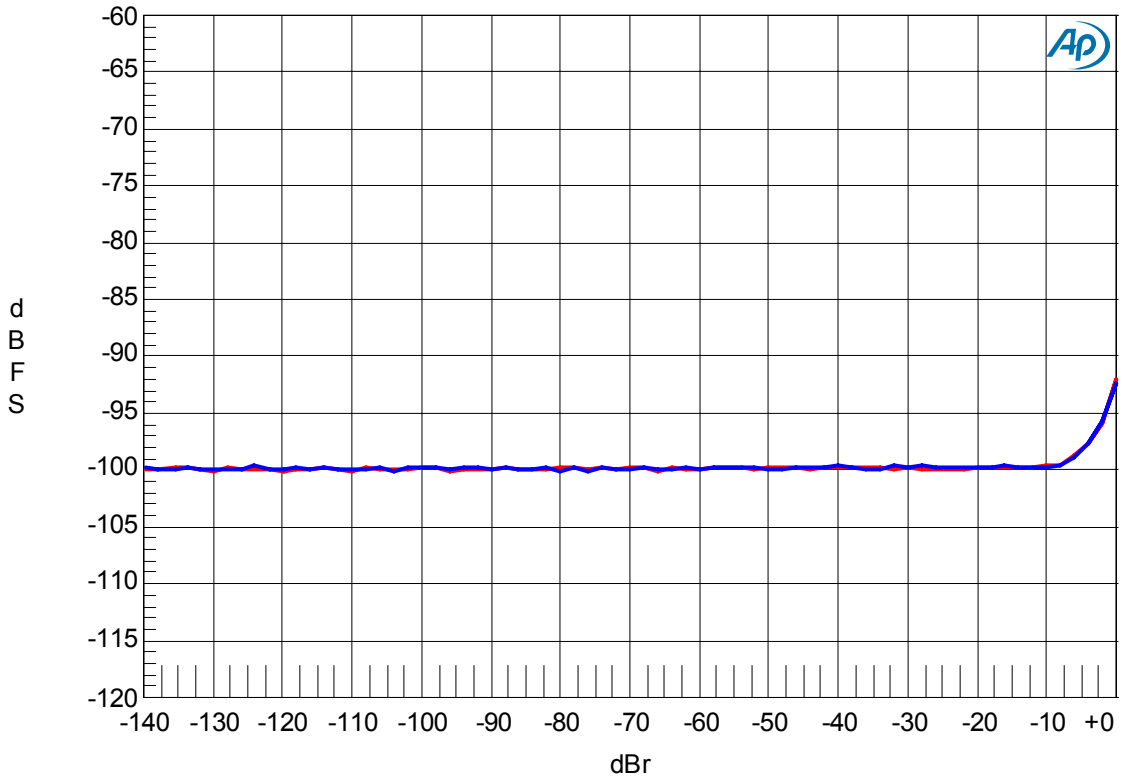
FFT (Input=-0.5dBr, fin=1kHz)



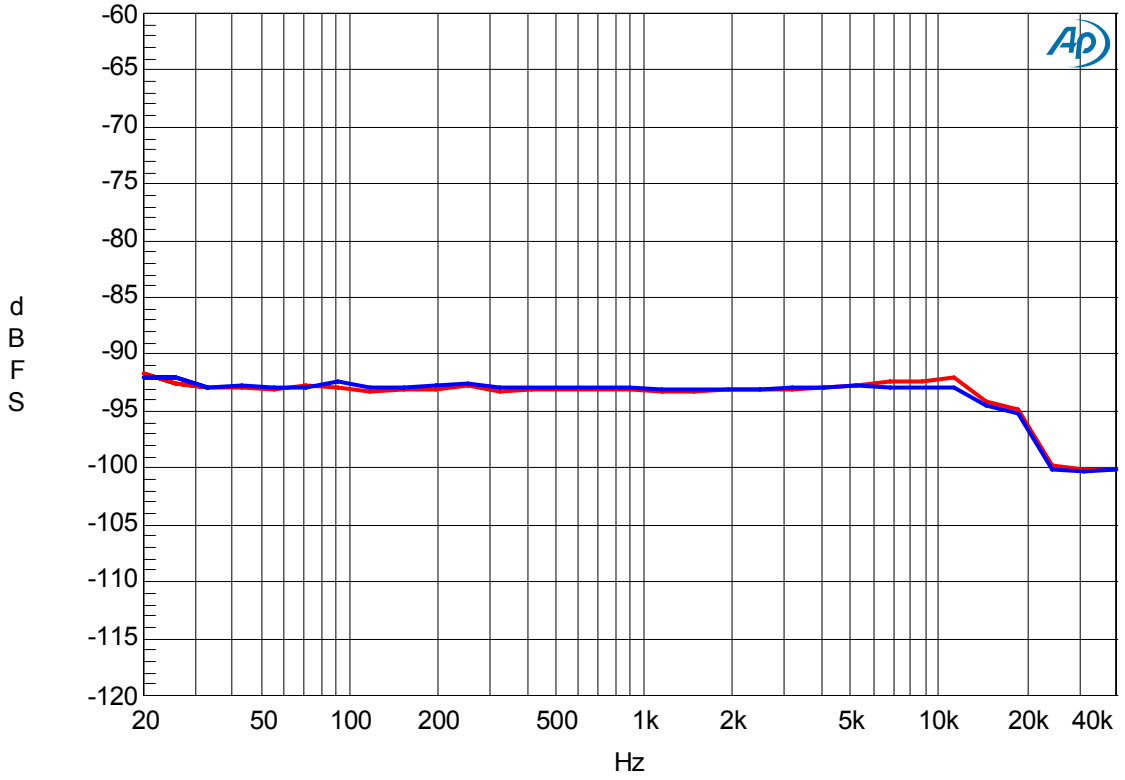
FFT (Input=-60dBr, fin=1kHz)



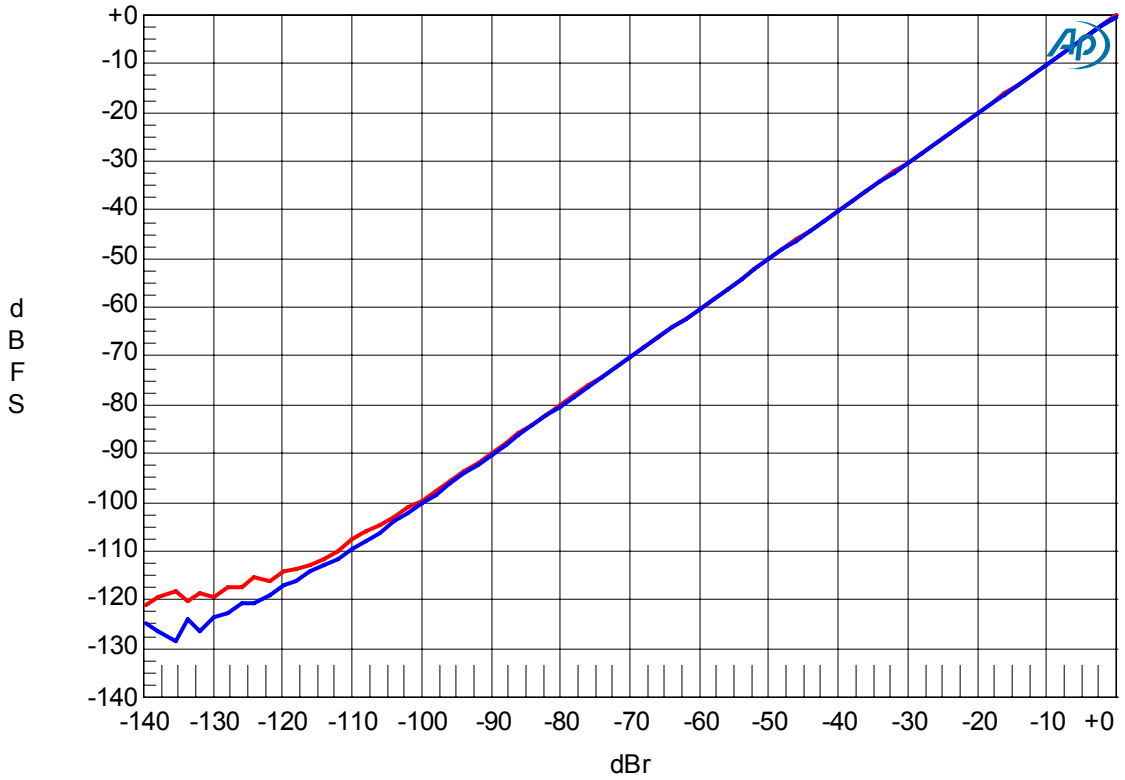
FFT (Noise floor)



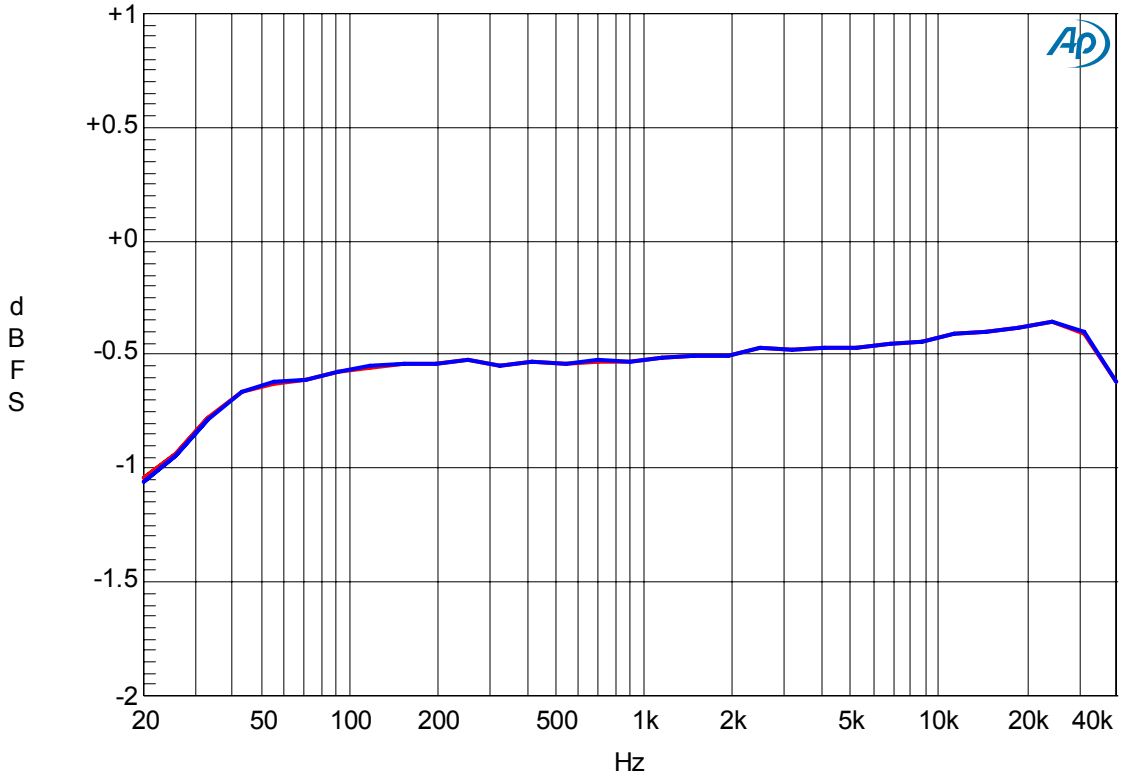
THD + N vs. Input Level (fin=1kHz)



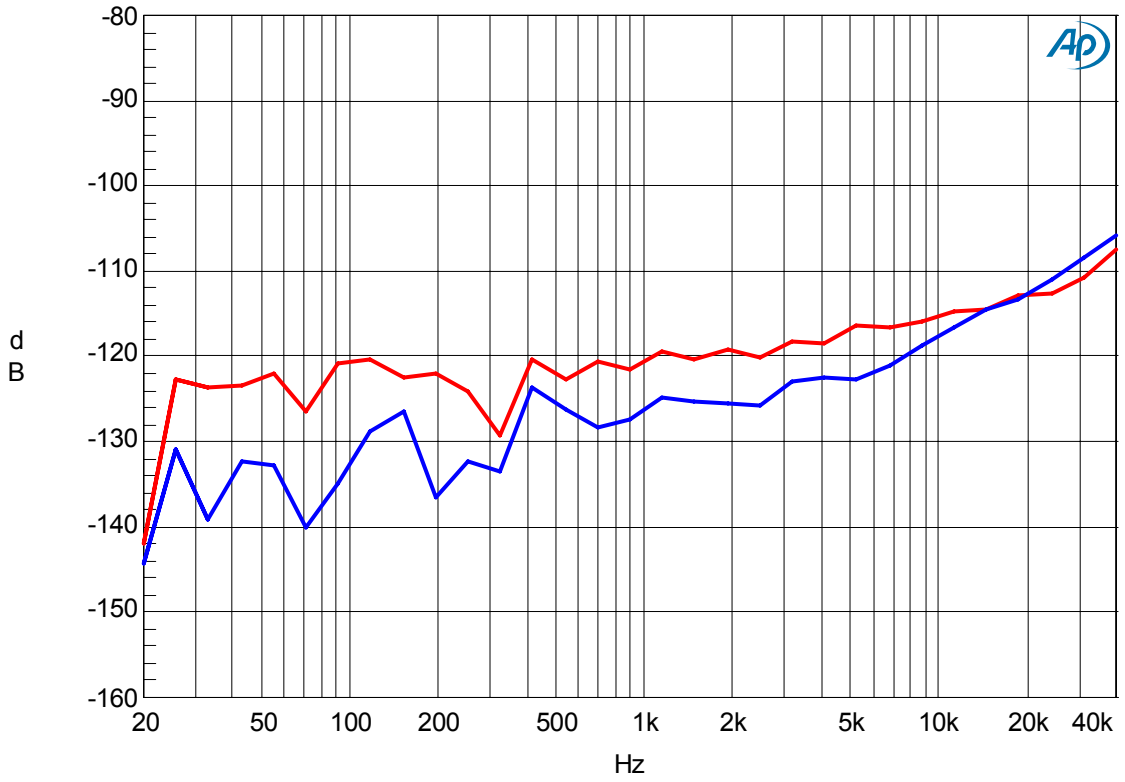
THD + N vs. Input Frequency (Input Level=-0.5dBr)



Linearity (fin=1kHz)

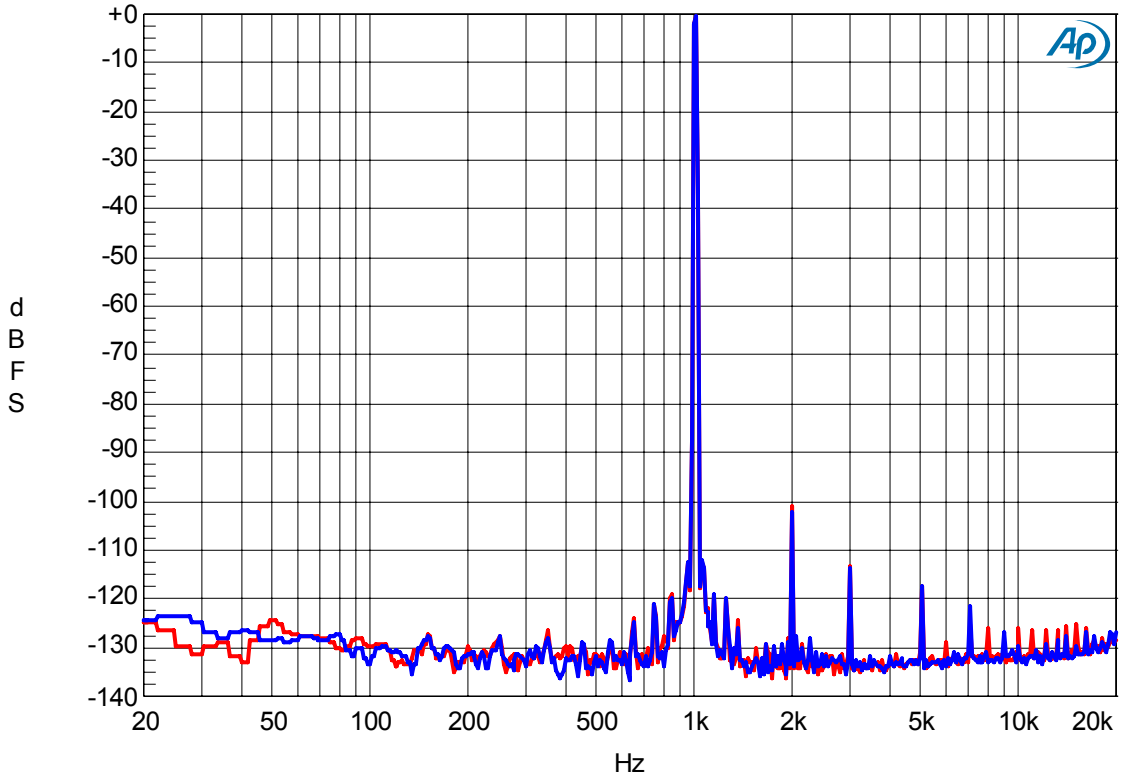


Frequency Response (Input Level=-0.5dBr)

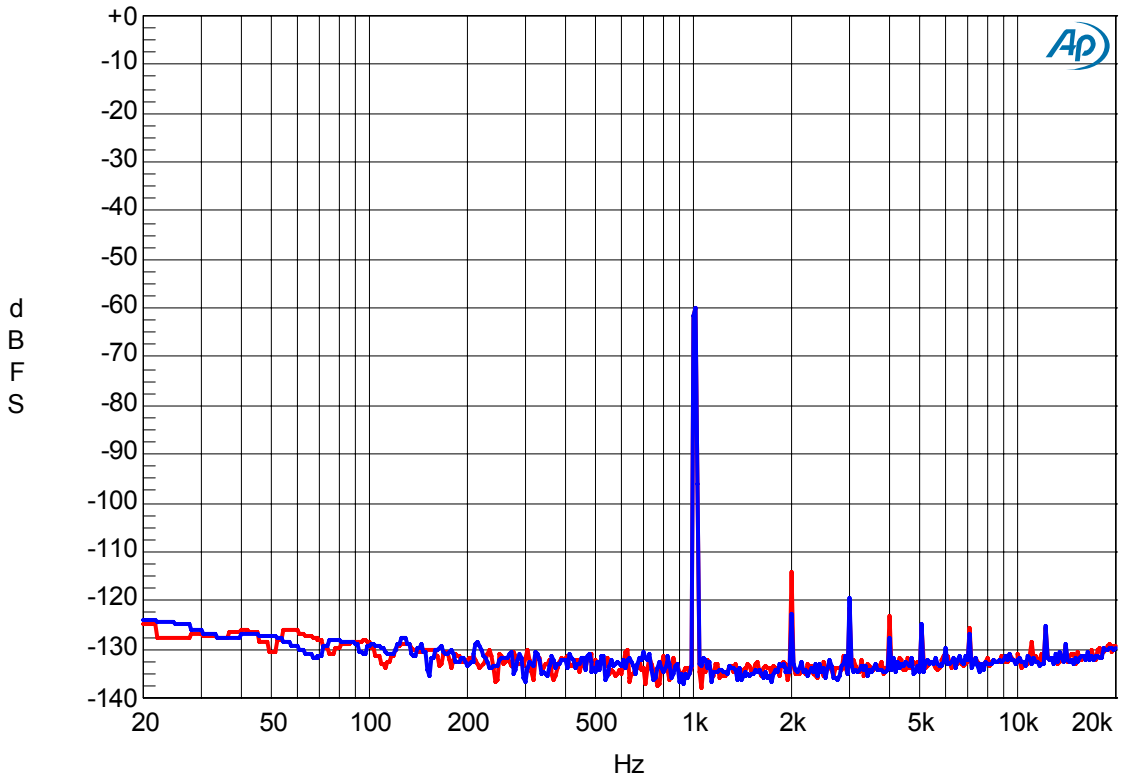


Crosstalk

1.2.1 ADC (fs=48kHz, Differential Inputs)

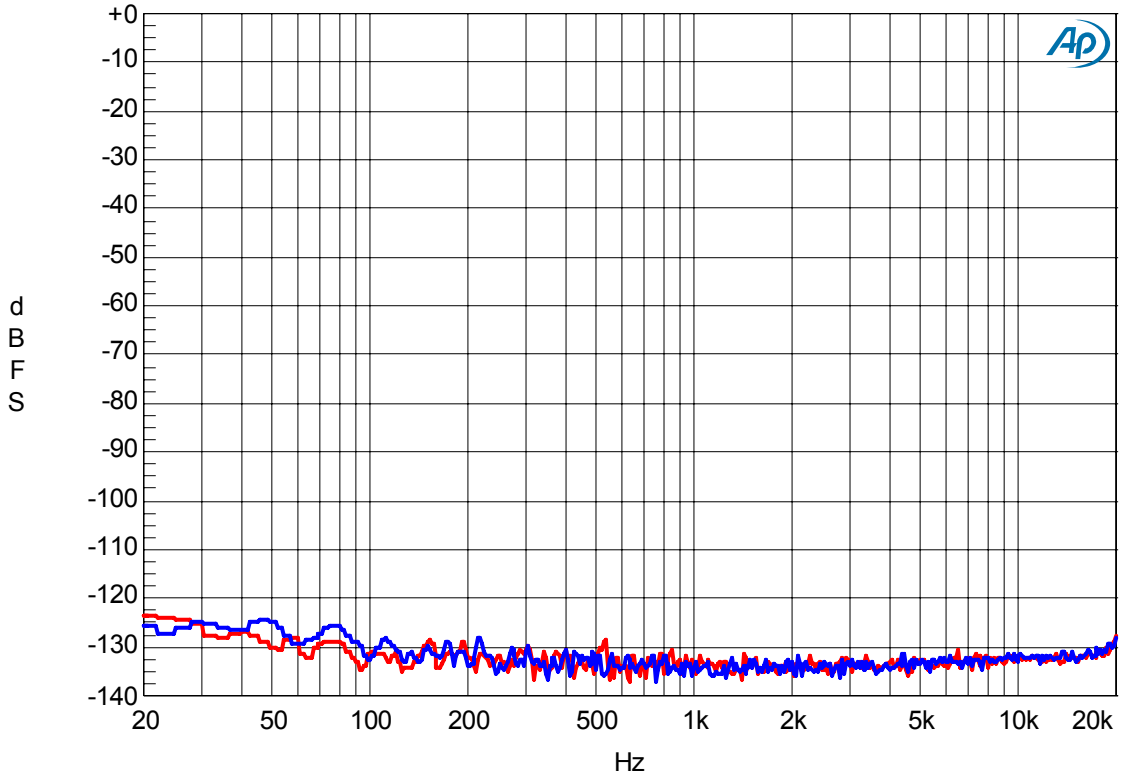


FFT (Input=-0.5dBr, fin=1kHz)

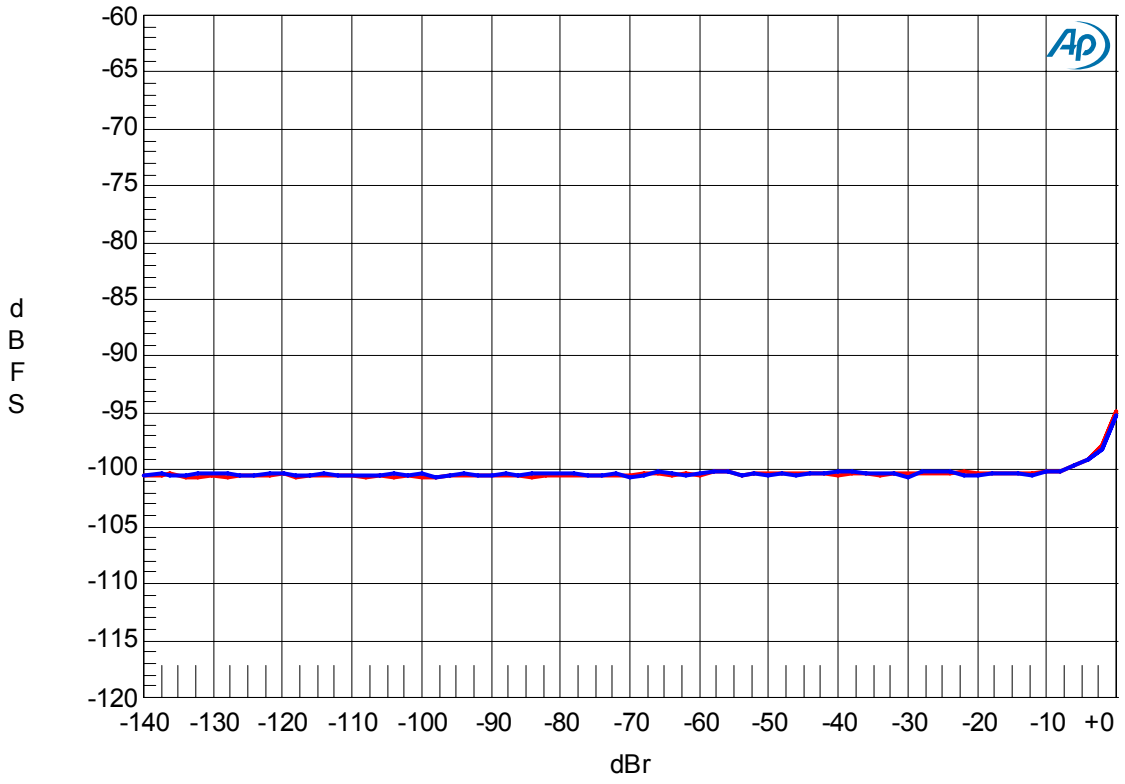


FFT

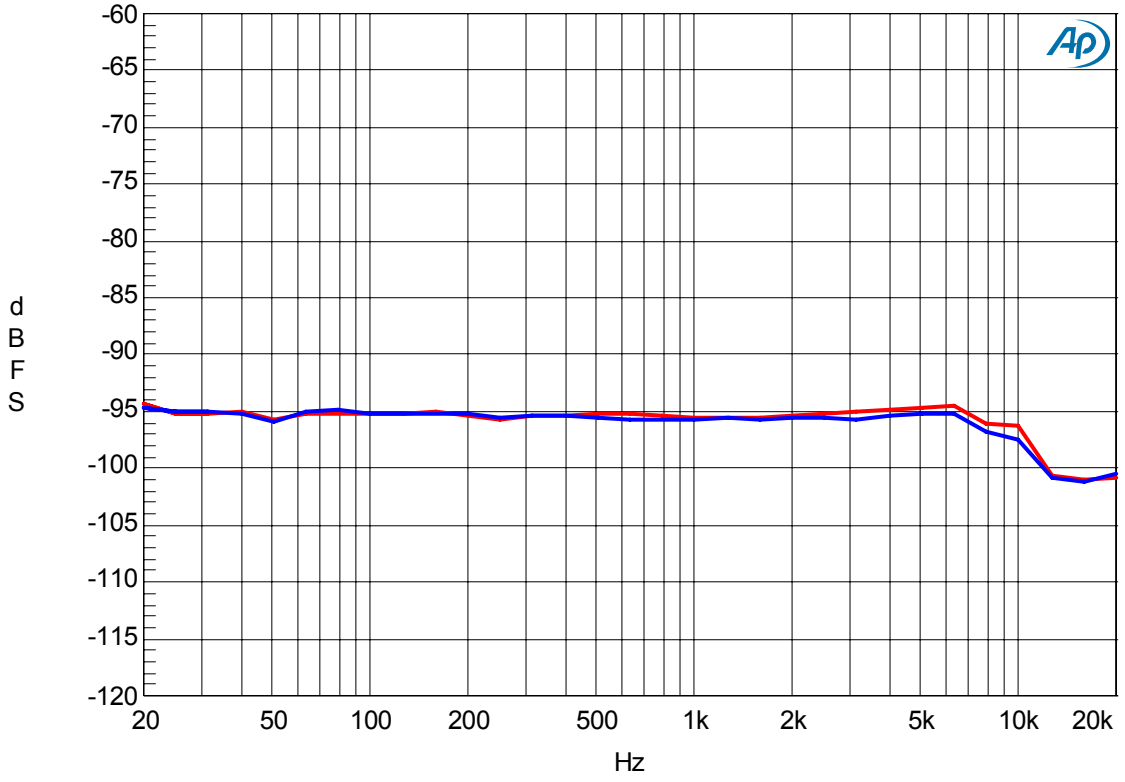
(Input=-60dBr, fin=1kHz)



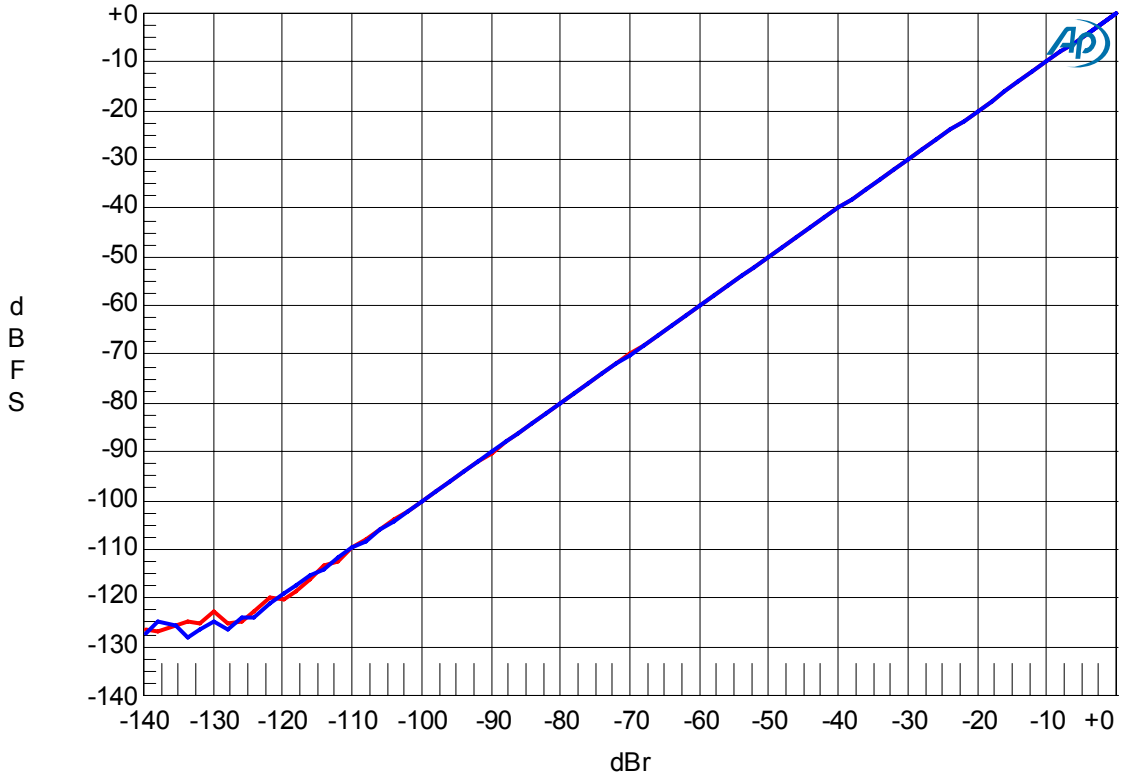
FFT (noise floor)



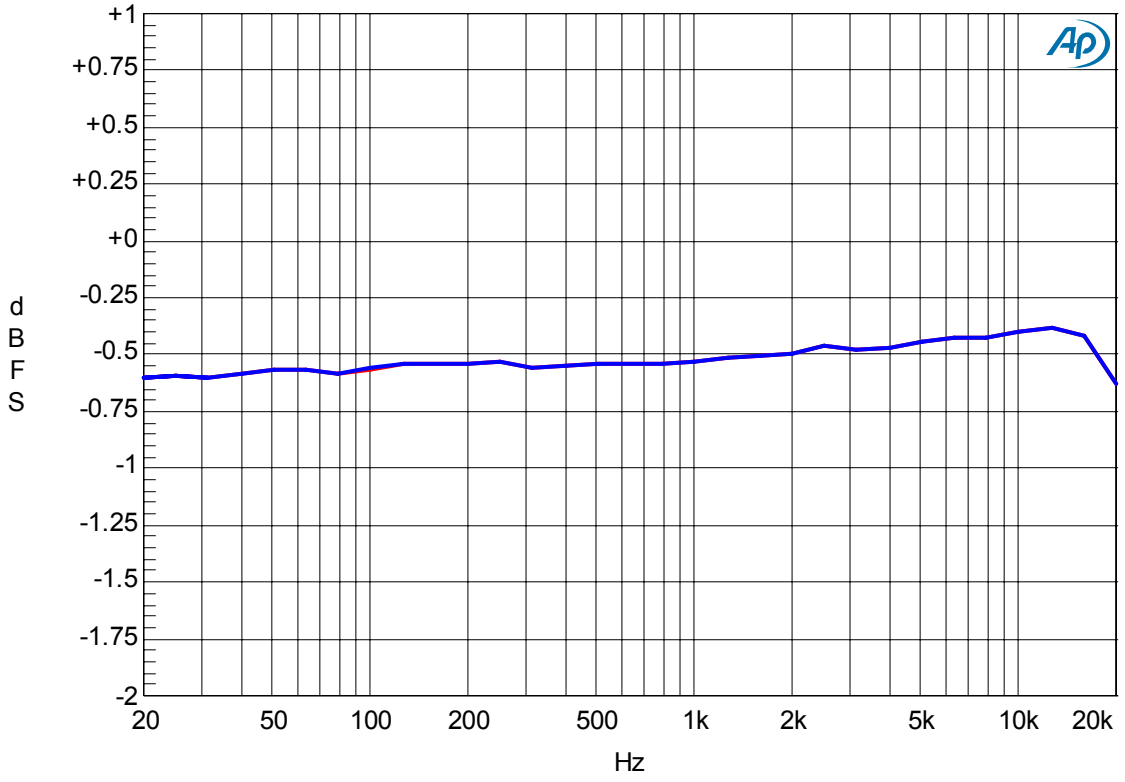
THD + N vs. Input Level (fin=1kHz)



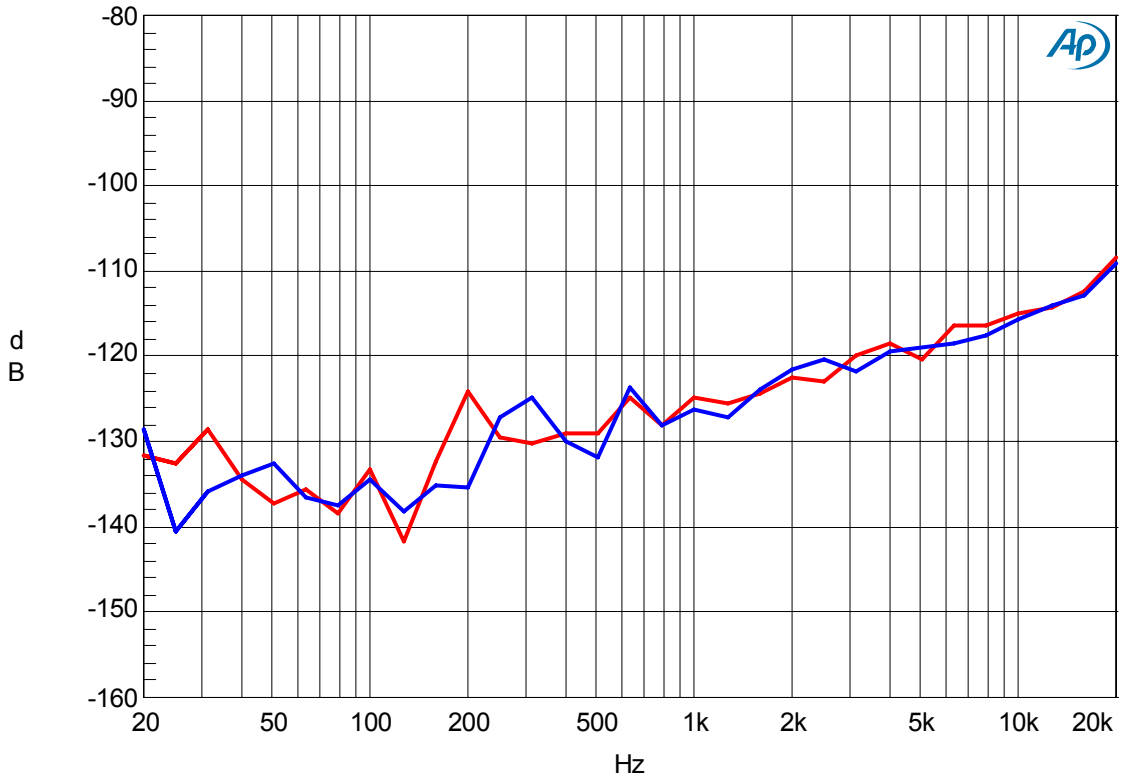
THD + N vs. Input Frequency (Input=-0.5dBr)



Linearity (fin=1kHz)

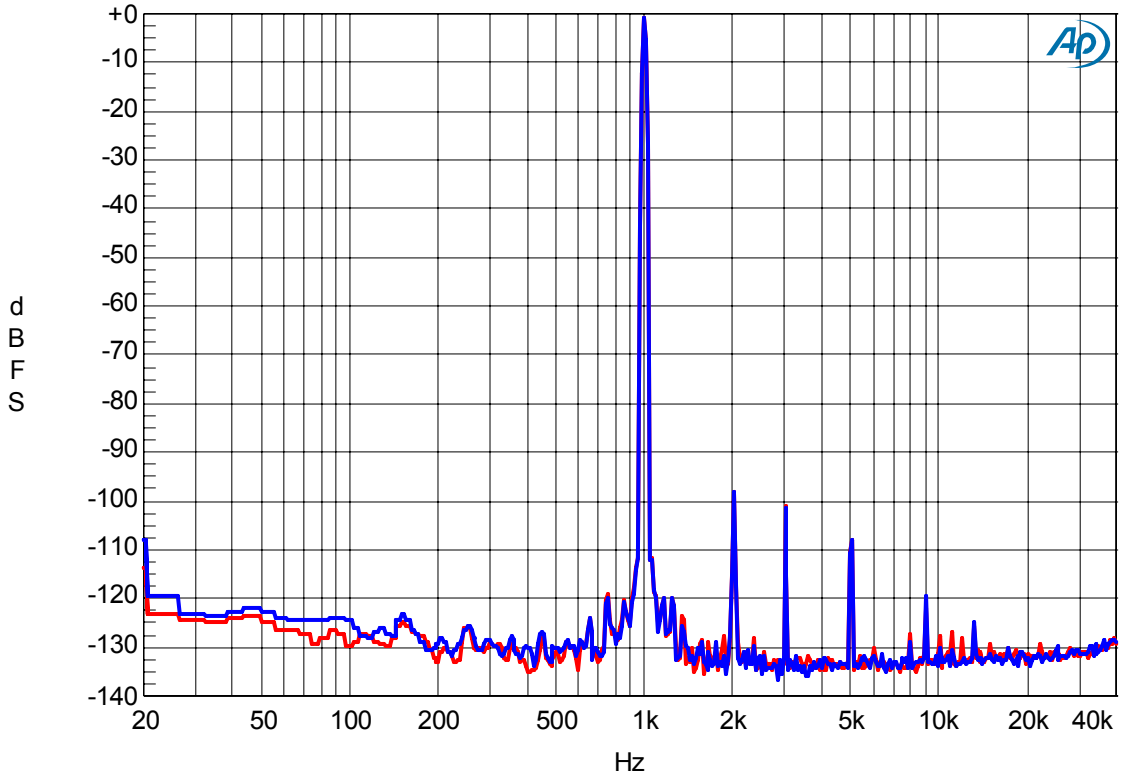


Frequency Response (Input Level=-0.5dBr)

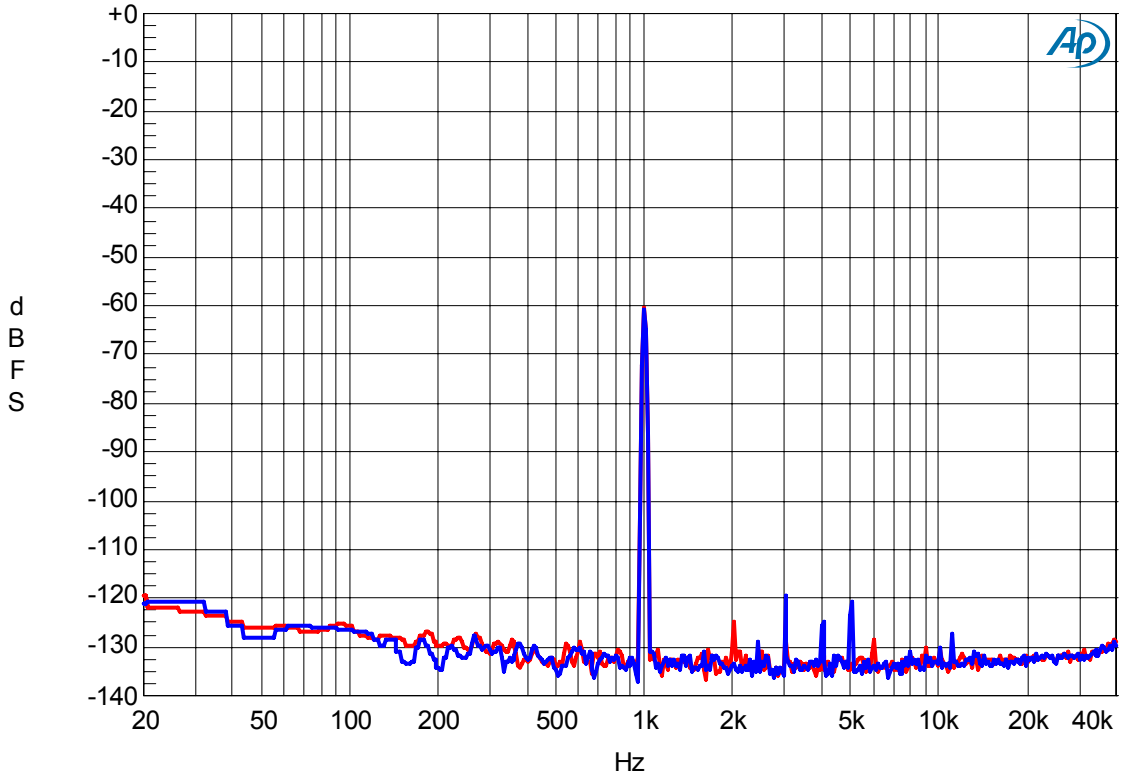


Crosstalk (Input Level=-0.5dBr)

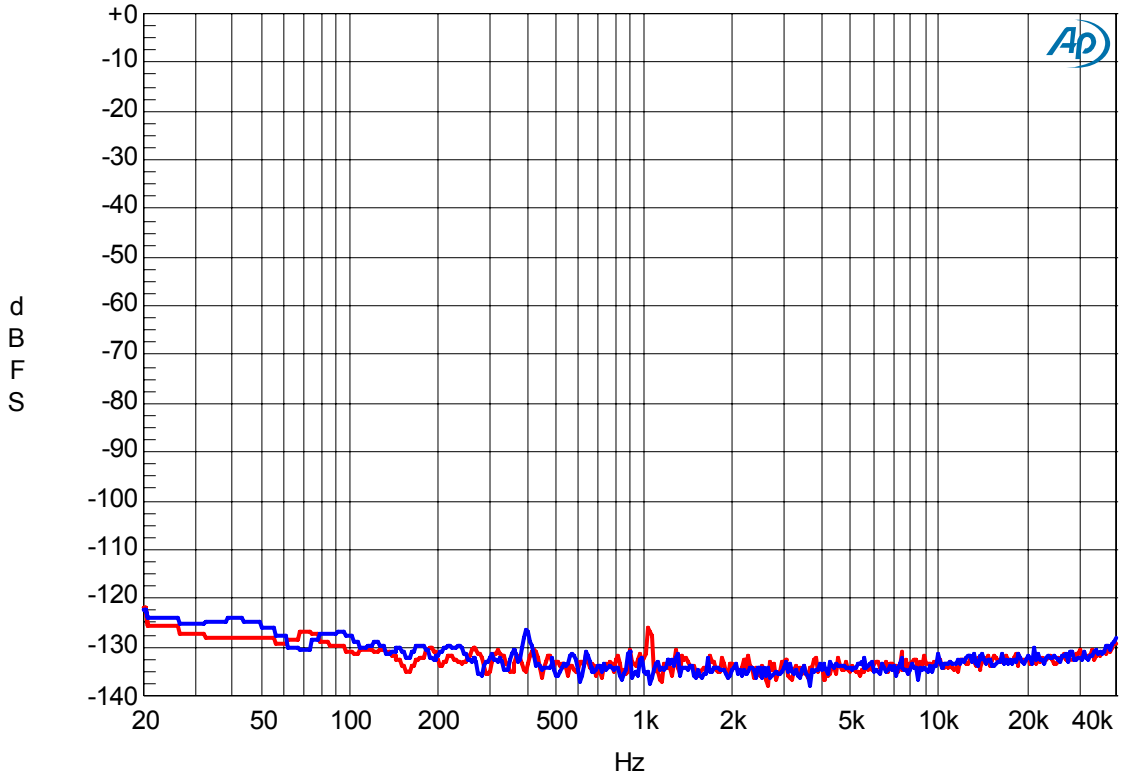
1.2.2 ADC (fs=96kHz, Differential Inputs)



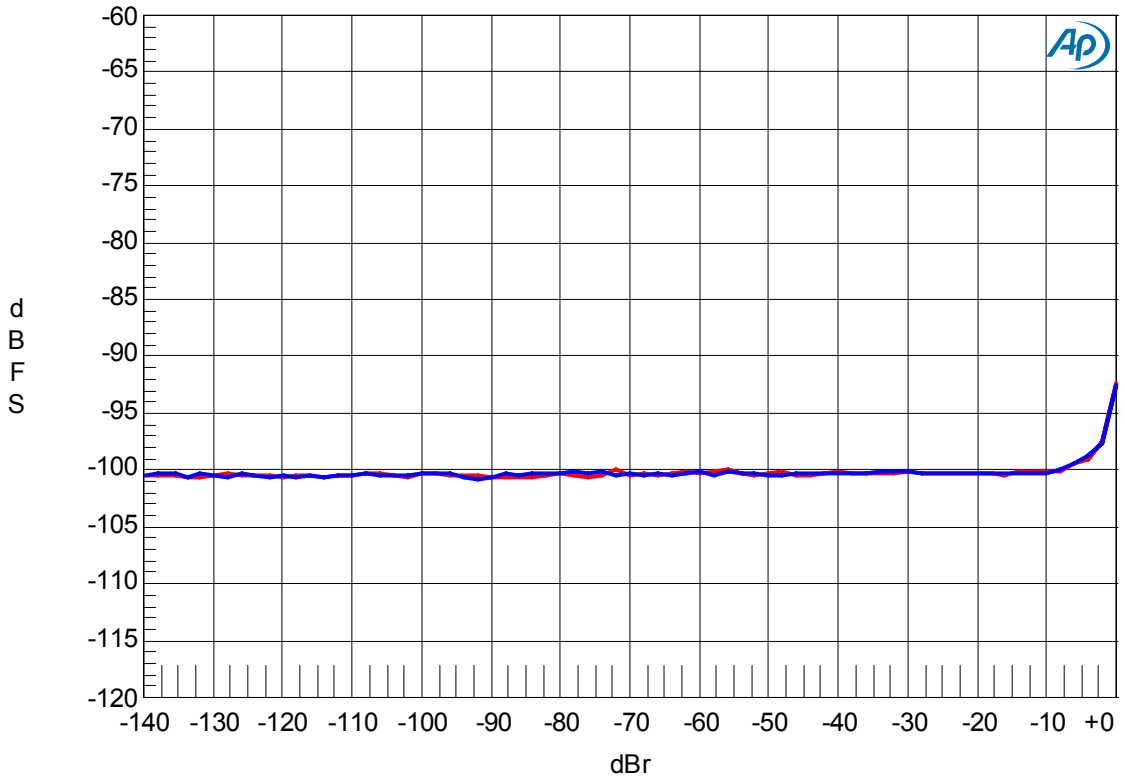
FFT (Input=-0.5dBr, fin=1kHz)



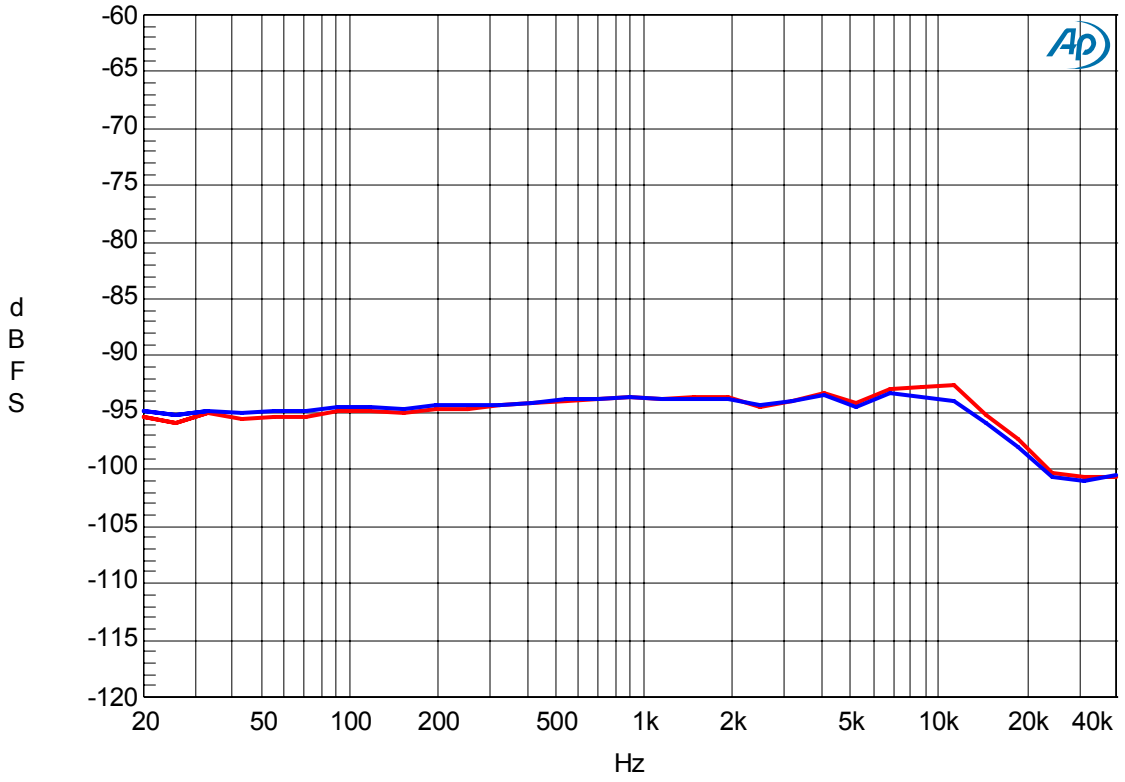
FFT (Input=-60dBr, fin=1kHz)



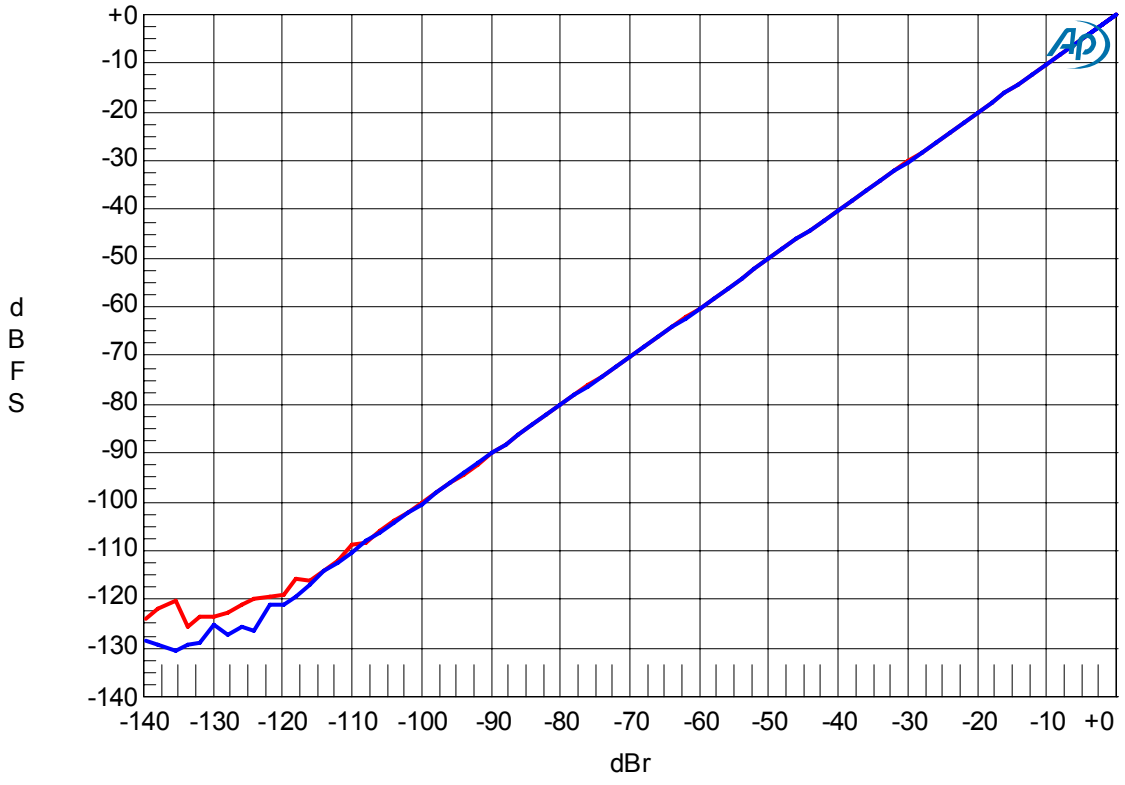
FFT (Noise floor)



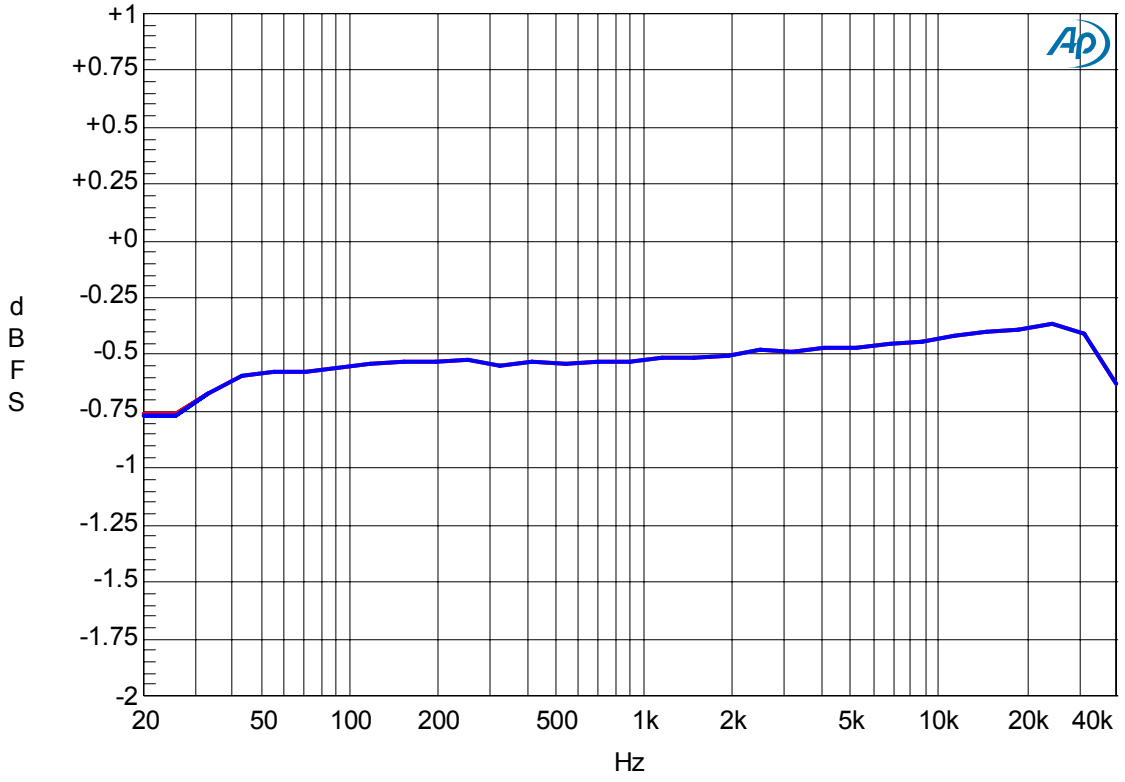
THD + N vs. Input Level (fin=1kHz)



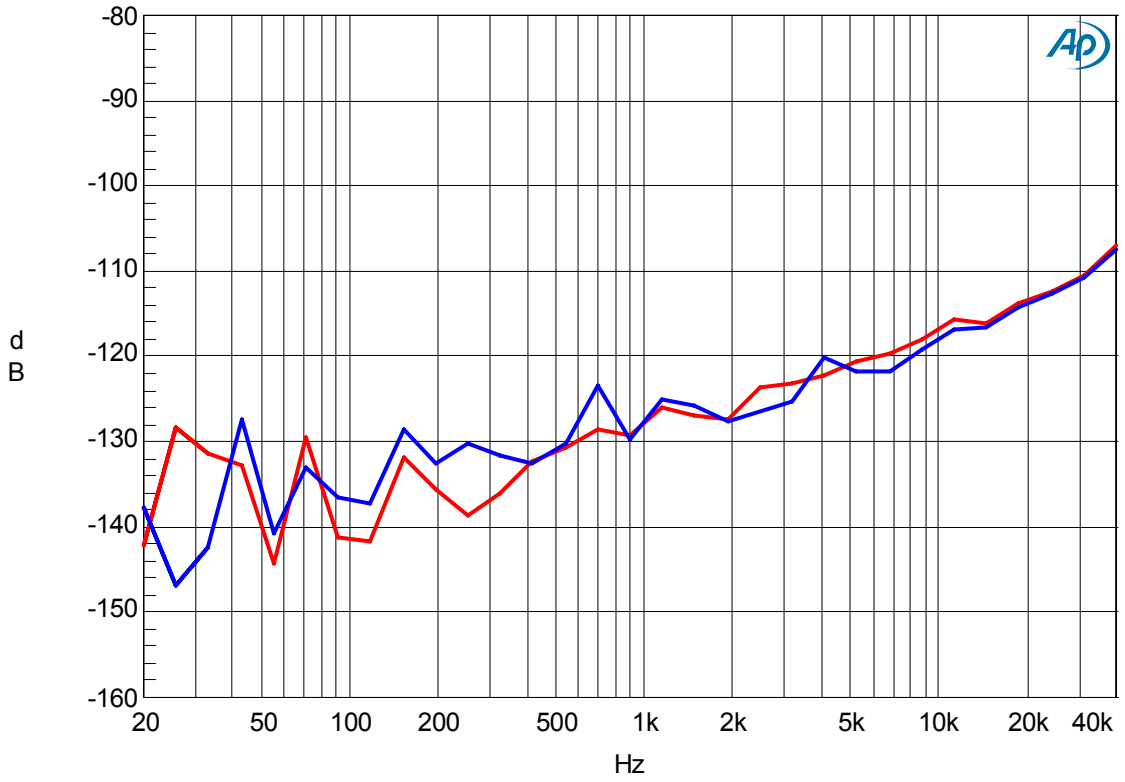
THD + N vs. Input Frequency (Input Level=-0.5dBr)



Linearity (fin=1kHz)

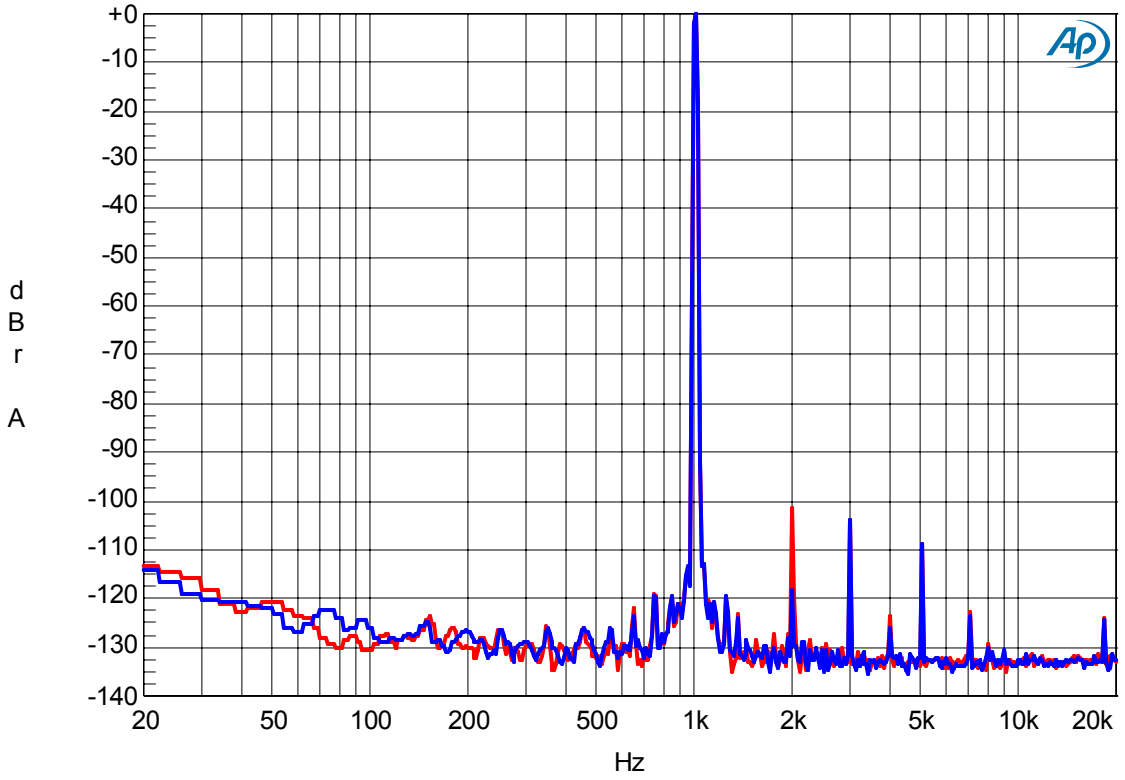


Frequency Response (Input Level=-0.5dBr)

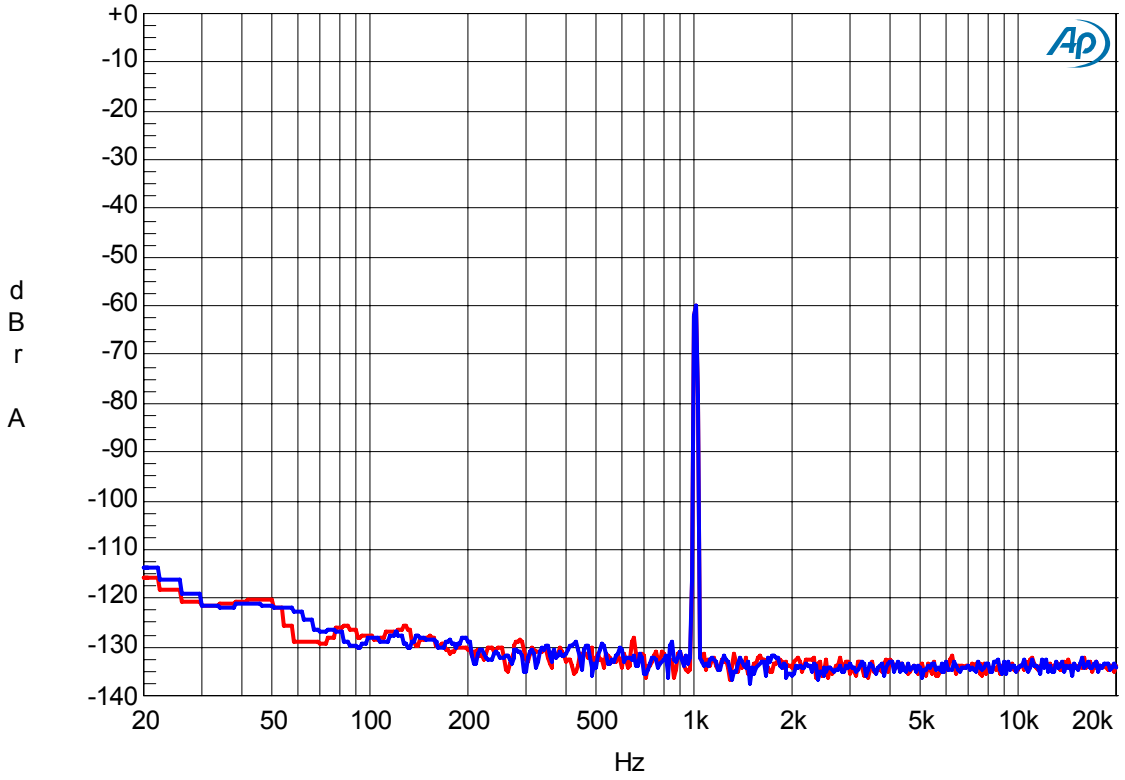


Crosstalk (Input Level=-0.5dBr)

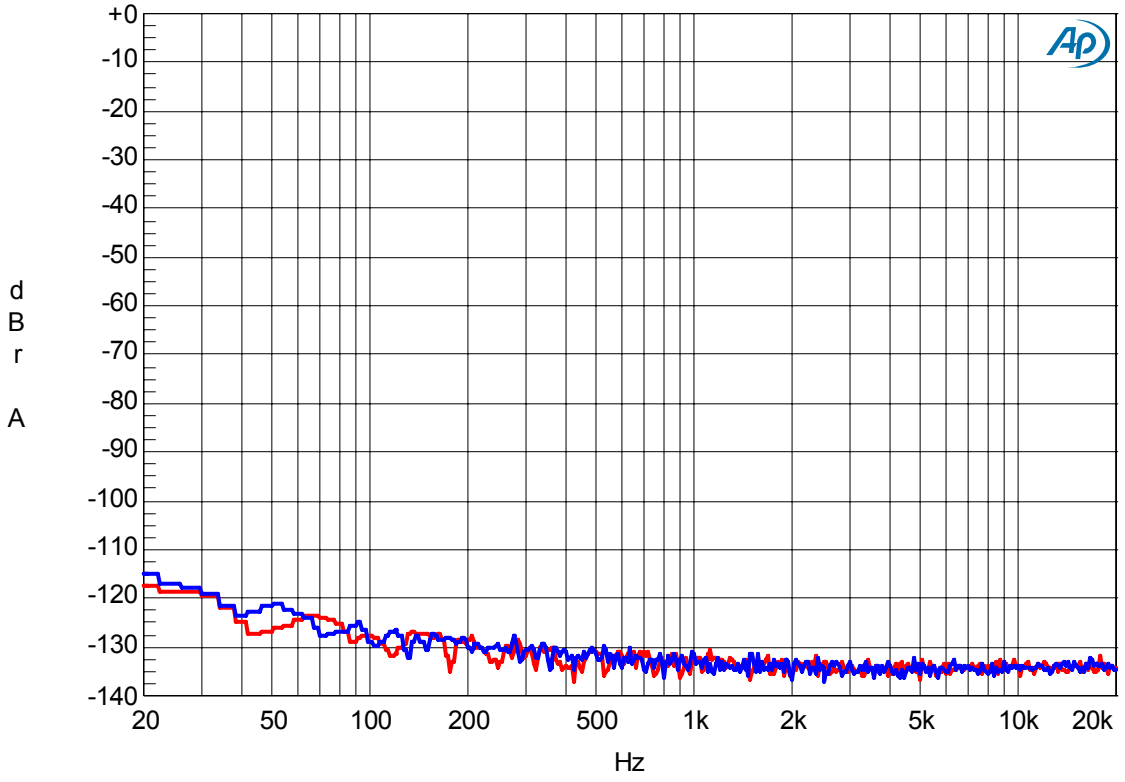
2.1 DAC (fs=48kHz)



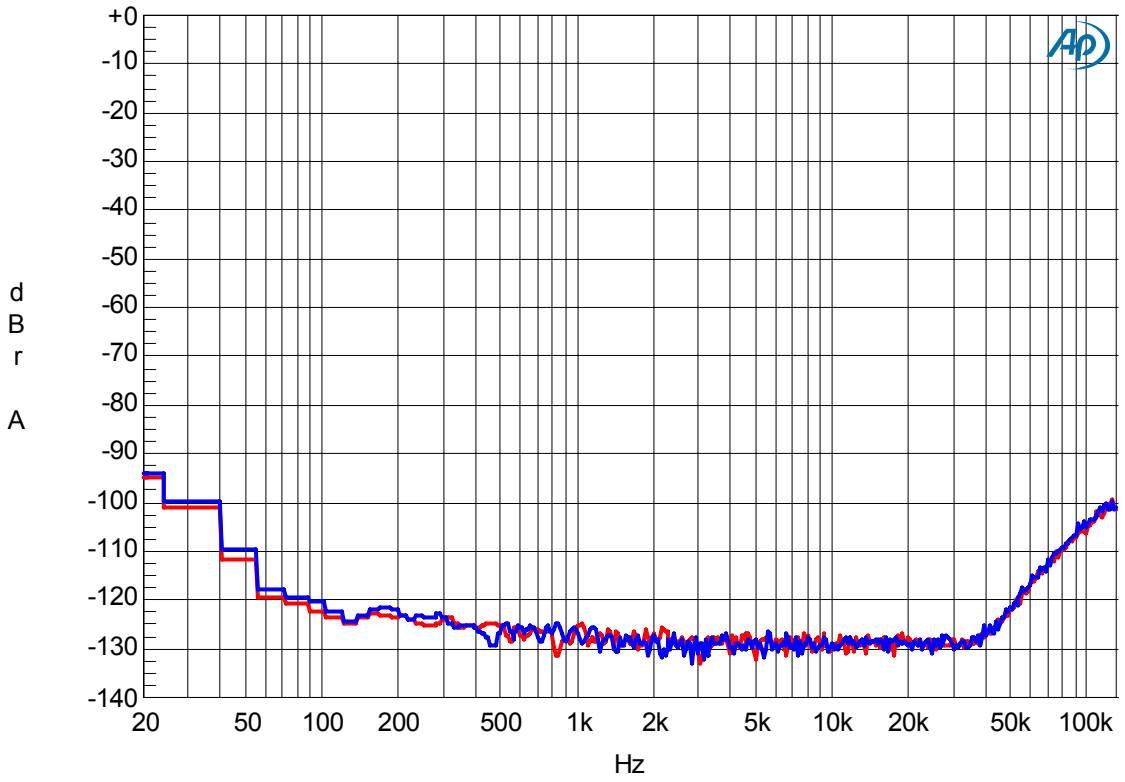
FFT (Input=0dBFS, fin=1kHz)



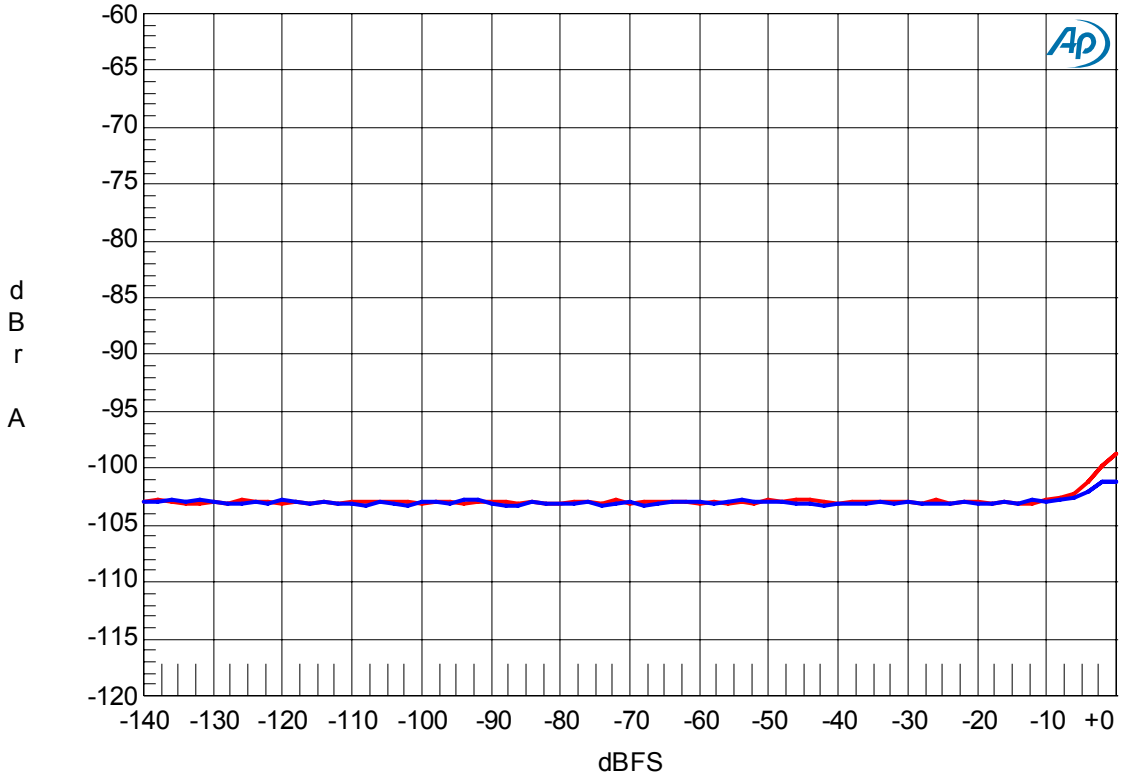
FFT (Input=-60dBFS, fin=1kHz)



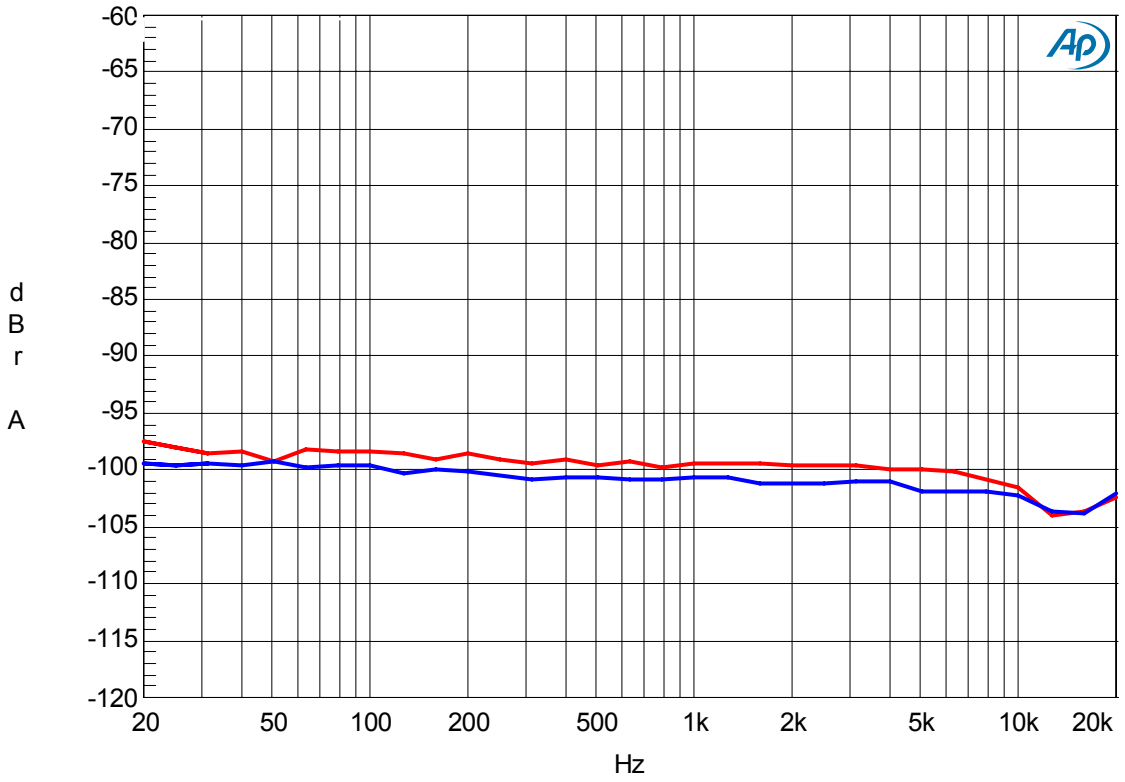
FFT (Noise floor)



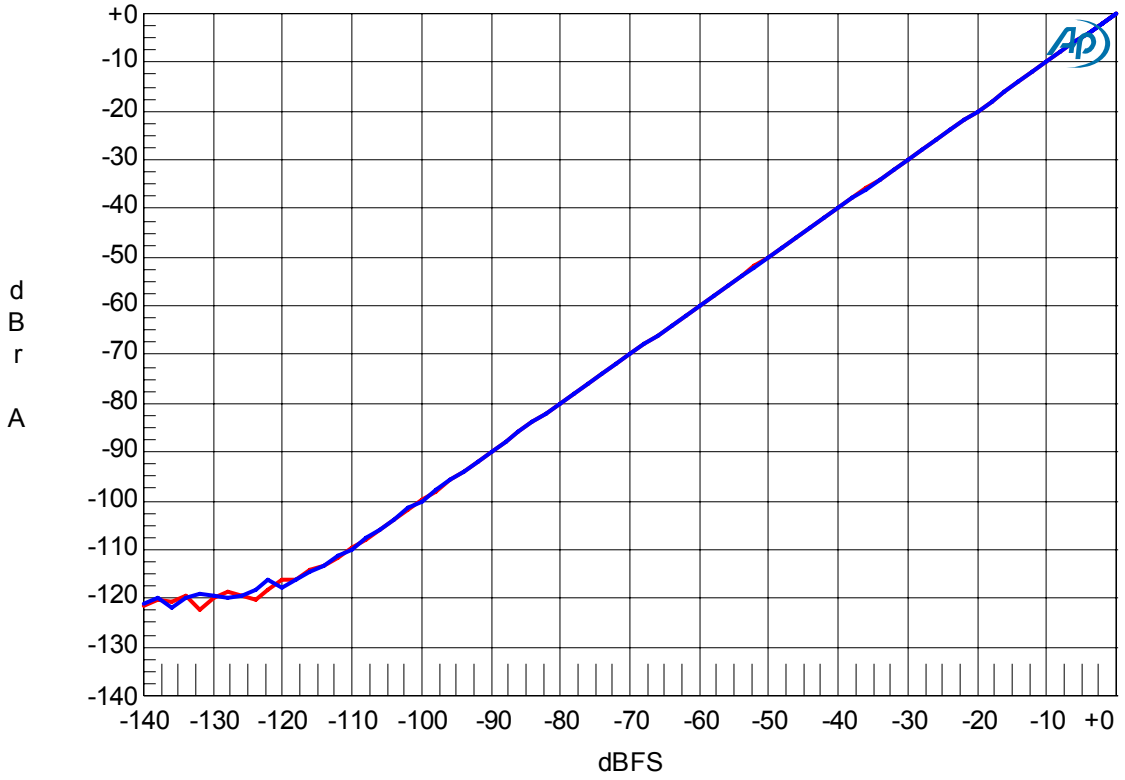
FFT (Out-of-band noise)



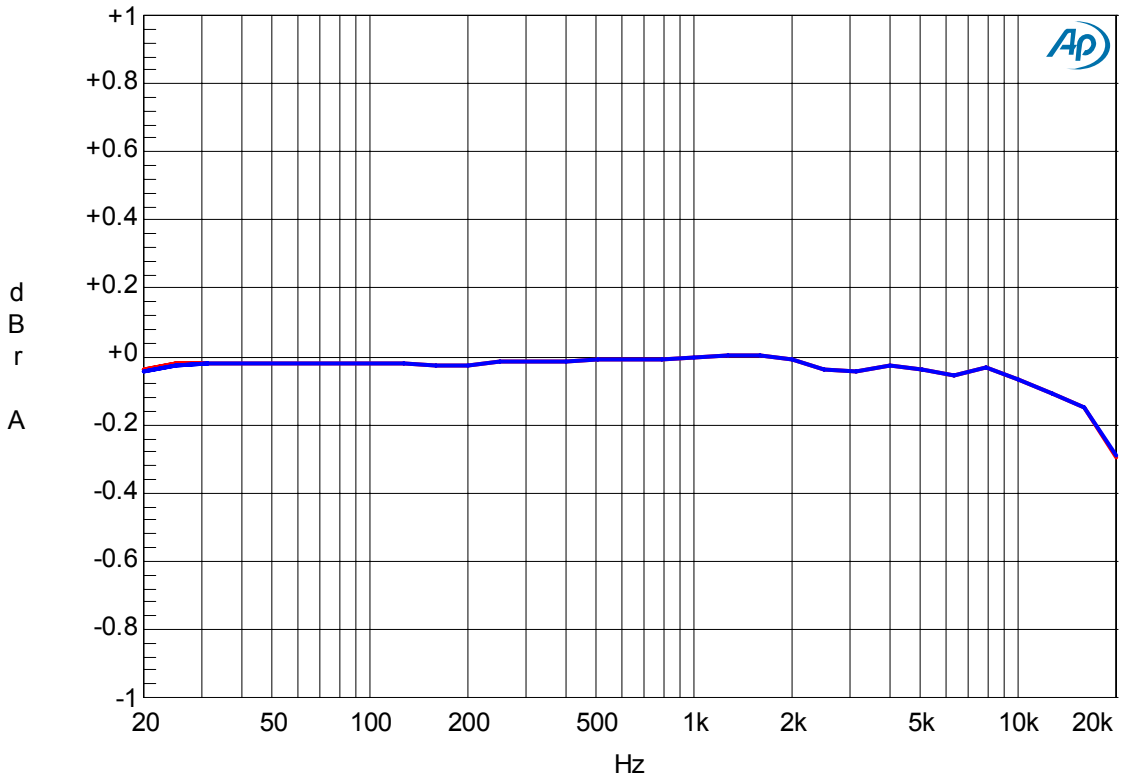
THD + N vs. Input Level (fin=1kHz)



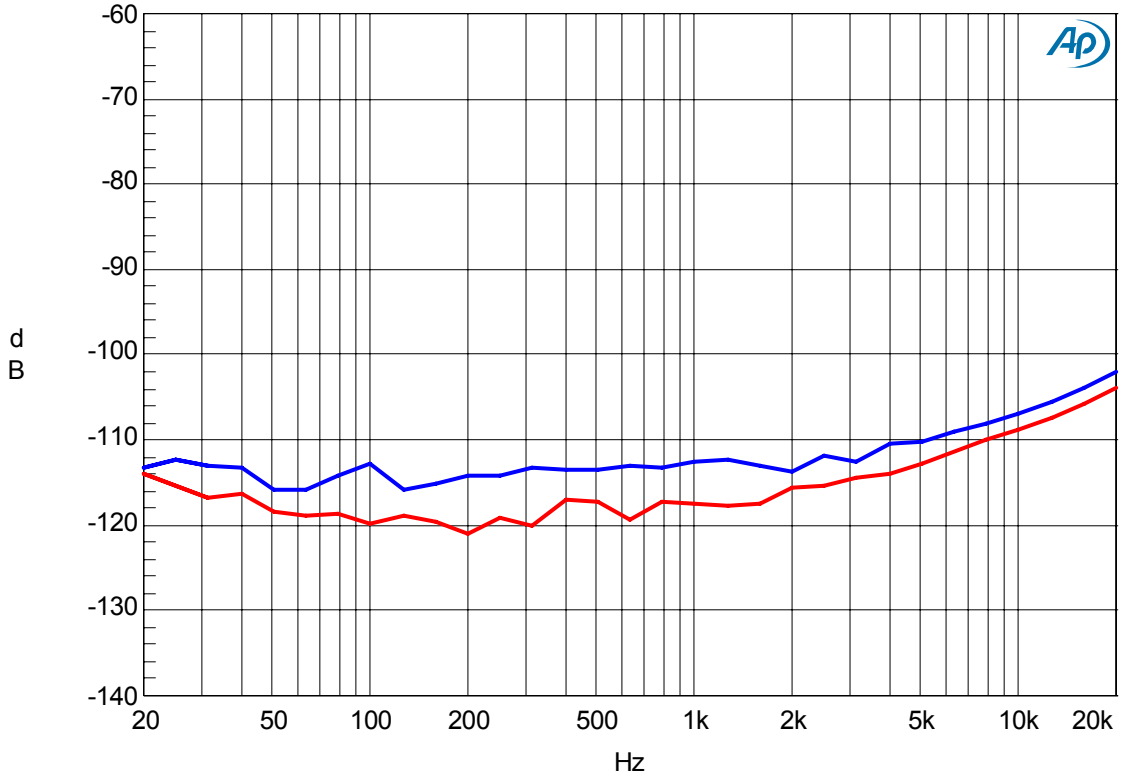
THD + N vs. Input Frequency (Input=0dBFS)



Linearity (fin=1kHz)

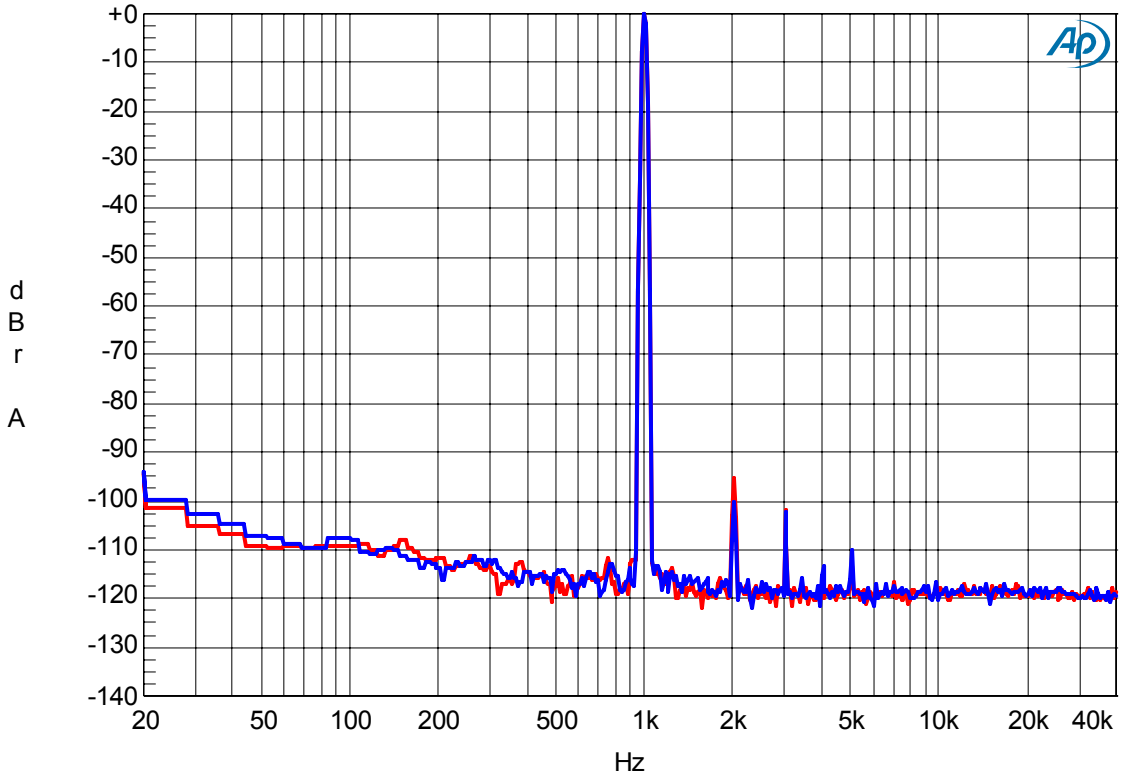


Frequency Response (Including external RC filter)

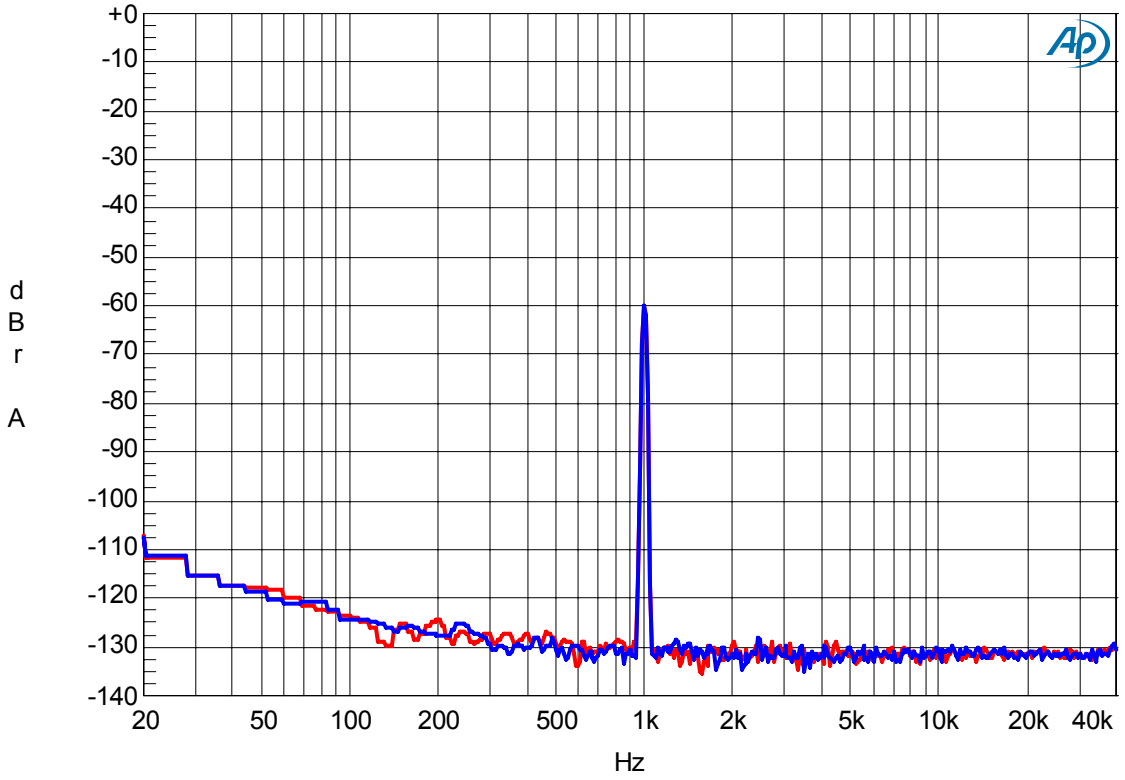

-60
-70
-80
-90
-100
-110
-120
-130
-140
dB
20
50
100
200
500
1k
2k
5k
10k
20k
Hz

Crosstalk

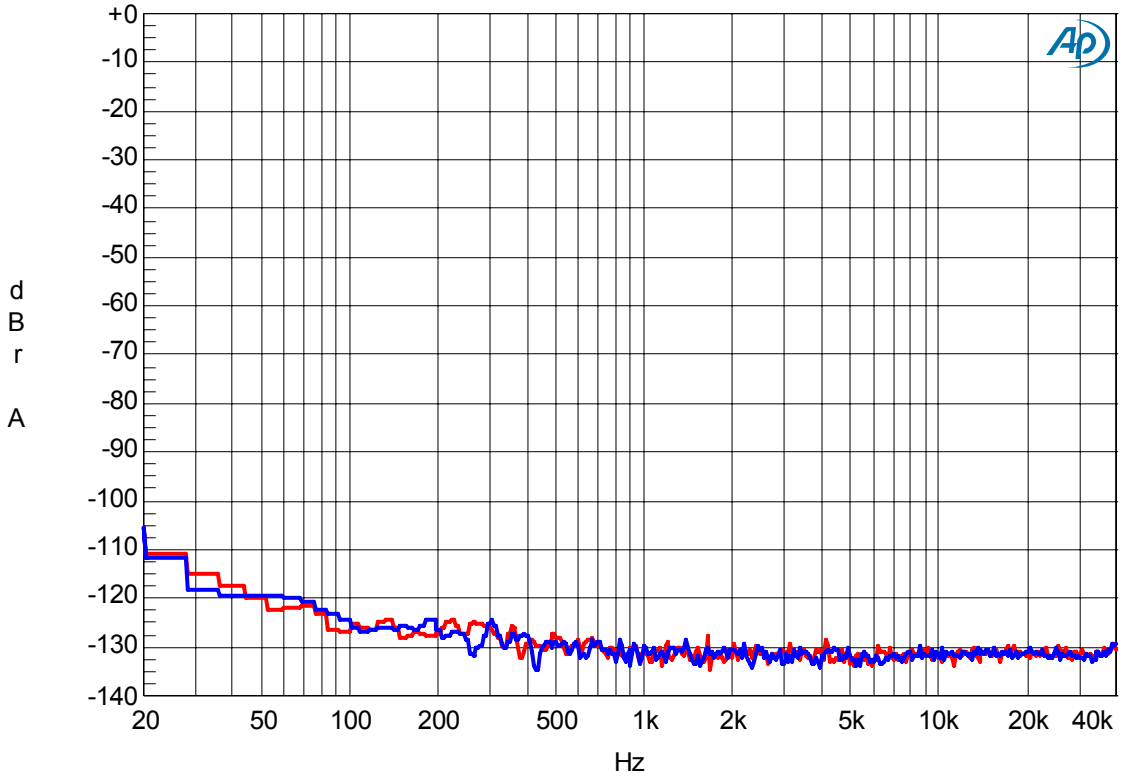
2.2 DAC (fs=96kHz)



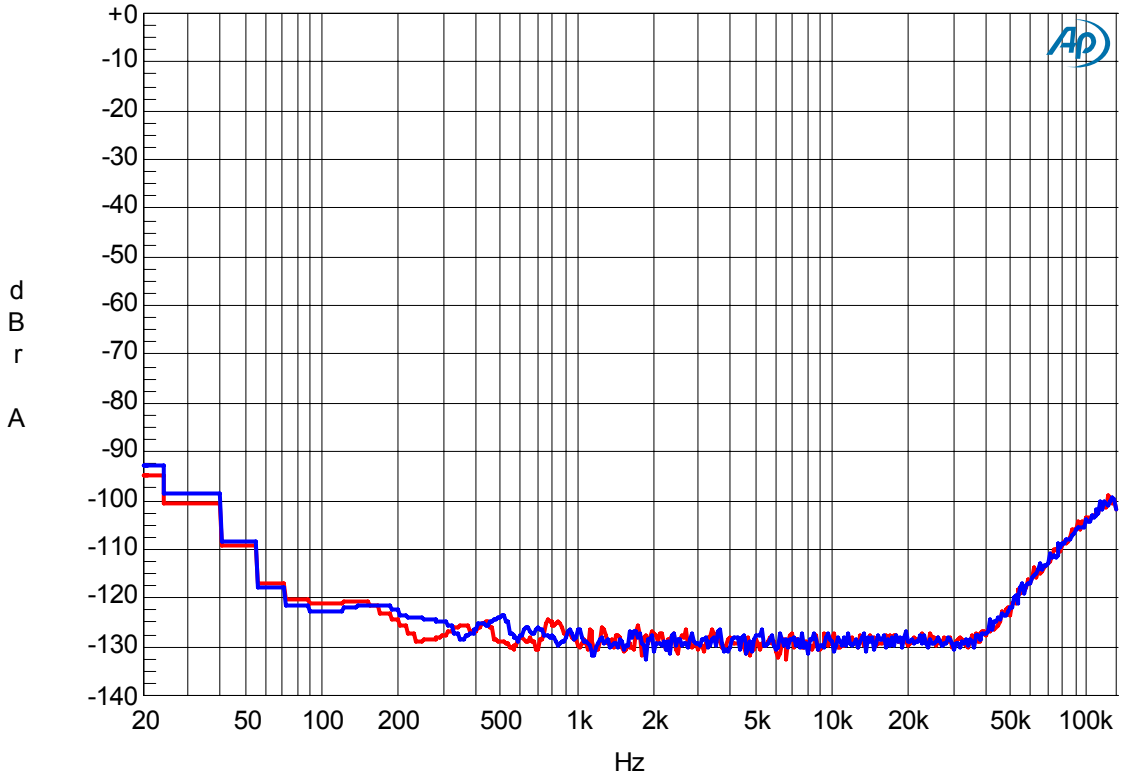
FFT (Input=0dBFS, fin=1kHz)



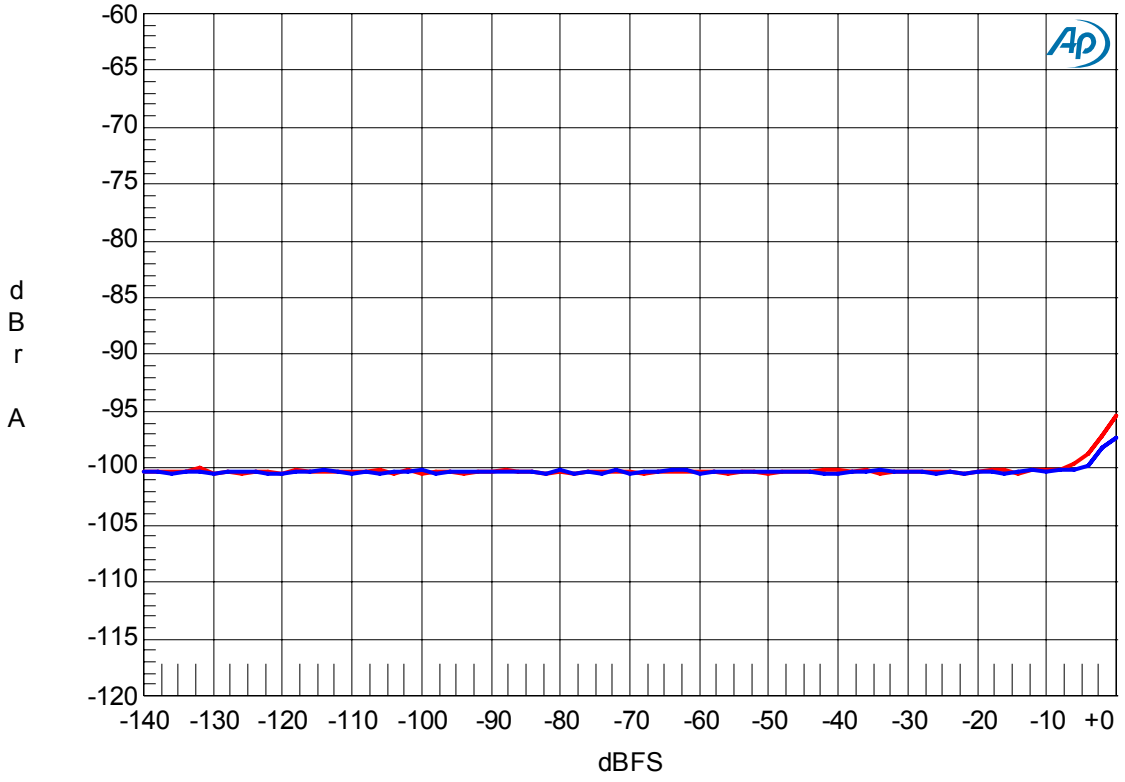
FFT (Input=-60dBFS,fin=1kHz)



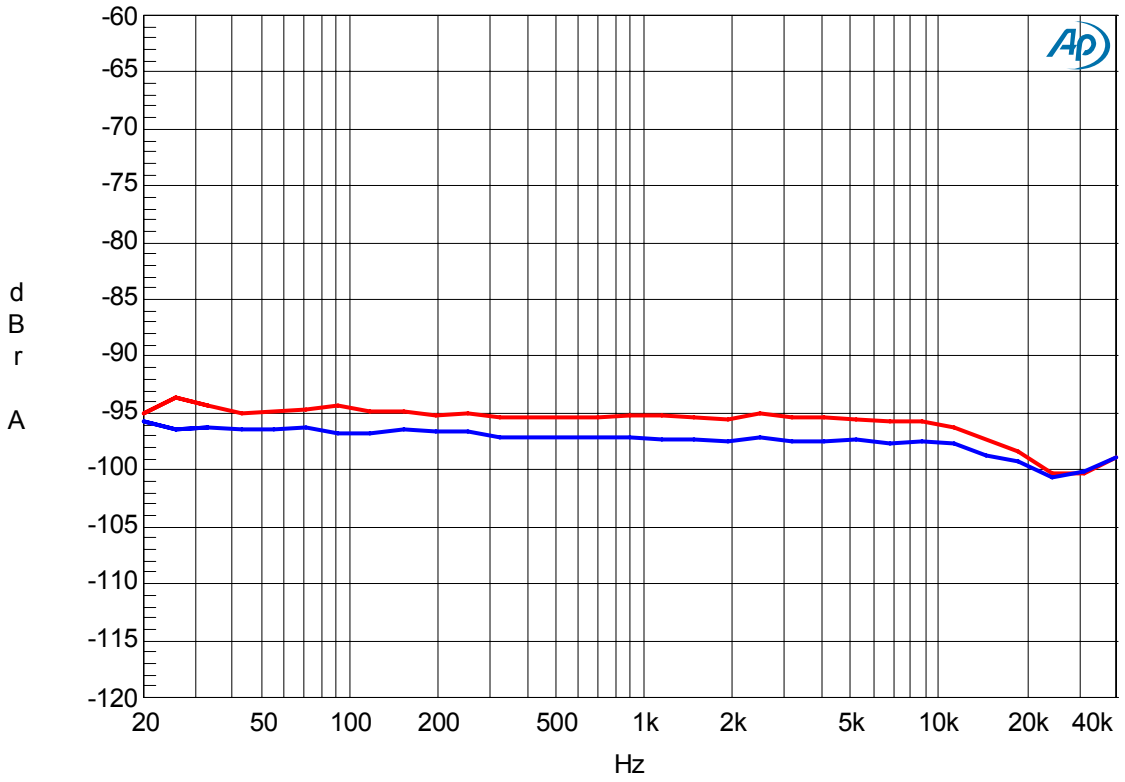
FFT (Noise floor)



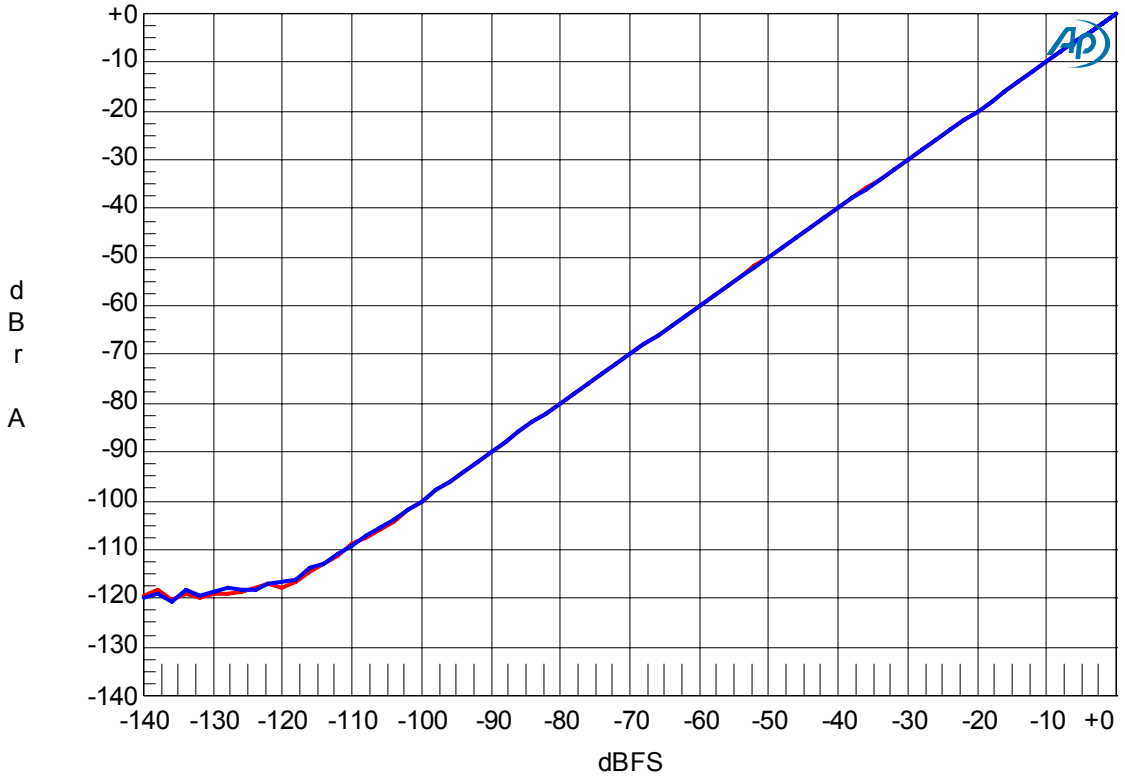
FFT (Out-of-band noise)



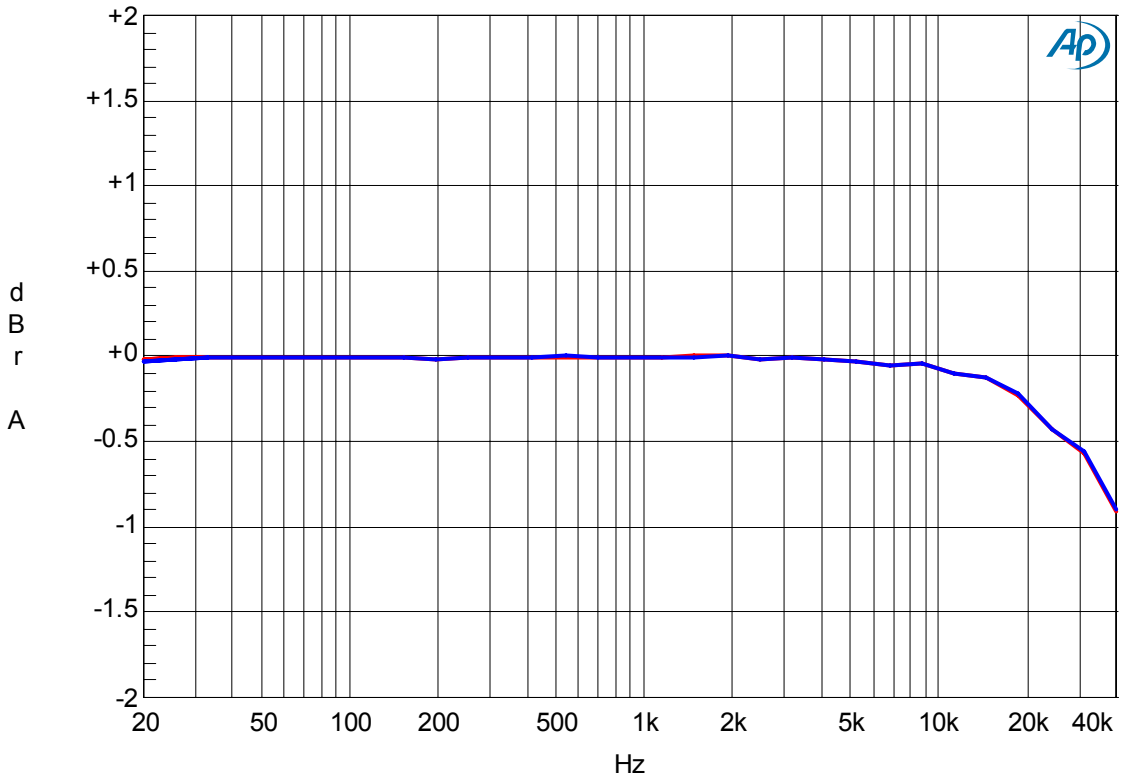
THD + N vs. Input Level (fin=1kHz)



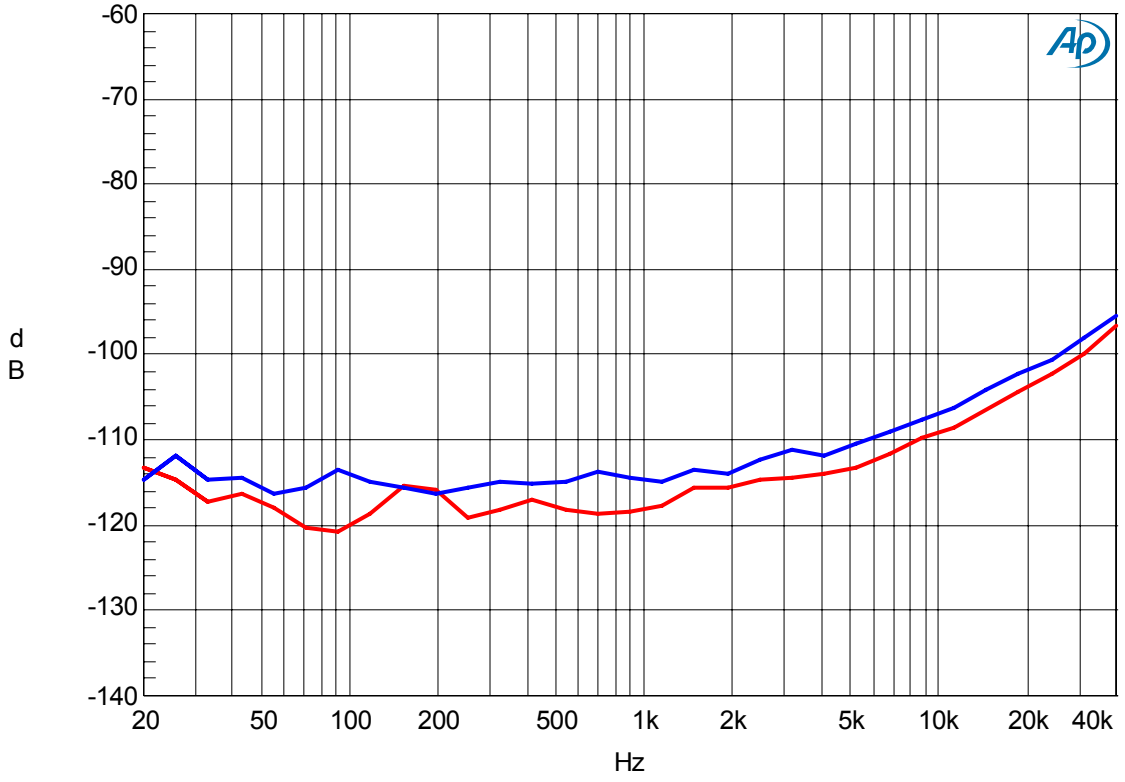
THD + N vs. Input Frequency (Input=0dBFS)



Linearity (fin=1kHz)

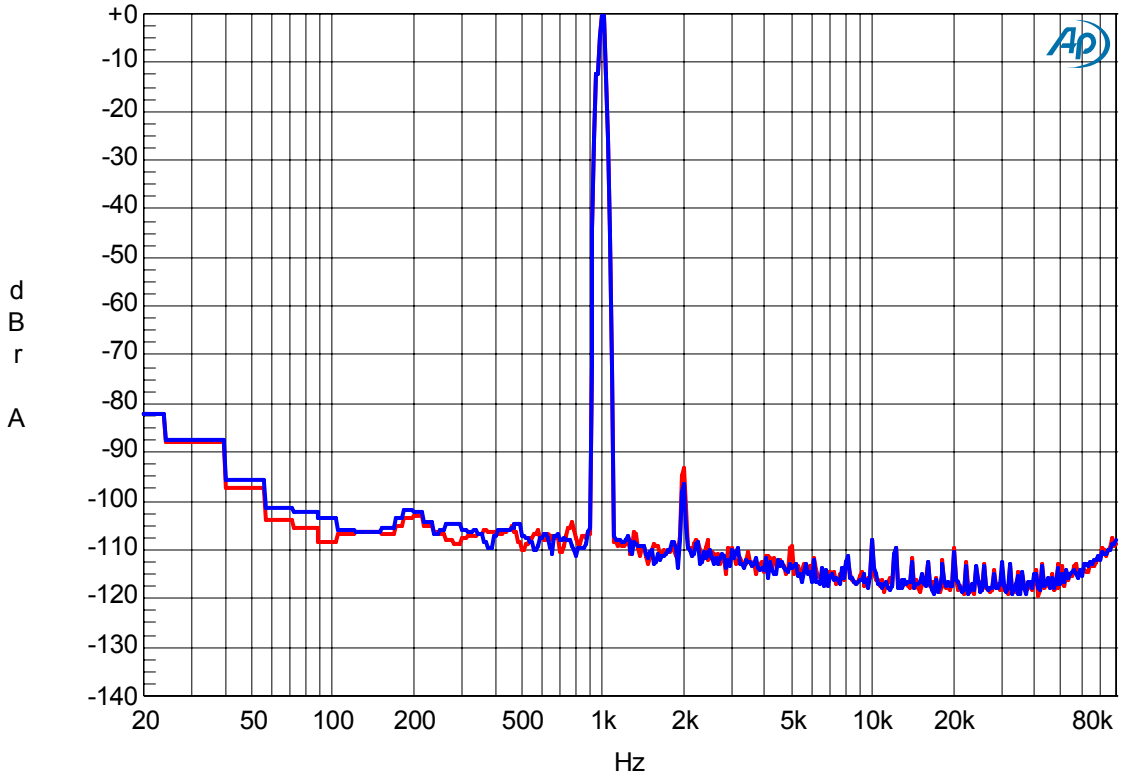


Frequency Response (Including external RC filter)

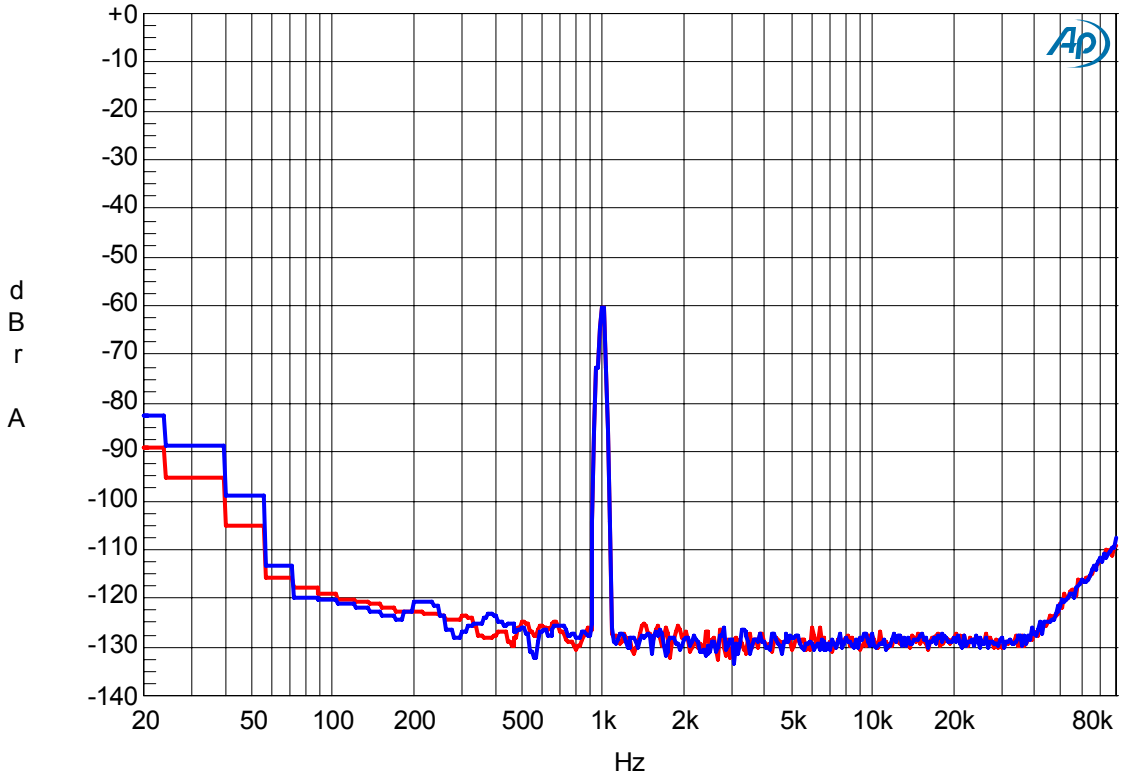


Crosstalk (Input=0dBFS)

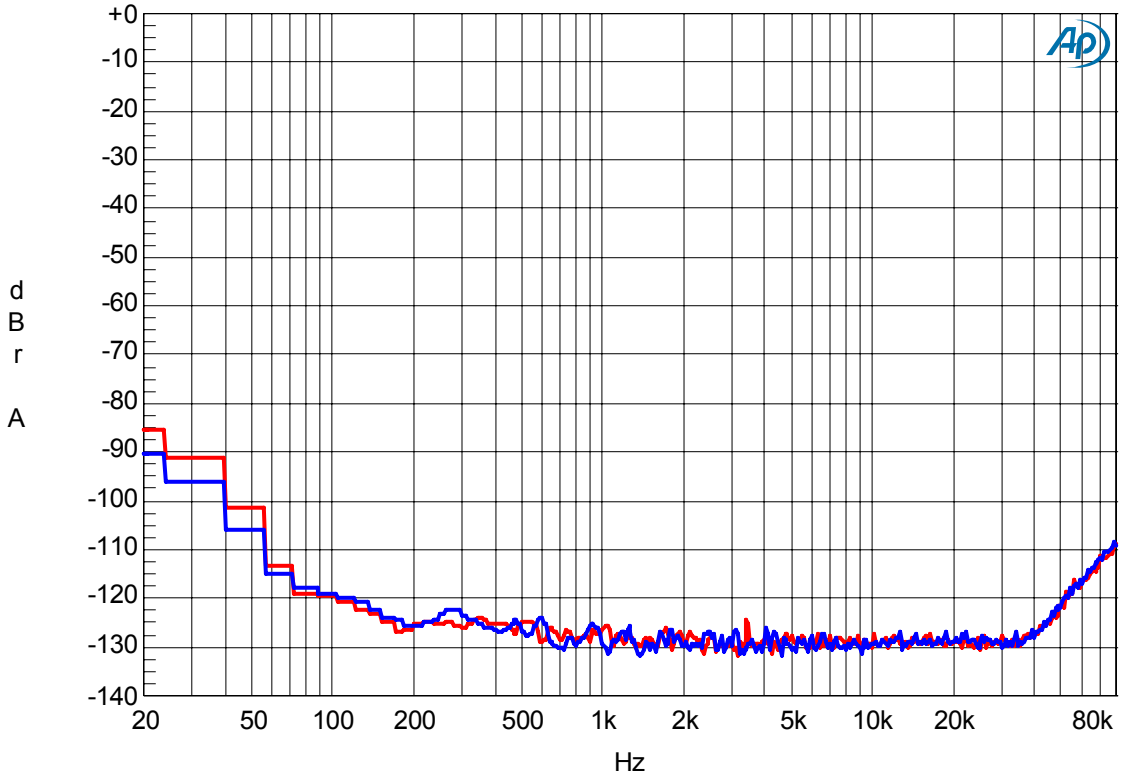
2.3 DAC (fs=192kHz)



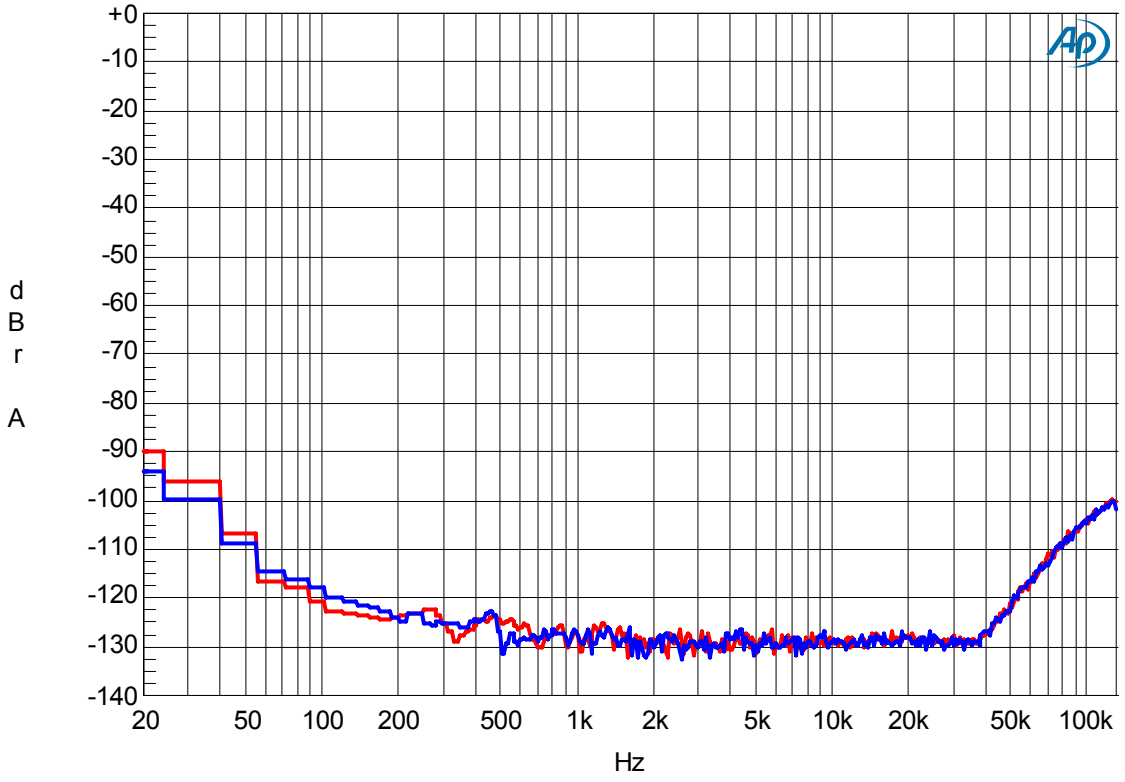
FFT (Input=0dBFS, fin=1kHz)



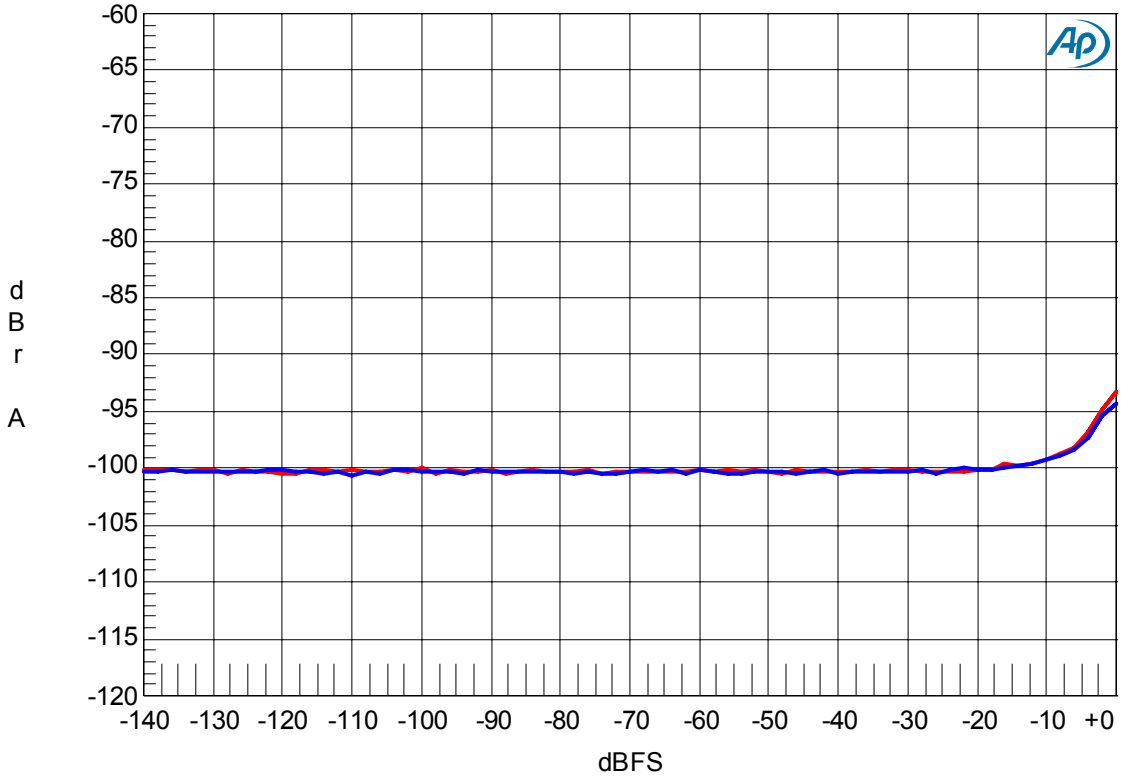
FFT (Input=-60dBFS,fin=1kHz)



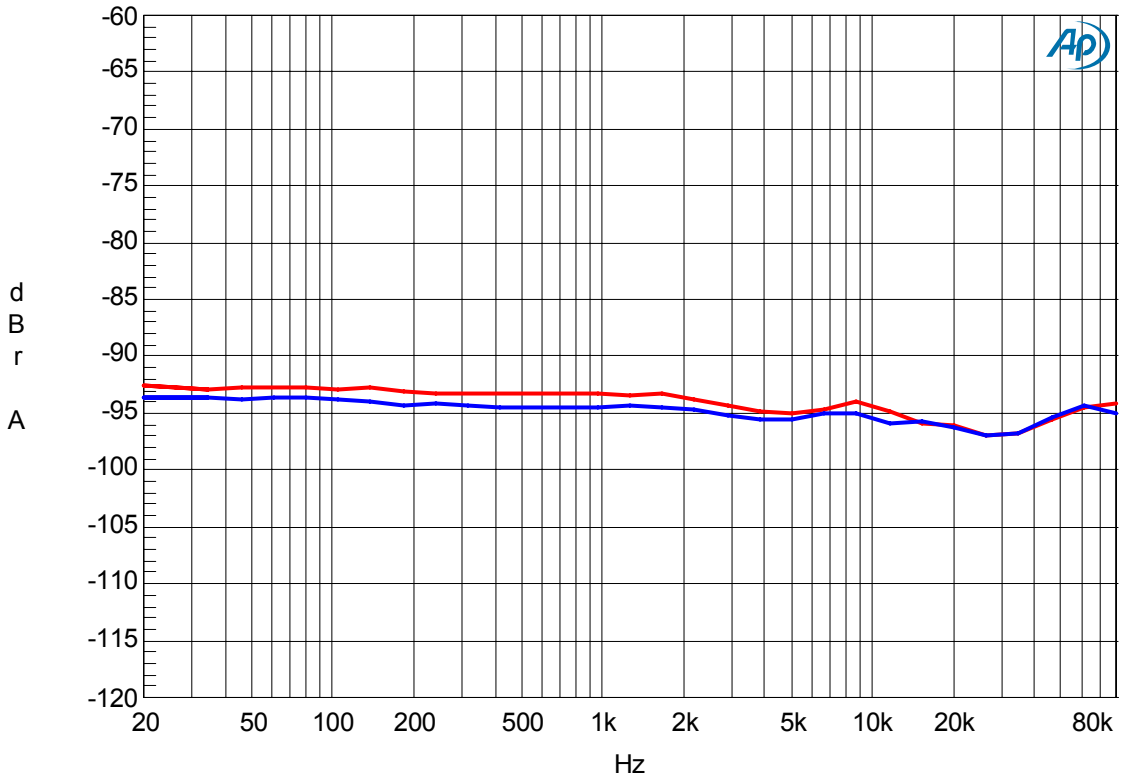
FFT (Noise floor)



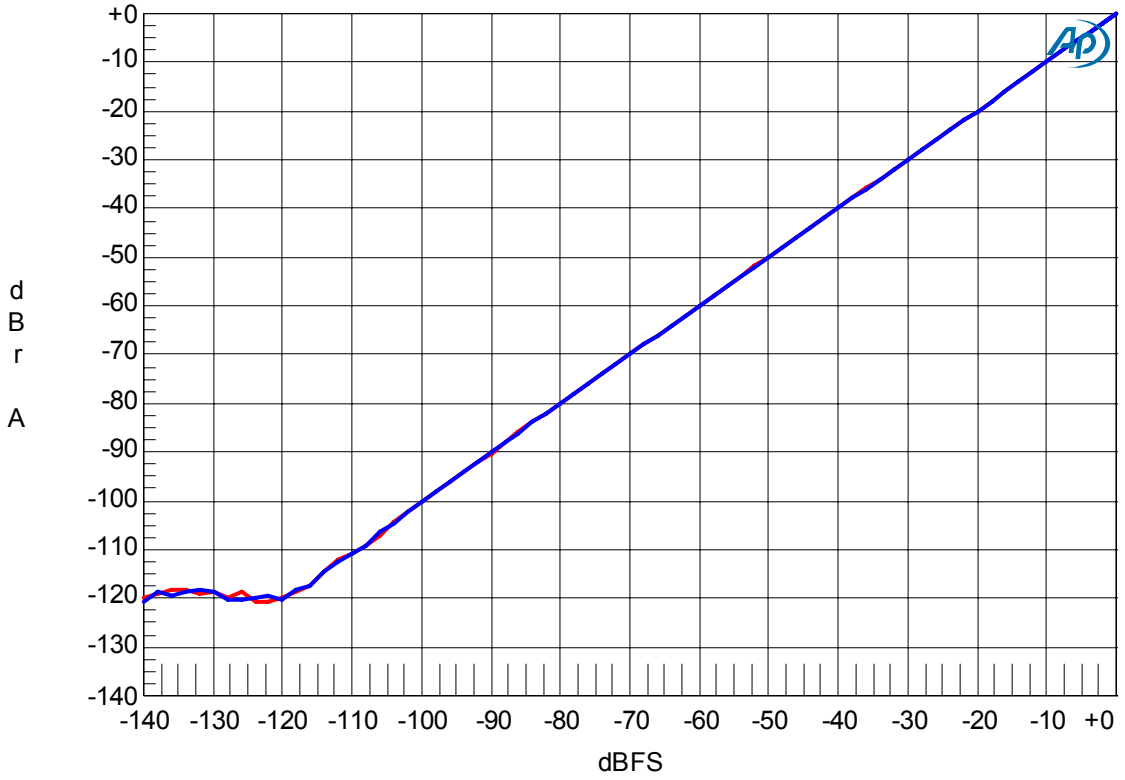
FFT (Out-of-band noise)



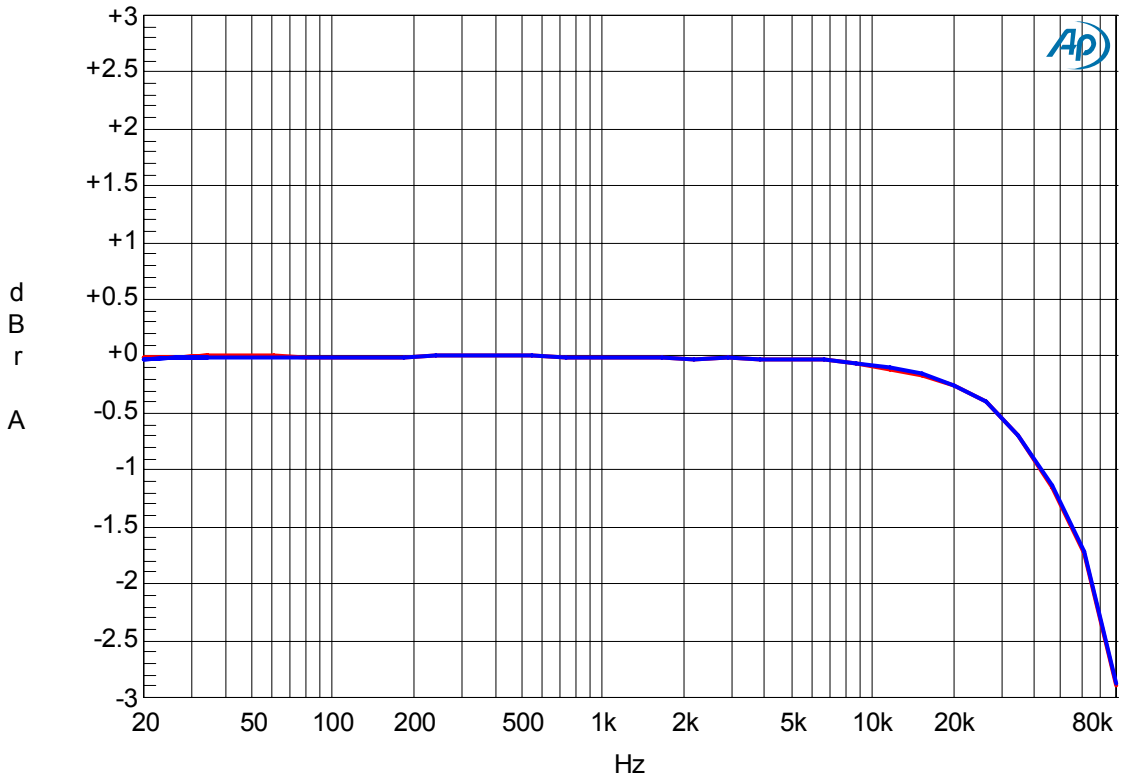
THD + N vs. Input Level (fin=1kHz)



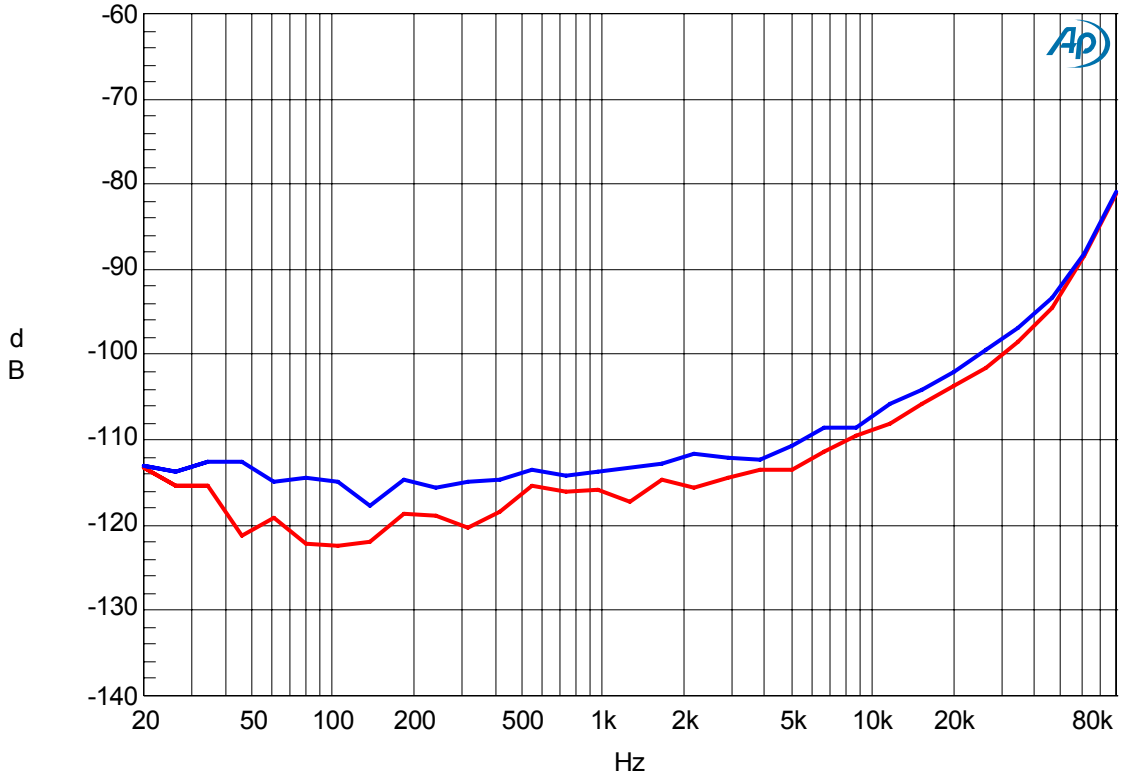
THD + N vs. Input Frequency (Input=0dBFS)



Linearity (fin=1kHz)



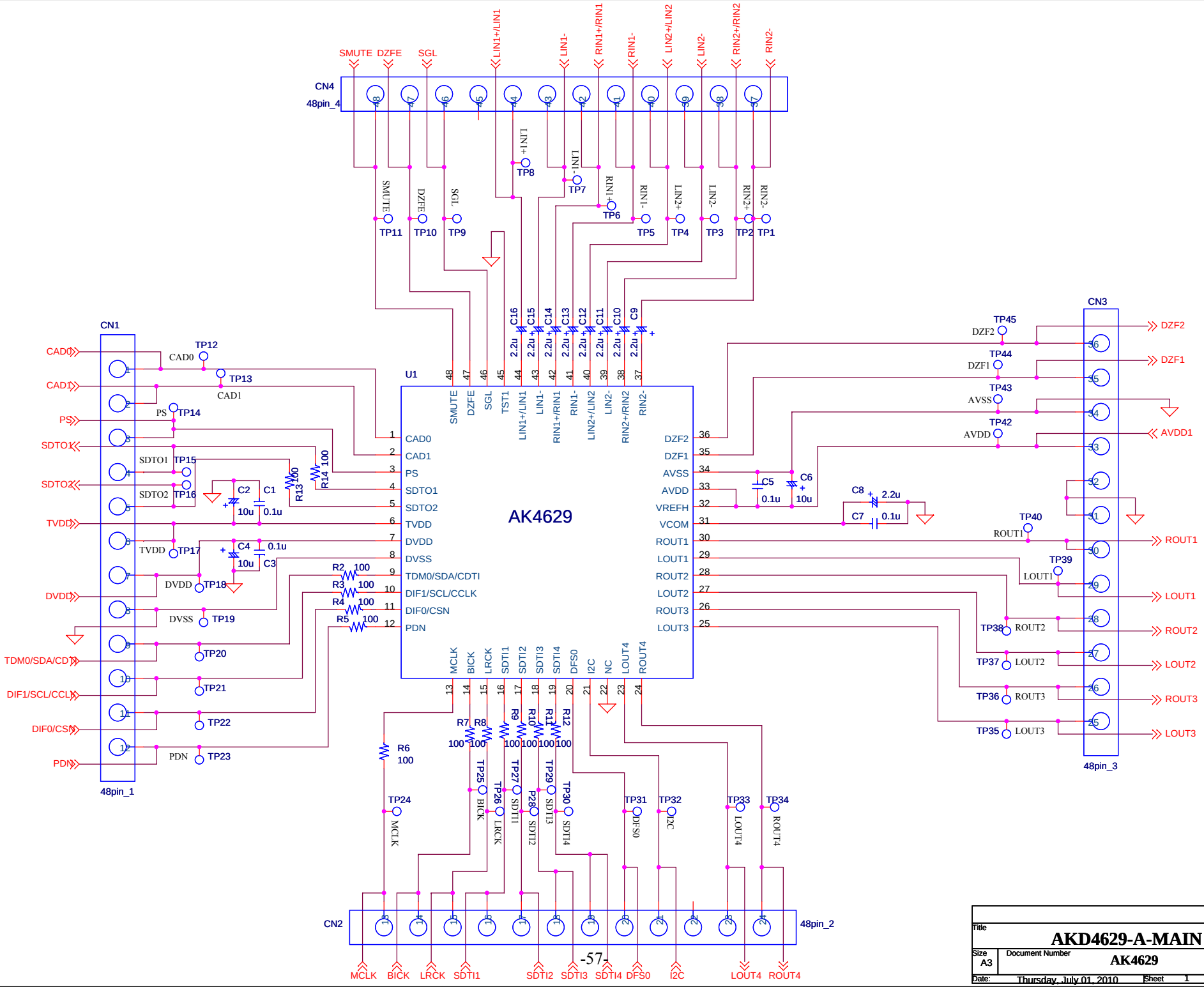
Frequency Response (Including external RC filter)



Crosstalk (Input=0dBFS)

Revision History

Date (YY/MM/DD)	Manual Revision	Board Revision	Reason	Contents
2010/08/09	KM101900	0	First Edition	
2010/01/26	KM101901	1	Device Rev. Changed Contorl Soft Rev. updated	AKD4629 Rev.A → Rev.B Measurement results were updated. P11, P15: Control soft's plots were updated; P11: The explanation about AKDUSBIF-B interface board was added. P16, P17: Explanations of the "Tool" tab were added.



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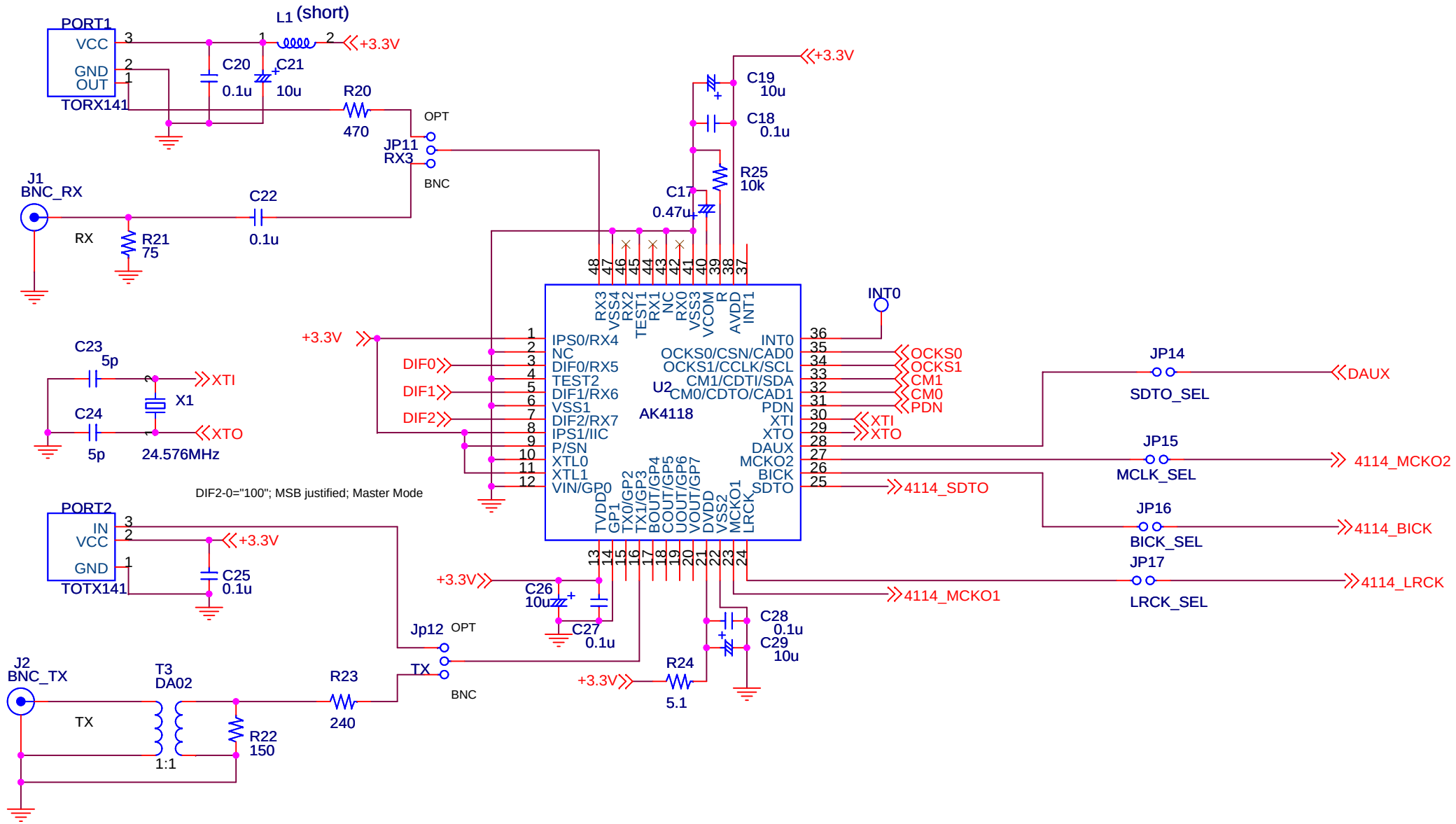
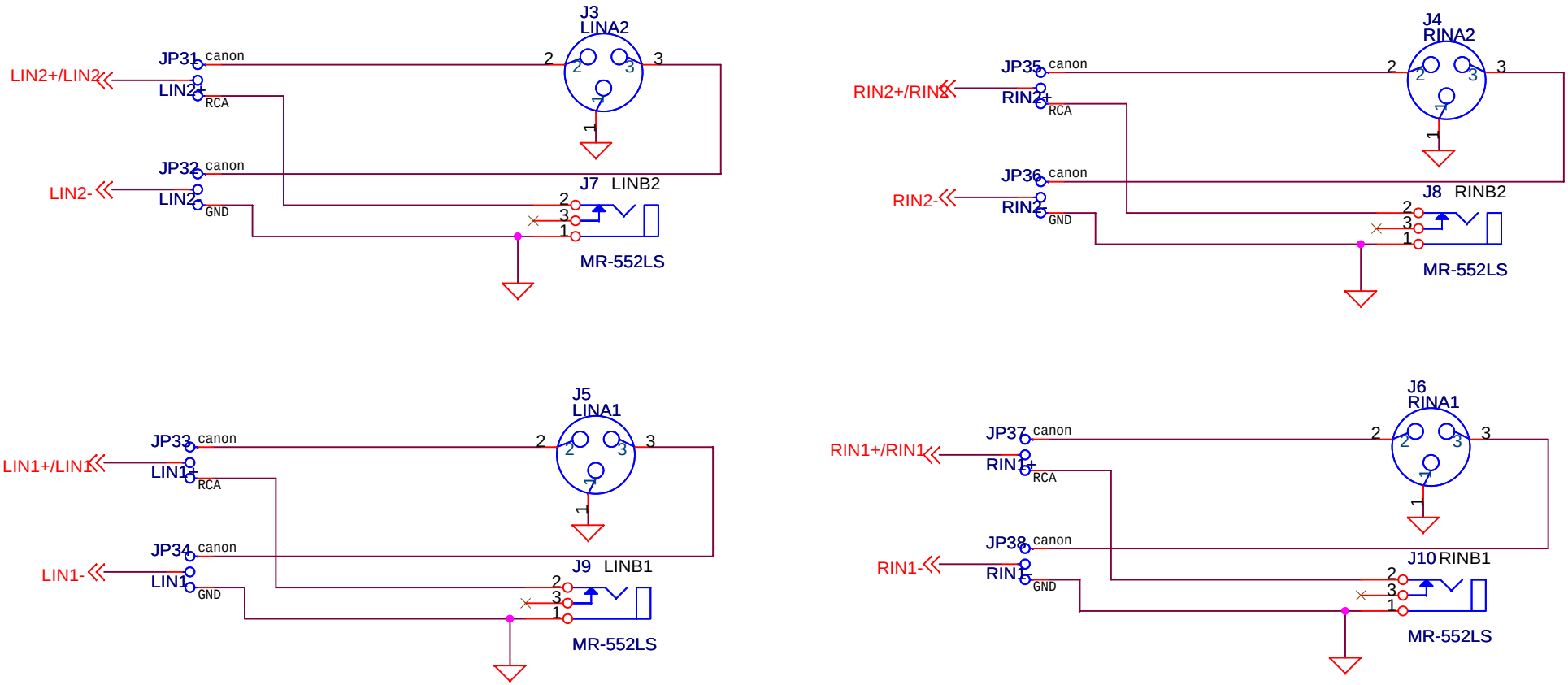
Size A3	Document Number AK4629		Rev 0
Date: Thursday, July 01, 2010	Sheet 1 of 6		



Title	AKD4629-A-Main	
Size A4	Document Number AK4114	Rev 0
Date: Monday, December 21, 2009	Sheet 1 of 6	



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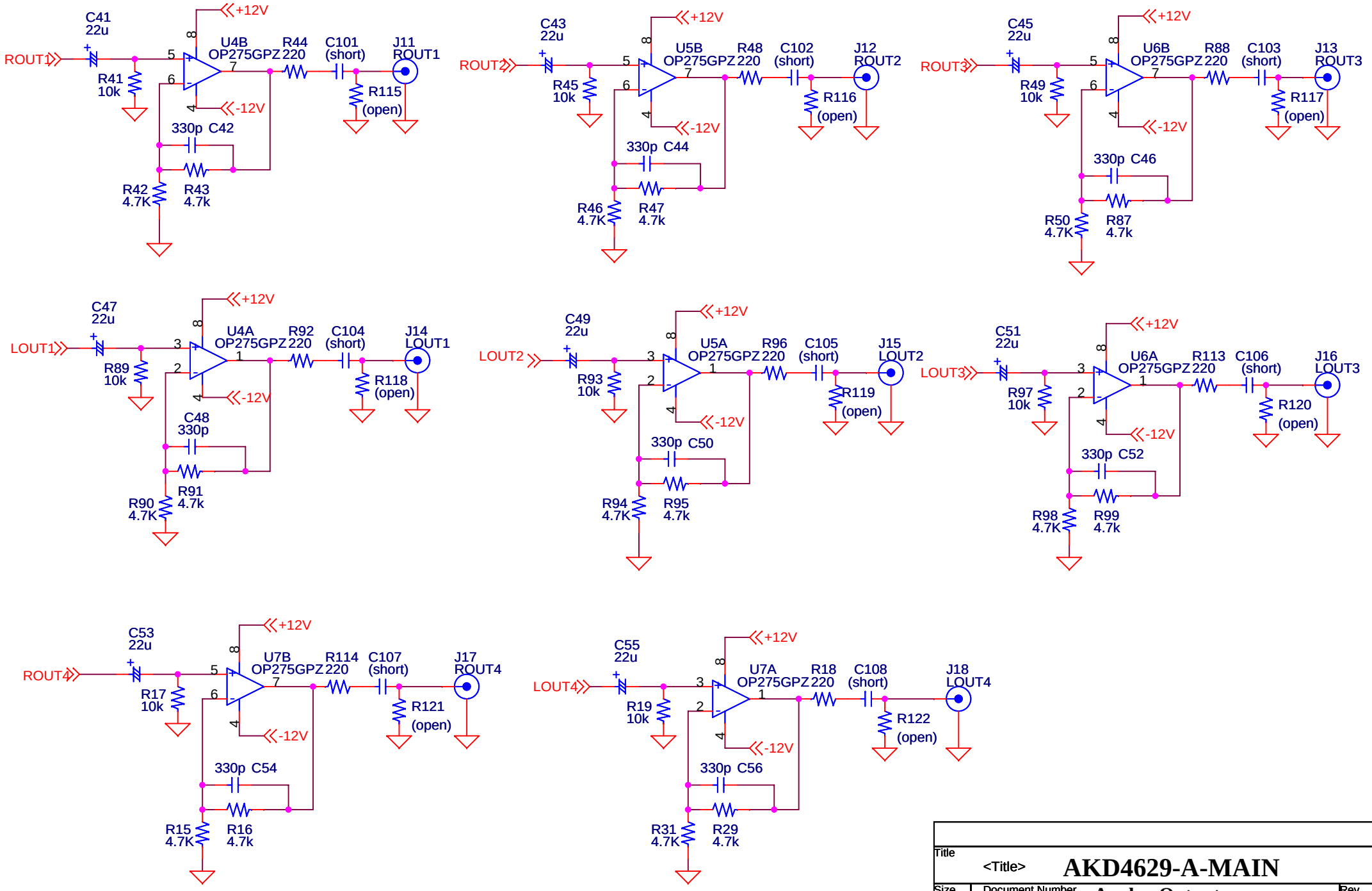
Size A4	Document Number <Doc>	Analog Input	Rev 0
Date: Tuesday, December 01, 2009	Sheet 3 of 6		



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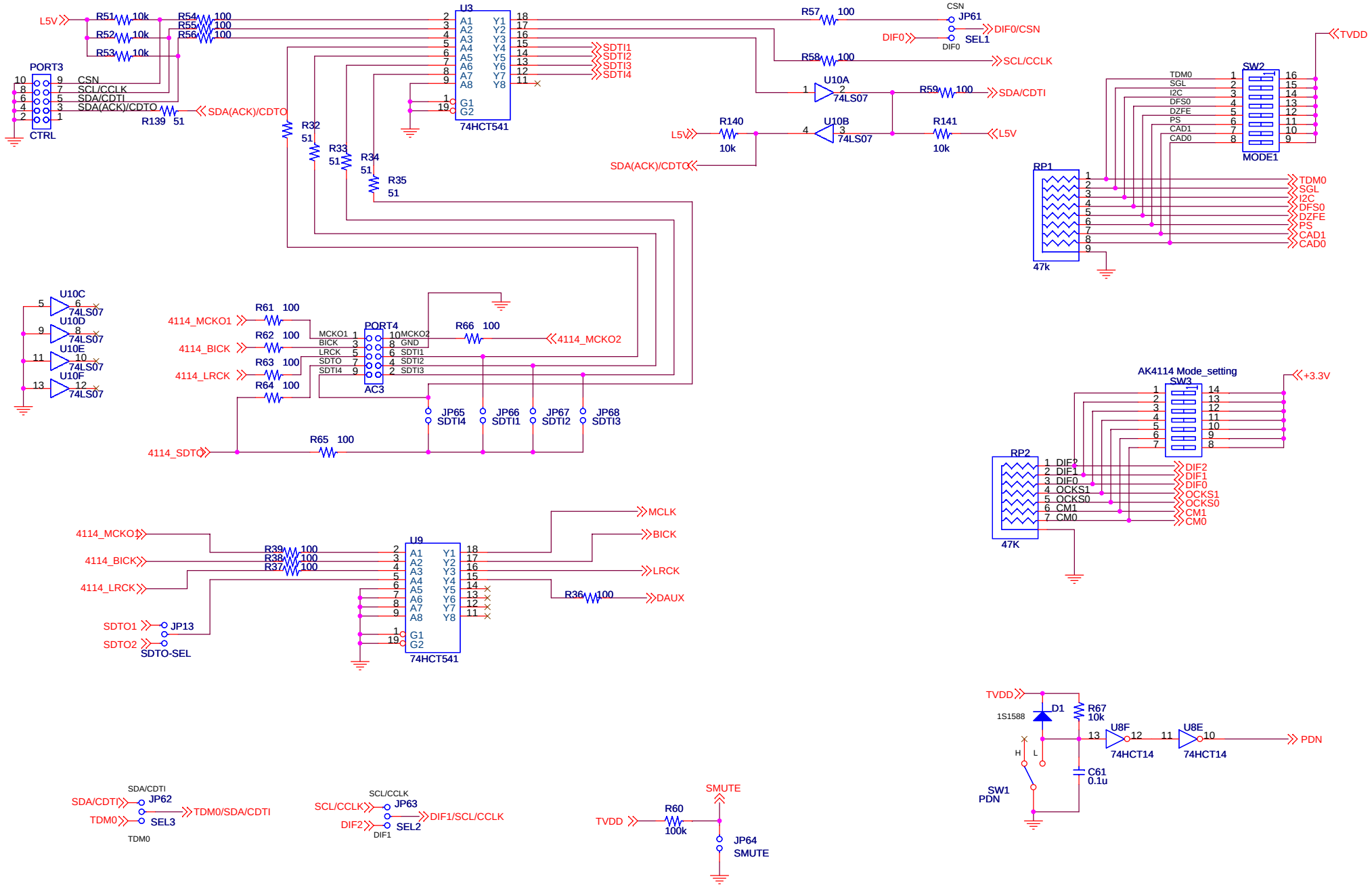
Date: Monday, December 21, 2009	Sheet 4 of 6		



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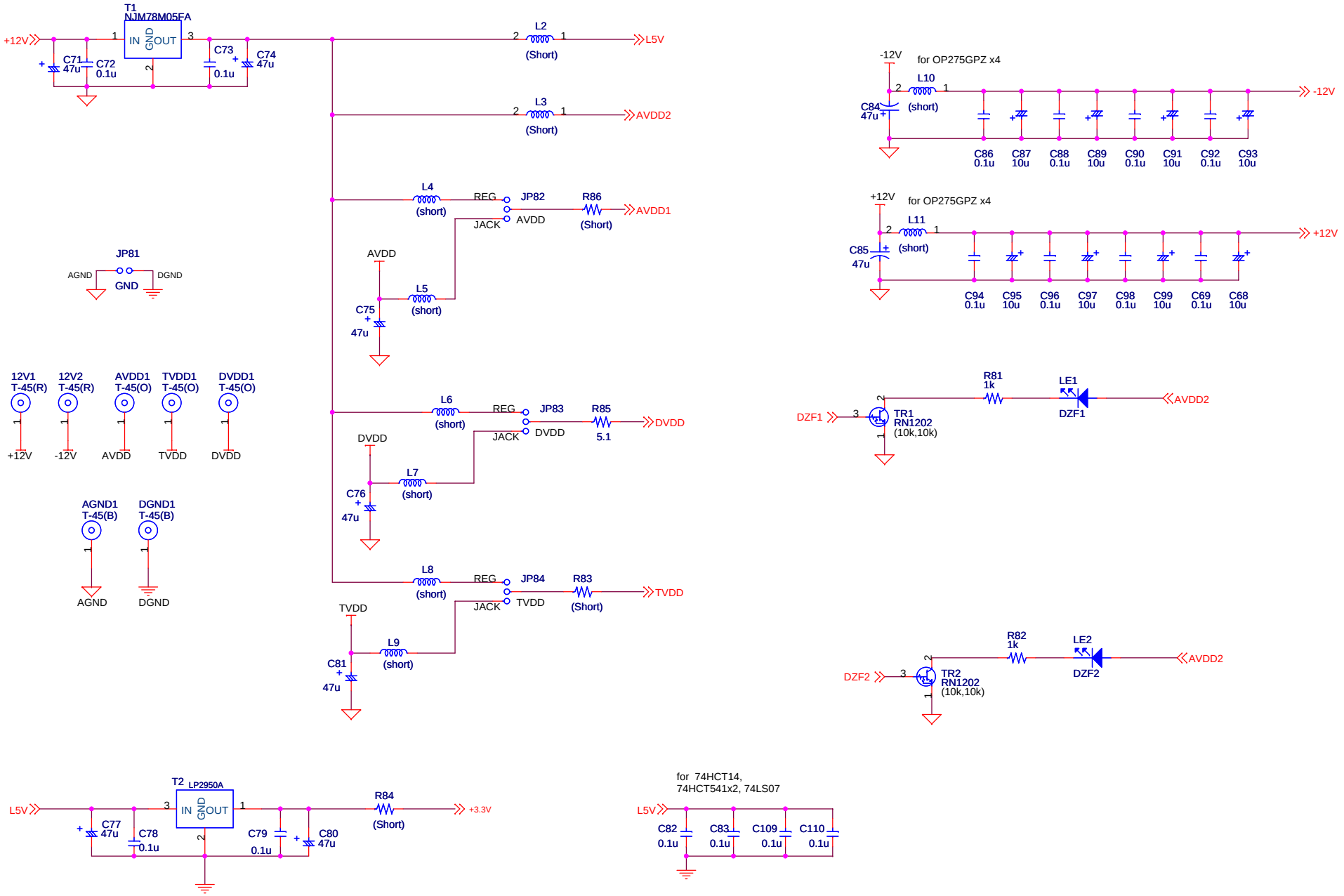
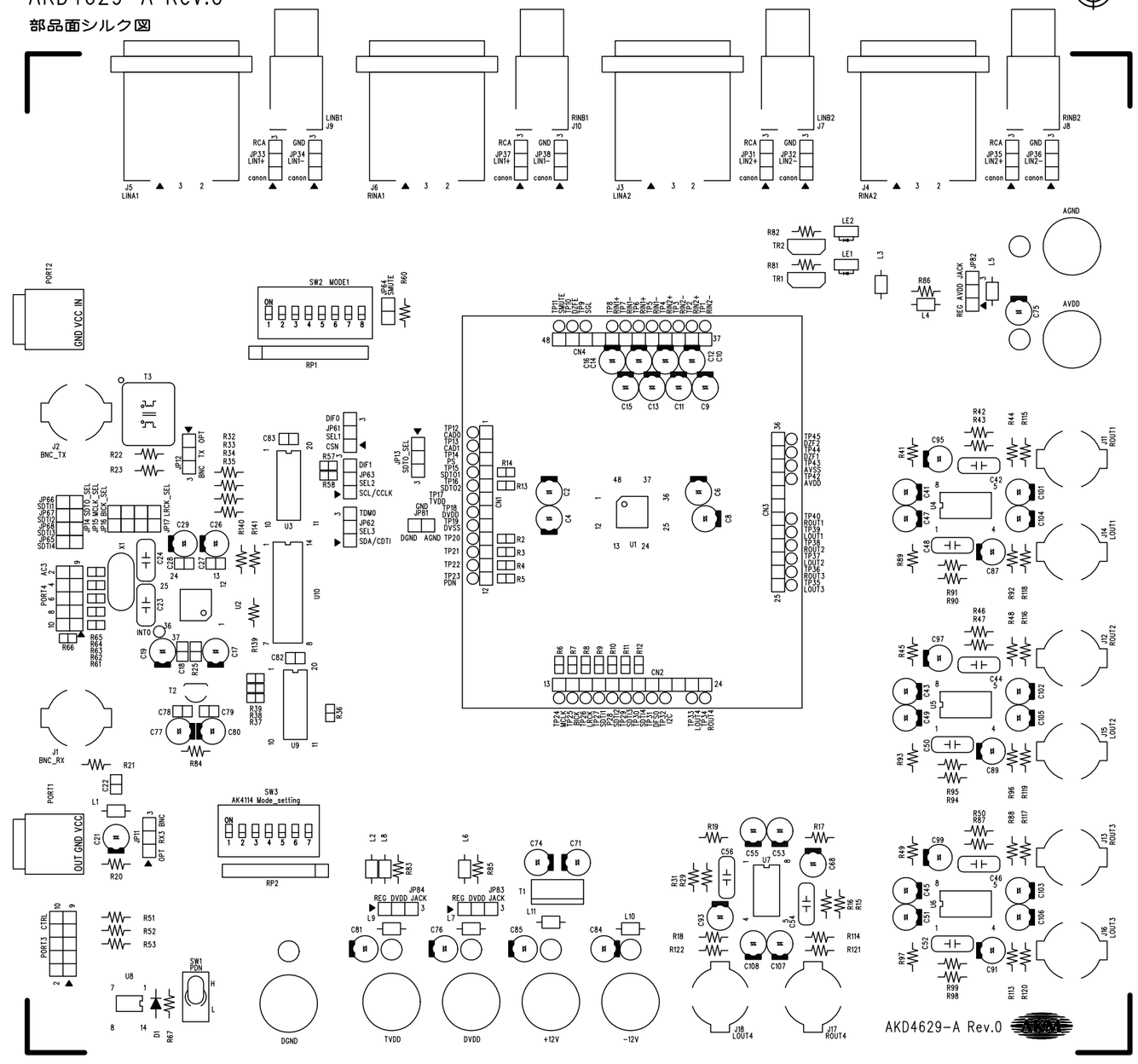
Size A3	Document Number <Doc> Digital I/F		Rev 0
Date: Wednesday, August 04, 2010	Sheet 5 of 6		



Title	<Title>	AKD4629-A-MAIN
Size A3	Document Number <Doc>	Power Supply
Date: Thursday, July 01, 2010	Sheet 6 of 6	Rev 0

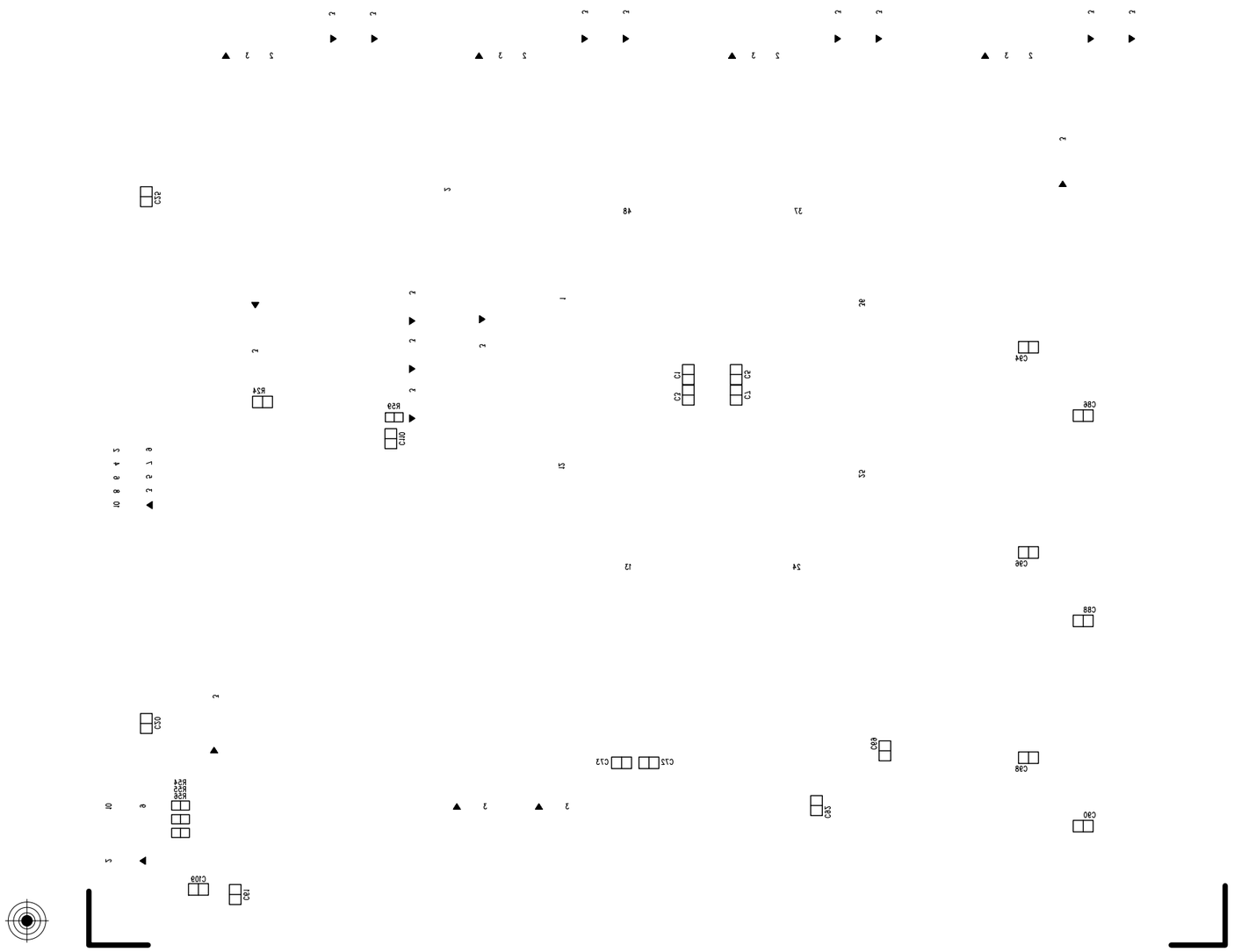
AKD4629-A Rev.0

部品面シルク図



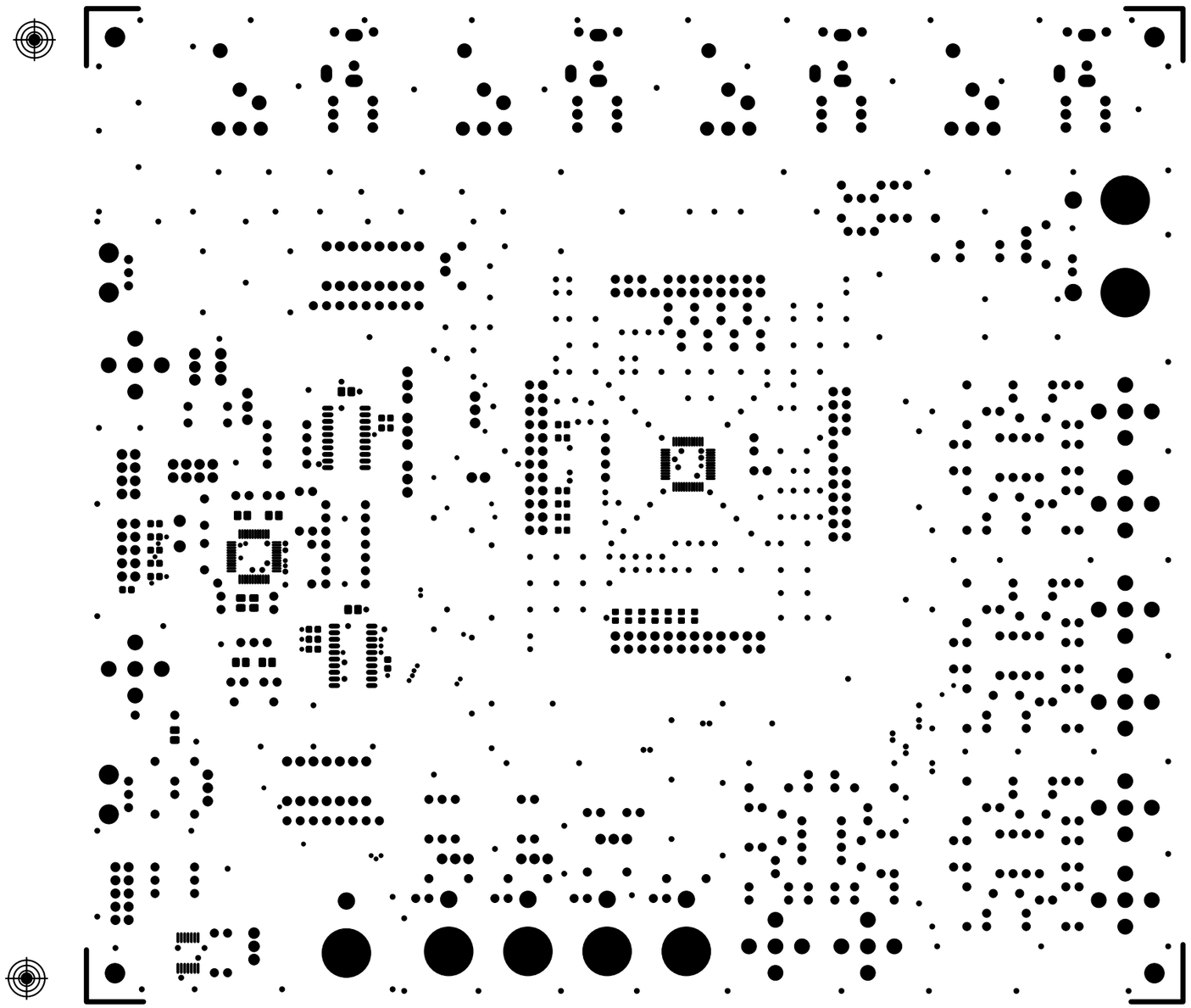
AKD4629-A Rev.0

半田面シルク図



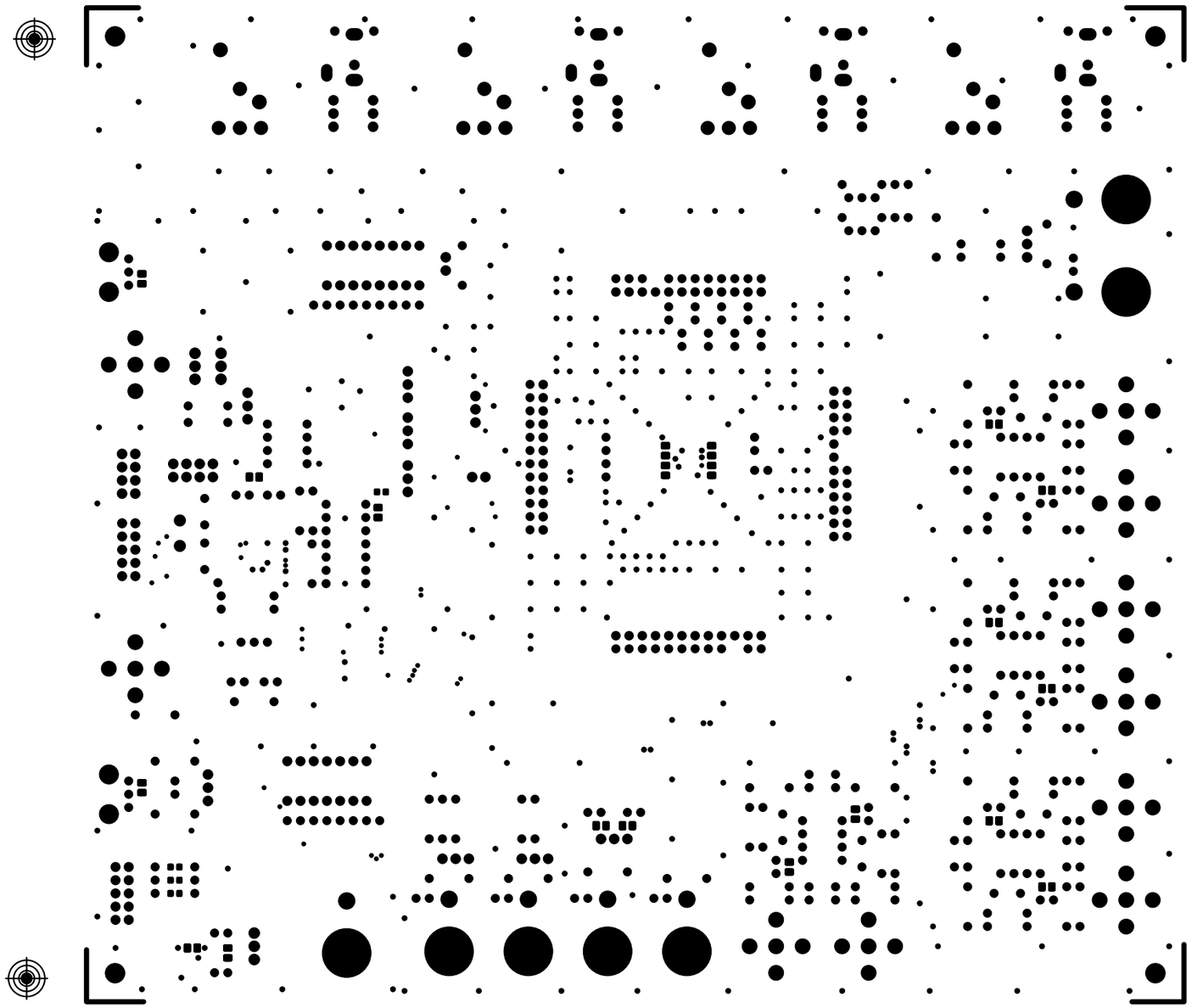
AKD4629-A Rev.0

部品面レジスト 図



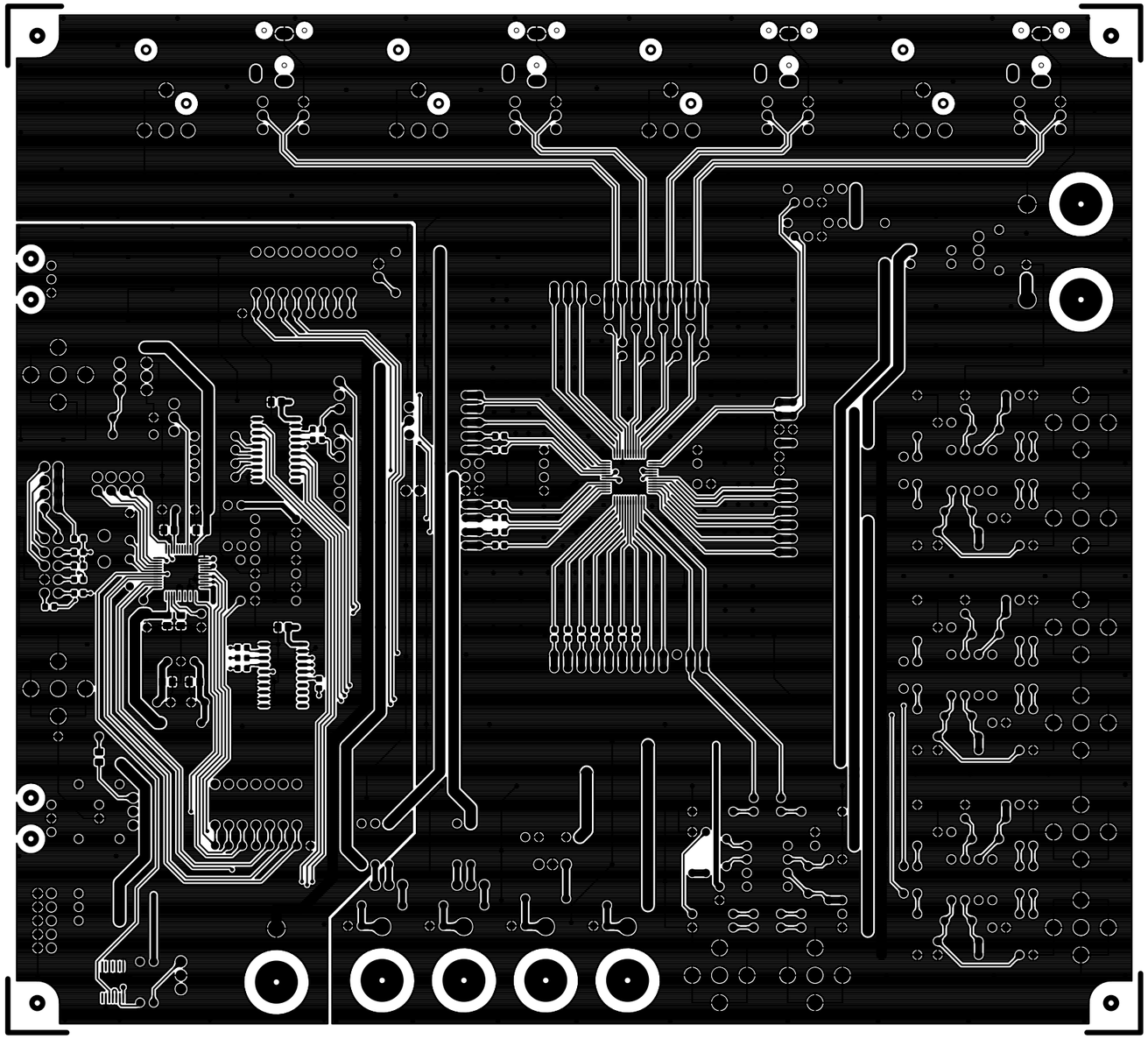
AKD4629-A Rev.0

半田面レジスト図



AKD4629-A Rev.0

部品面パターン図



AKD4629-A Rev.0

半田面パターン図