AKD4645A-A
Evaluation board Rev.1 for AK4645A

GENERAL DESCRIPTION

AKD4645A is an evaluation board for the AK4645A, stereo CODEC with built-in MIC/HP amplifier. The AKD4645A can evaluate A/D converter and D/A converter separately in addition to loopback mode (A/D → D/A). The AKD4645A also has the digital audio interface and can achieve the interface with digital audio systems via opt-connector.

■ Ordering guide

AKD4645A --- Evaluation board for AK4645A
(Cable for connecting with printer port of IBM-AT,compatible PC and control software are packed with this. This control software does not support Windows NT.)

FUNCTION

- **DIT/DIR with optical input/output**
- **BNC connector for an external clock input**
- **10pin Header for serial control mode**

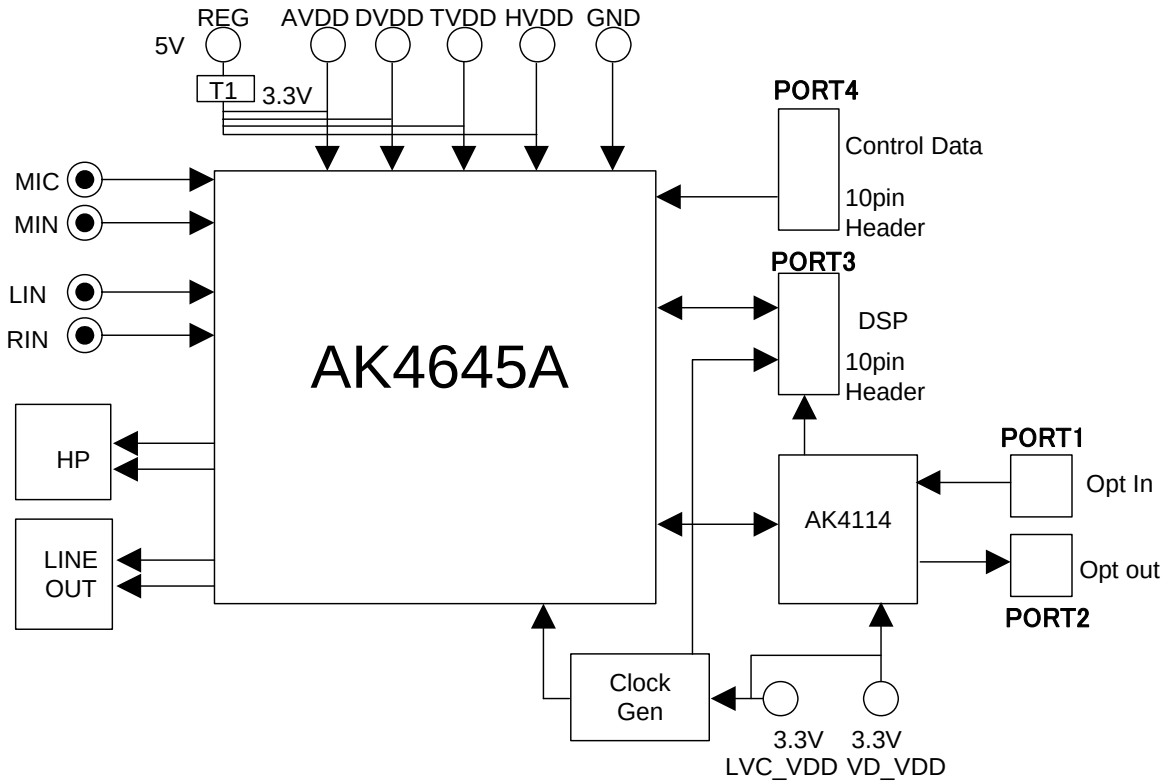


Figure 1. AKD4645A Block Diagram

* Circuit diagram and PCB layout are attached at the end of this manual

Board Outline Chart

■ Outline Chart

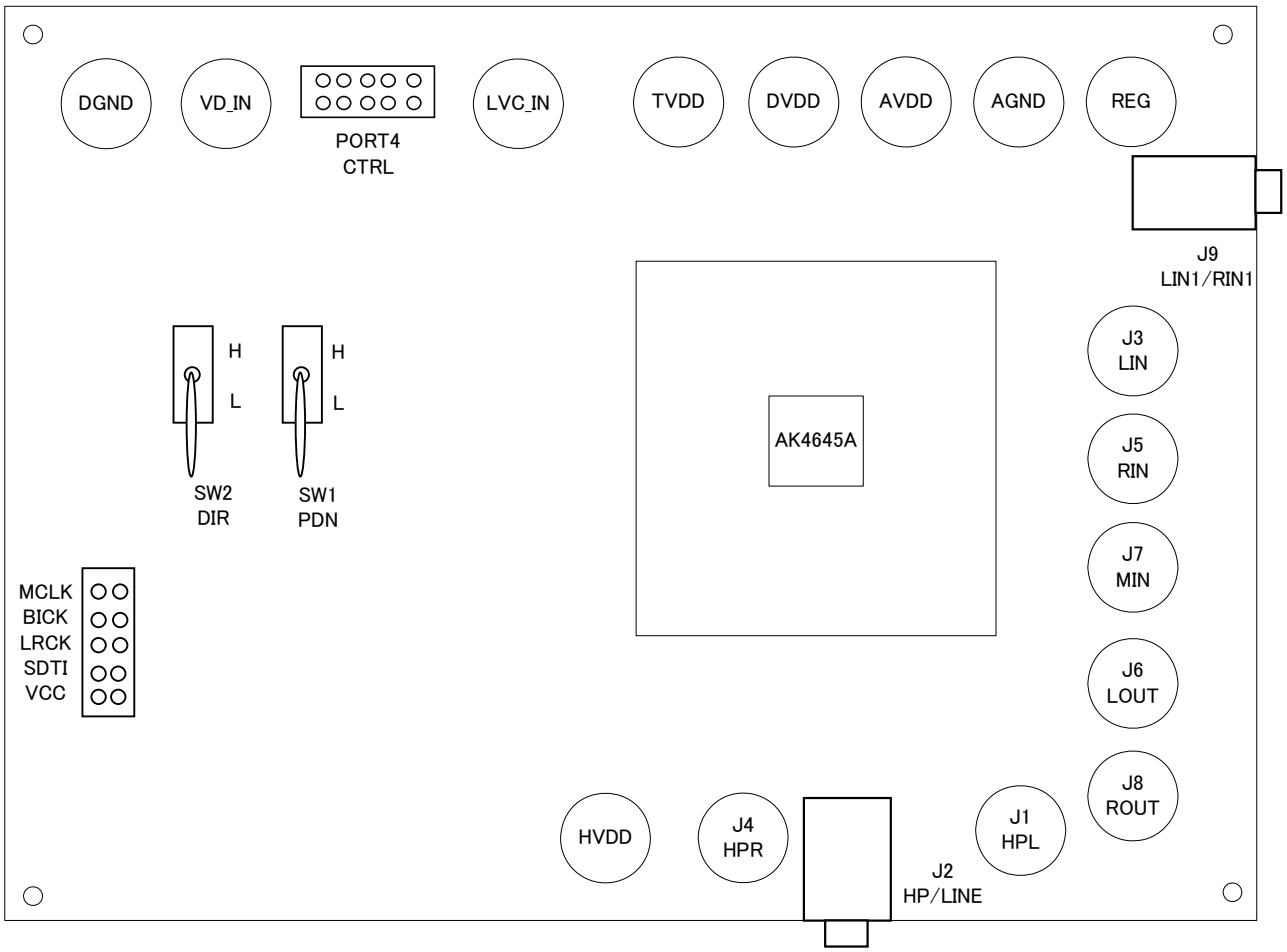


Figure 2. AKD4645A Outline Chart

■ Operation sequence

1) Set up the power supply lines.

[AVDD]	(orange)	= 2.6 ~ 3.6V	: for AVDD of AK4645A (typ. 3.3V)
[HVDD]	(orange)	= 2.6 ~ 5.25V	: for HVDD of AK4645A (typ. 3.3/5.0V)
[DVDD]	(orange)	= 2.6 ~ 3.6V	: for DVDD of AK4645A (typ. 3.3V:=AVDD±0.3V)
[TVDD]	(orange)	= 1.6 ~ 3.6V	: for TVDD of AK4645A (typ. 3.3V:≤DVDD)
[LVC_IN]	(orange)	= 1.6 ~ 3.6V	: for logic (typ. 3.3V:=TVDD)
[VD_IN]	(orange)	= 2.7 ~ 3.6V	: for AK4114 and logic (typ. 3.3V)
[REG]	(red)	= 5.0V	: for regulator (typ. 5.0V)
[AGND]	(black)	= 0V	: for analog ground
[DGND]	(black)	= 0V	: for logic ground

Each supply line should be distributed from the power supply unit.

2) Set up the evaluation mode, jumper pins and DIP switches. (See the followings.)

3) Power on.
The AK4645A and AK4114 should be reset once bringing SW1 and SW2 "L" upon power-up.

■ Evaluation mode

(1) External Slave Mode

In case of AK4645A evaluation using AK4114, it is necessary to correspond to audio interface format for AK4645A and AK4114. About AK4645A's audio interface format, refer to datasheet of AK4645A. About AK4114's audio interface format, refer to **Table 1** in this manual.

(1-1) Evaluation of Recording block (MIC, ADC) using DIT of AK4114 **<default>**
(1-2) Evaluation of Playback block (HP, LINEOUT) using DIR of AK4114
(1-3) Evaluation of Loop-back using AK4114
(1-4) All interface signals including master clock are fed externally.

(1-1) Evaluation of Recording block (MIC, ADC) using DIT of AK4114 <default>

PORT2 (DIT) and X1 (X'tal) are used. DIT generates audio bi-phase signal from received data and which is output through optical connector (TOTX141). Nothing should be connected to PORT1 (DIR) and PORT3 (DSP) and J11 (EXT). The jumper pins should be set to the following.

JP name	State	JP name	State
JP25(EXT)	Short	JP32(BICK_SEL)	Short
JP26(4114_MCKI_IN)	Open	JP33(LRCK_SEL)	Short
JP27(4114BICK_SEL)	Open	JP35(LRCK_MODE)	Open
JP28(4114LRCK_SEL)	Open	JP36(BICK_MODE)	Open

When AK4114 is used, JP22 (MKFS) and JP23 (BCFS) are not used. Therefore, JP22 (MKFS) should be set to "x1" and JP23 (BCFS) should be set to "64fs".

* The AK4114 operates at fs of 32kHz or more. If the fs is slower than 32kHz, this evaluation mode can't be used.

(1-2) Evaluation of Playback block (HP, LINEOUT) using DIR of AK4114

PORT1 (DIR) is used. Nothing should be connected to PORT2 (DIT), PORT3 (DSP) and J11 (EXT). The jumper pins should be set to the following.

JP name	State	JP name	State
JP25(EXT)	Short	JP32(BICK_SEL)	Short
JP26(4114_MCKI_IN)	Open	JP33(LRCK_SEL)	Short
JP27(4114BICK_SEL)	Open	JP35(LRCK_MODE)	Open
JP28(4114LRCK_SEL)	Open	JP36(BICK_MODE)	Open

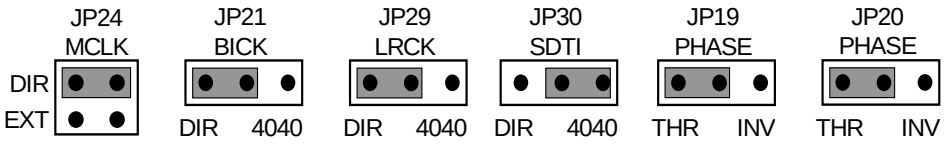
When AK4114 is used, JP22 (MKFS) and JP23 (BCFS) are not used. Therefore, JP22 (MKFS) should be set to "x1" and JP23 (BCFS) should be set to "64fs".

* The AK4114 operates at fs of 32kHz or more. If the fs is slower than 32kHz, this evaluation mode can't be used.

(1-3) Evaluation of Loop-back using AK4114

X'tal oscillator (X1) is used. Nothing should be connected to PORT1 (DIR), PORT3 (DSP) and J11 (EXT). The jumper pins should be set to the following.

JP name	State	JP name	State
JP25(EXT)	Short	JP32(BICK_SEL)	Short
JP26(4114_MCKI_IN)	Open	JP33(LRCK_SEL)	Short
JP27(4114BICK_SEL)	Open	JP35(LRCK_MODE)	Open
JP28(4114LRCK_SEL)	Open	JP36(BICK_MODE)	Open



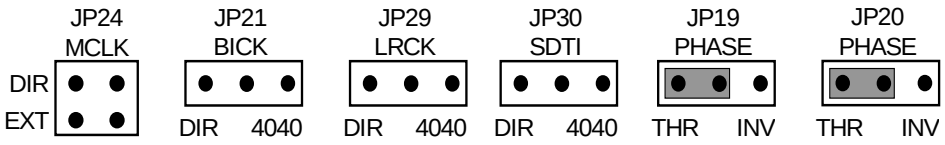
When AK4114 is used, JP22 (MKFS) and JP23 (BCFS) are not used. Therefore, JP22 (MKFS) should be set to "x1" and JP23 (BCFS) should be set to "64fs".

* The AK4114 operates at fs of 32kHz or more. If the fs is slower than 32kHz, this evaluation mode can't be used.

(1-4) All interface signals including master clock are fed externally.

PORT3 (ROM) is used. Nothing should be connected to PORT1 (DIR), PORT2 (DIT), and J11 (EXT). The jumper pins should be set to the following. Please set SW2= "L"

JP name	State	JP name	State
JP25(EXT)	Short	JP32(BICK_SEL)	Short
JP26(4114_MCKI_IN)	Open	JP33(LRCK_SEL)	Short
JP27(4114BICK_SEL)	Open	JP35(LRCK_MODE)	Open
JP28(4114LRCK_SEL)	Open	JP36(BICK_MODE)	Open



When AK4114 is used, JP22 (MKFS) and JP23 (BCFS) are not used. Therefore, JP22 (MKFS) should be set to "x1" and JP23 (BCFS) should be set to "64fs".

JP20 (PHASE) is jumper which decides polarity of BICK, "THR" or "INV" should be selected according to the audio interface format.

■ DIP Switch set up

[S1] : Mode Setting of AK4114 and AK4645A
ON is "H", OFF is "L".

No.	Name	ON ("H")	OFF ("L")	default
1	DIF0	AK4114 Audio Format Setting See Table 2		OFF
2	DIF1			OFF
3	DIF2			ON
4	OCKS1	AK4114 Master Clock Setting See Table 3		OFF
5	CAD0	See Table 4		OFF
6	I2C			OFF

Table 1. Mode Setting for AK4645A and AK4114

DIF2	DIF1	DIF0	AK4114DAUX	AK4114SDTO	LRCK		BICK		
						I/O		I/O	
0	0	0	24bit, Left justified	16bit, Right justified	H/L	O	64fs	O	
0	0	1	24bit, Left justified	18bit, Right justified	H/L	O	64fs	O	
0	1	0	24bit, Left justified	20bit, Right justified	H/L	O	64fs	O	
0	1	1	24bit, Left justified	24bit, Right justified	H/L	O	64fs	O	
1	0	0	24bit, Left justified	24bit, Left justified	H/L	O	64fs	O	**<default>**
1	0	1	24bit, I^2S	24bit, I^2S	L/H	O	64fs	O	
1	1	0	24bit, Left justified	24bit, Left justified	H/L	I	64-128fs	I	
1	1	1	24bit, I^2S	24bit, I^2S	L/H	I	64-128fs	I	

Table 2. Setting for AK4114 Audio Interface Format

OCKS1	X'tal
0	256fs
1	512fs

<default>

Table 3. AK4114 Master Clock Setting

■ Other jumper pins set up

[JP1] (GND) : Analog ground and Digital ground
OPEN : Separated.
SHORT : Common. (The connector "DGND" can be open.) **<default>**

[JP2] : Selection of MIN path or LIN3 path
MIN : MIN path (**AIN3 bit="0"** : Register Address 21H)
LIN3 : LIN3 path (**AIN3 bit="1"** : Register Address 21H)

[JP5, 4] : Selection of using MIC-power supply for L/RIN1 path
SHORT : MIC-power is supplied.
OPEN : MIC-power is not supplied. **<default>**

[JP3,6,7,8] : power AVDD,DVDD,HVDD,TVDD
short : for regulator (typ. 5.0V)**<default>**
open : Separated.

[JP11] (HPL) : Analog Output
BNC: Output from J1. **<default>**
HP: Output from J2.

[JP12] (LIN-SEL): Analog Input
LIN2: LIN2 Input.**<default>**
LIN3: LIN3 Input.
LIN4: LIN4 Input.

[JP13] (HPR) : Analog Output
BNC: Output from J4. **<default>**
HP: Output from J2.

[JP14] (RIN-SEL): Analog Input
LIN2 : RIN2 Input.**<default>**
LIN3: RIN3 Input.
LIN4: RIN4 Input

[JP15] (LOUT-SEL) : Analog Output
BNC: Output from J6. **<default>**
Mini-Jack: Output from J2.

[JP16] (ROUT-SEL) : Analog Output
BNC: Output from J8**<default>**
Mini-Jack: Output from J2.

[JP22] (MKFS) : MCLK Frequency
x1 : 256fs **<default>**
x2 : 512fs
x4 : 1024fs

[JP23] (BCFS) : BICK Frequency
32fs : 32fs frequency
64fs : 64fs frequency **<default>**

[JP31] (MODE_SEL) : Serial Control Interface
3-WIRE : 3-WIRE Serial Control Mode **<default>**
I2C : I^2C-bus Control Mode

[JP34] (DAUX_SEL): Presence of external device connection via PORT3(DSP)
SHORT : connection
OPEN : non-connection **<default>**

■ The function of the toggle SW

[SW1] (PDN): Power down of AK4645A. Keep "H" during normal operation.

[SW2] (DIR): Power down of AK4114. Keep "H" during normal operation.
Keep "L" when AK4114 is not used.

■ Indication for LED

[LED1] (ERF): Monitor INT0 pin of the AK4114. LED turns on when some error has occurred to AK4114.

■ Serial Control

The AK4645A can be controlled via the printer port (parallel port) of IBM-AT compatible PC. Connect PORT4 (CTRL) with PC by 10 wire flat cable packed with the AKD4645A.Table 4 shows switch and jumper settings for serial control.

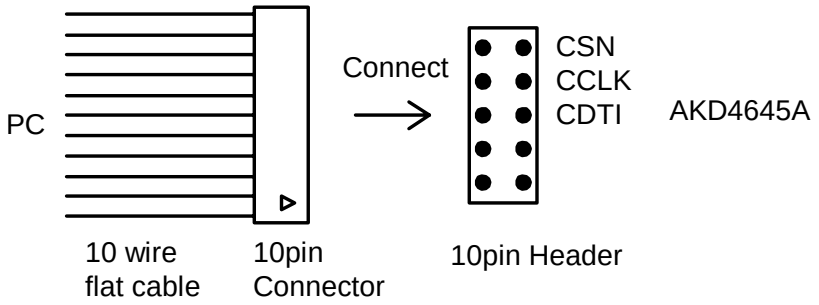


Figure 3. Connect of 10 wire flat cable

Mode		S1	
		I2C	CAD0
3-WIRE		OFF	OFF
I2C	CAD0=0	ON	OFF
	CAD0=1	ON	ON

Table 4. Serial Control Setting

■ Analog Input/Output Circuits

(1) Input Circuits

(1-1) LIN1/RIN1, LIN2/RIN2, LIN3/RIN3, LIN4/RIN4 Input Circuit

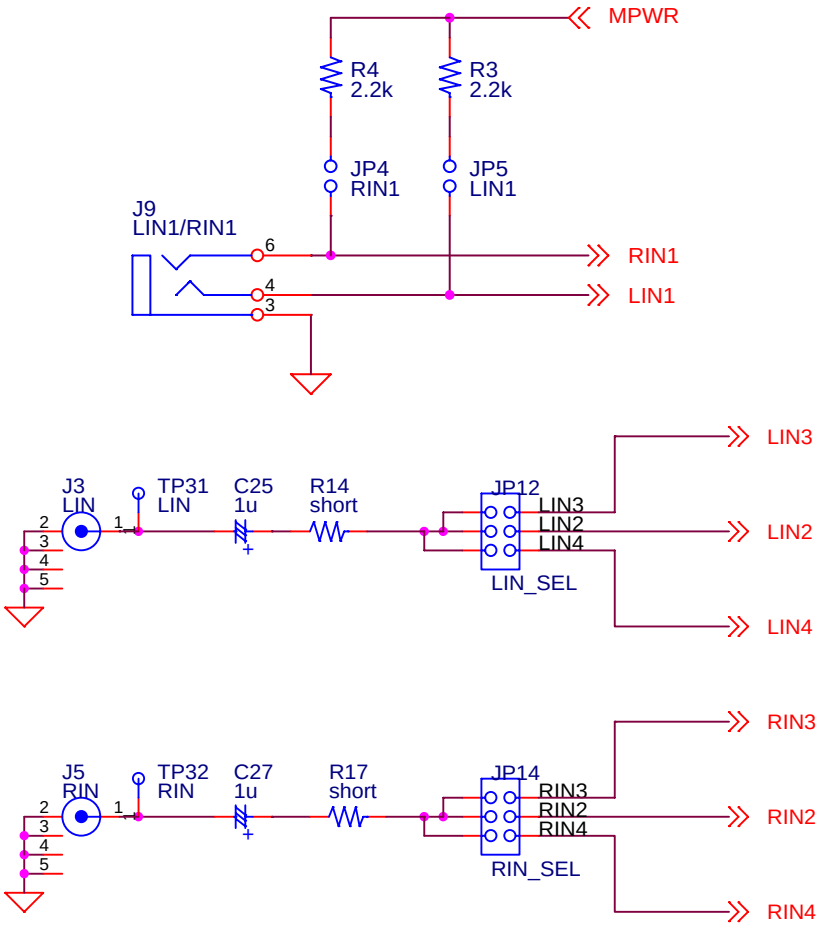
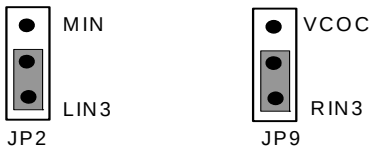


Figure 4. LIN1/RIN1, LIN2/RIN2, LIN3/RIN3, LIN4/RIN4 Input Circuit

LIN2/RIN2, LIN3/RIN3, LIN4/RIN4 shares J3/J5.
JP12(LIN_SEL) and JP14(RIN_SEL) select each path.

When LIN3/RIN3 paths of AK4645A are used, JP2 and JP9 should be set as below.
AIN3bit =“1” (Register Address 21H)



When microphone is connected to J9, JP4 and JP5 should be short.

(1-2) MIN Input Curcuits

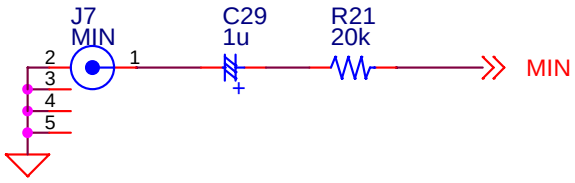
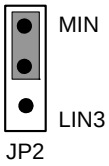


Figure 5 . MIN Input Circuit

When MIN Input path of AK4645A is used, JP2 should be set as below.
AIN3bit =“0” (Register Address 21H)



(2) Output Circuits

(2-1) HP Output Circuit

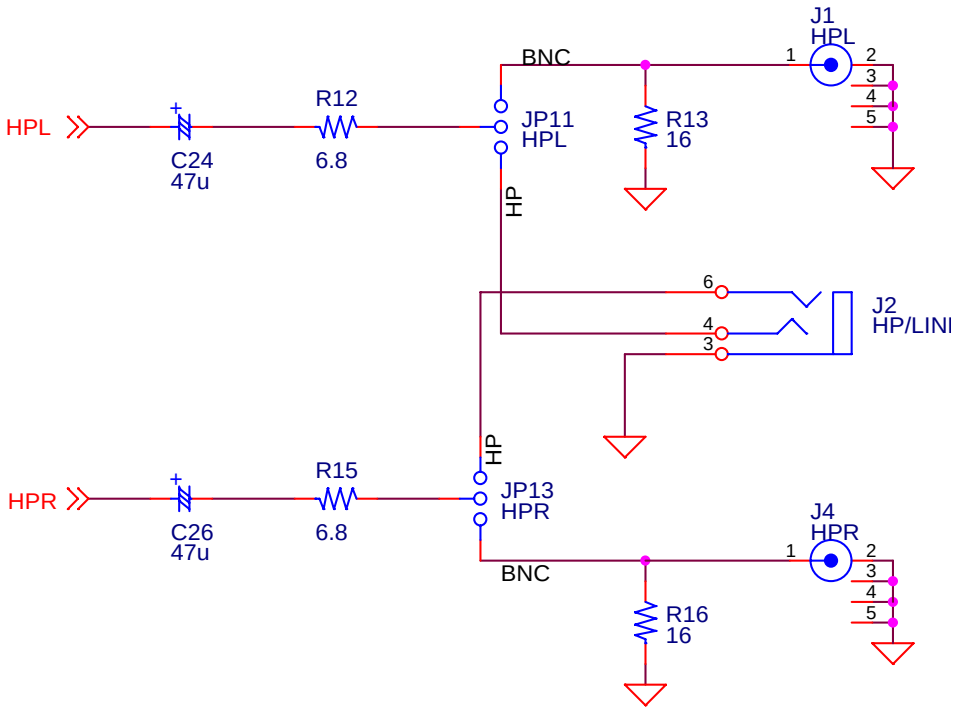
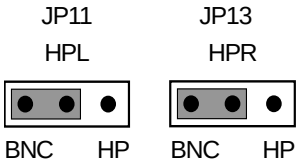
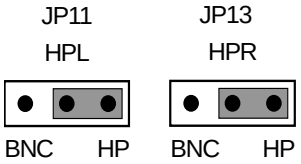


Figure 6 . HP Output Circuit

(2-1-1) In case that signal is output from J1 and J4.



(2-1-2) In case that signal is output from J2.



(2-2) LOUT/ROUT(LOP/LON) Output Circuit

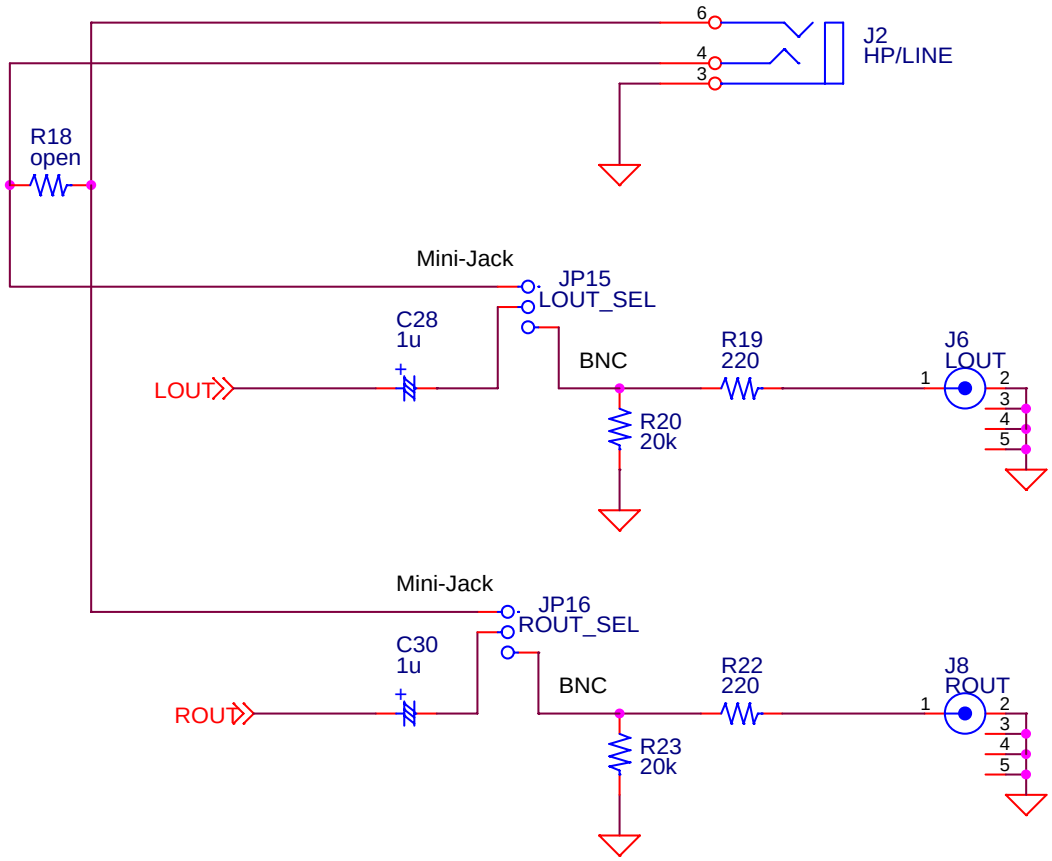
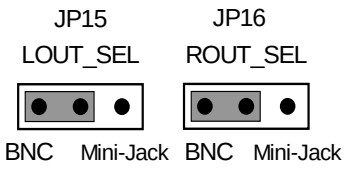
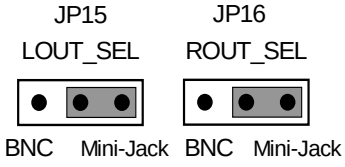


Figure 7 . LOUT/ROUT(LOP/LON) Output Circuit

(2-1-1) In case that signal is output from J6 and J8.



(2-1-1) In case that signal is output from J2.



∗ AKM assumes no responsibility for the trouble when using the above circuit examples.

Control Software Manual

■ Set-up of evaluation board and control software

1. Set up the AKD4645A-A according to previous term.

2. Connect IBM-AT compatible PC with AKD4645A-A by 10-line type flat cable (packed with AKD4645A-A). Take care of the direction of 10pin header. (Please install the driver in the CD-ROM when this control software is used on Windows 2000/XP. Please refer “Installation Manual of Control Software Driver by AKM device control software”. In case of Windows95/98/ME, this installation is not needed. This control software does not operate on Windows NT.)

3. Insert the CD-ROM labeled “AK4645A-A Evaluation Kit” into the CD-ROM drive.

4. Access the CD-ROM drive and double-click the icon of “AKD4645A.exe” to set up the control program.

5. Then please evaluate according to the follows.

■ Operation flow

Keep the following flow.

1. Set up the control program according to explanation above.
2. Click “Port Reset” button.

■ Explanation of each buttons

[Port Reset]	Set up the USB interface board (AKDUSBIF-A) .
[Write default] :	Initialize the register of AK4645A.
[All Write] :	Write all registers that is currently displayed.
[Function1] :	Dialog to write data by keyboard operation.
[Function2] :	Dialog to write data by keyboard operation.
[Function3] :	The sequence of register setting can be set and executed.
[Function4] :	The sequence that is created on [Function3] can be assigned to buttons and executed.
[Function5]:	The register setting that is created by [SAVE] function on main window can be assigned to buttons and executed.
[SAVE] :	Save the current register setting.
[OPEN] :	Write the saved values to all register.
[Write] :	Dialog to write data by mouse operation.
[Filter] :	Set Programmable Filter (FIL1, FIL3, EQ) of AK4645A easily.

■ Indication of data

Input data is indicated on the register map. Red letter indicates “H” or “1” and blue one indicates “L” or “0”. Blank is the part that is not defined in the datasheet.

■ Explanation of each dialog

1. [Write Dialog]: Dialog to write data by mouse operation

There are dialogs corresponding to each register.

Click the [Write] button corresponding to each register to set up the dialog. If you check the check box, data becomes "H" or "1". If not, "L" or "0".

If you want to write the input data to AK4645A, click [OK] button. If not, click [Cancel] button.

2. [Function1 Dialog] : Dialog to write data by keyboard operation

Address Box: Input registers address in 2 figures of hexadecimal.
Data Box: Input registers data in 2 figures of hexadecimal.

If you want to write the input data to AK4645A, click [OK] button. If not, click [Cancel] button.

3. [Function2 Dialog] : Dialog to evaluate IVOL and DVOL

Address Box: Input registers address in 2 figures of hexadecimal.
Start Data Box: Input starts data in 2 figures of hexadecimal.
End Data Box: Input end data in 2 figures of hexadecimal.
Interval Box: Data is written to AK4645A by this interval.
Step Box: Data changes by this step.
Mode Select Box:

If you check this check box, data reaches end data, and returns to start data.
[Example] Start Data = 00, End Data = 09
Data flow: 00 01 02 03 04 05 06 07 08 09 09 08 07 06 05 04 03 02 01 00

If you do not check this check box, data reaches end data, but does not return to start data.
[Example] Start Data = 00, End Data = 09
Data flow: 00 01 02 03 04 05 06 07 08 09

If you want to write the input data to AK4645A, click [OK] button. If not, click [Cancel] button.

4. [Save] and [Open]

4-1. [Save]

Save the current register setting data. The extension of file name is “akr”.

(Operation flow)
(1) Click [Save] Button.
(2) Set the file name and push [Save] Button. The extension of file name is “akr”.

4-2. [Open]

The register setting data saved by [Save] is written to AK4645A. The file type is the same as [Save].

(Operation flow)
(1) Click [Open] Button.
(2) Select the file (*.akr) and Click [Open] Button.

5. [Function3 Dialog]

The sequence of register setting can be set and executed.

(1) Click [F3] Button.

(2) Set the control sequence.
Set the address, Data and Interval time. Set "-1" to the address of the step where the sequence should be paused.

(3) Click [Start] button. Then this sequence is executed.

The sequence is paused at the step of Interval="-1". Click [START] button, the sequence restarts from the paused step.

This sequence can be saved and opened by [Save] and [Open] button on the Function3 window. The extension of file name is "aks".

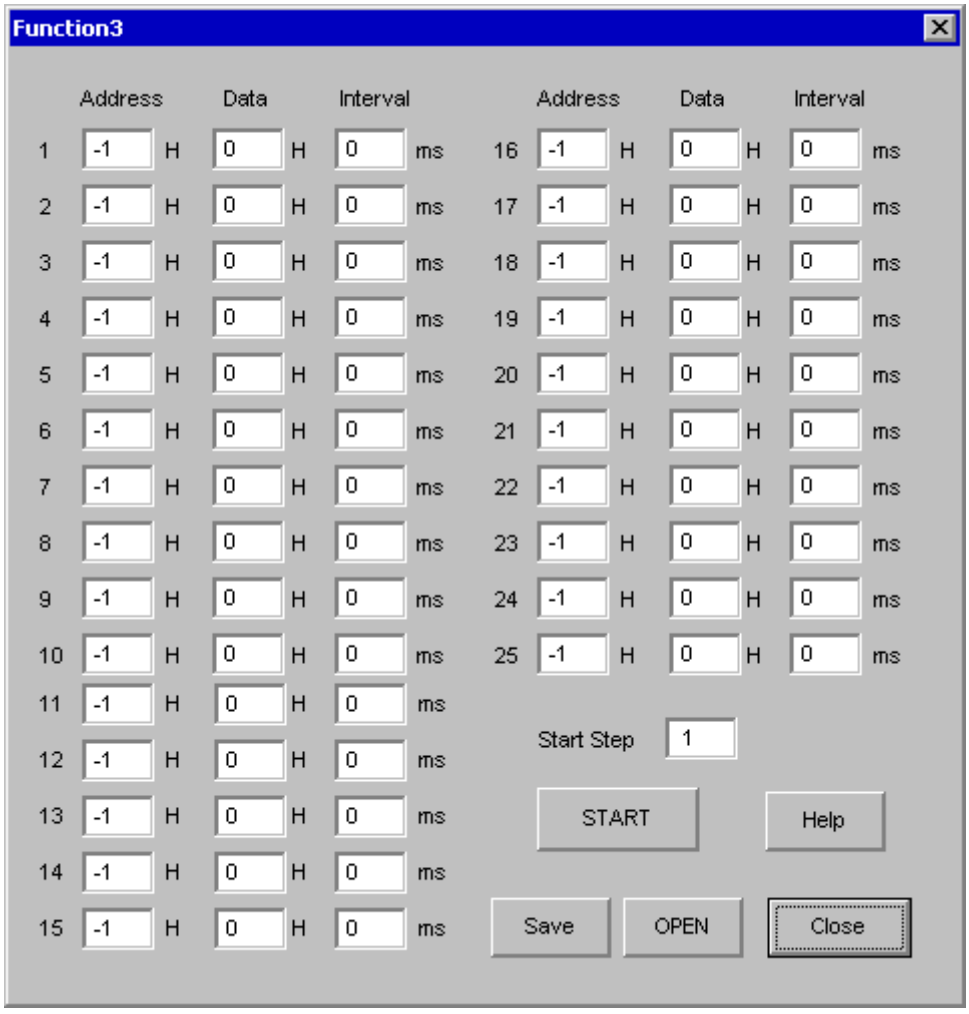


Figure 8. Window of [F3]

6. [Function4 Dialog]

The sequence that is created on [Function3] can be assigned to buttons and executed. When [F4] button is clicked, the window as shown in Figure 9 opens.

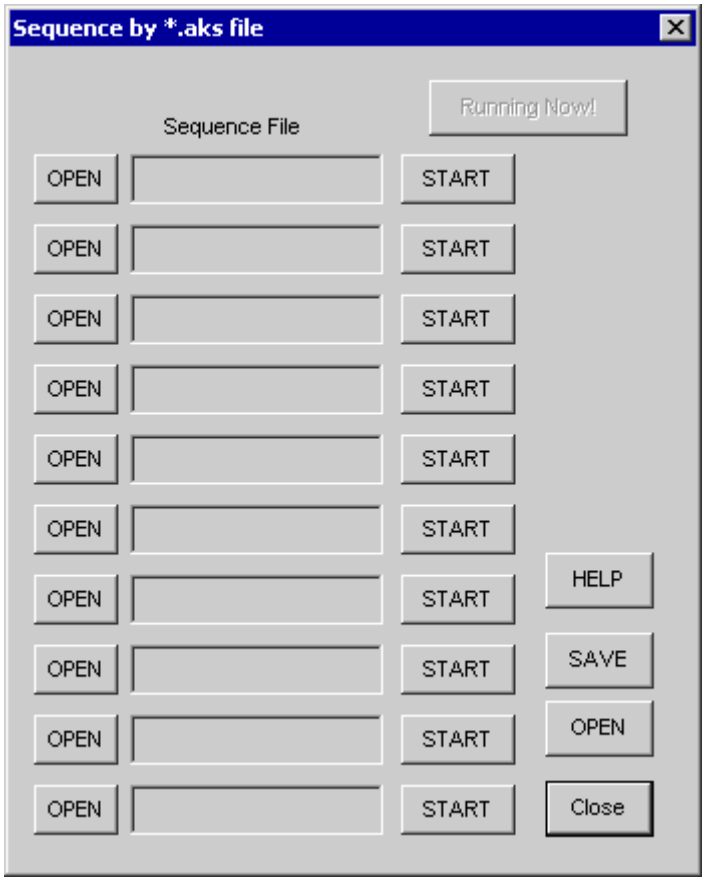


Figure 9. [F4] window

6-1. [OPEN] buttons on left side and [START] buttons

(1) Click [OPEN] button and select the sequence file (*.aks).

The sequence file name is displayed as shown in Figure 10.

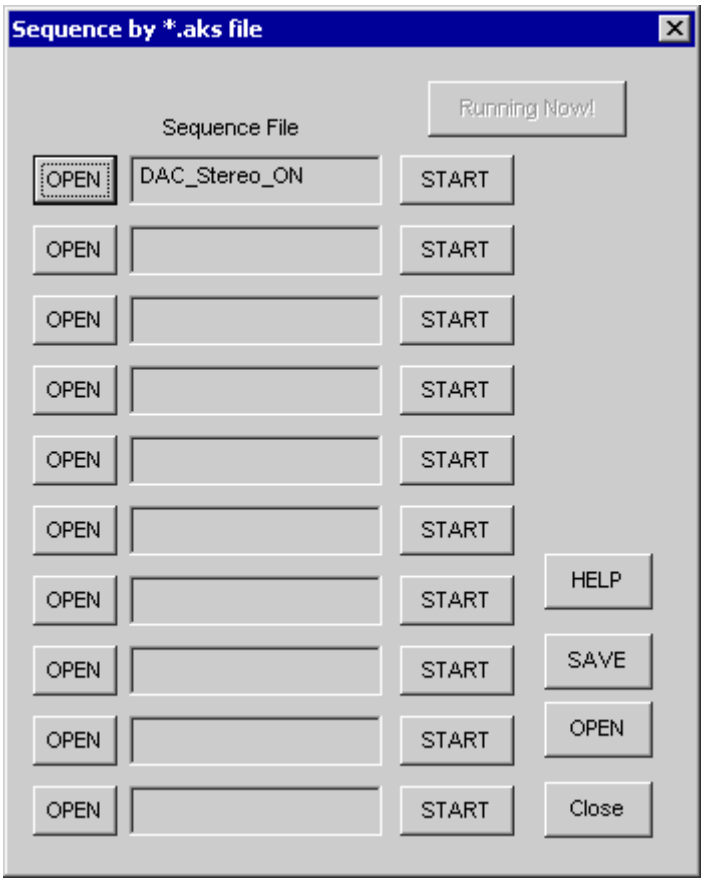


Figure 10. [F4] window(2)

(2) Click [START] button, then the sequence is executed.

3-2. [SAVE] and [OPEN] buttons on right side

[SAVE] : The sequence file names can assign be saved. The file name is *.ak4.

[OPEN] : The sequence file names assign that are saved in *.ak4 are loaded.

3-3. Note

(1) This function doesn't support the pause function of sequence function.

(2) All files need to be in same folder used by [SAVE] and [OPEN] function on right side.

(3) When the sequence is changed in [Function3], the file should be loaded again in order to reflect the change.

7. [Function5 Dialog]

The register setting that is created by [SAVE] function on main window can be assigned to buttons and executed. When [F5] button is clicked, the following window as shown in Figure 11 opens.

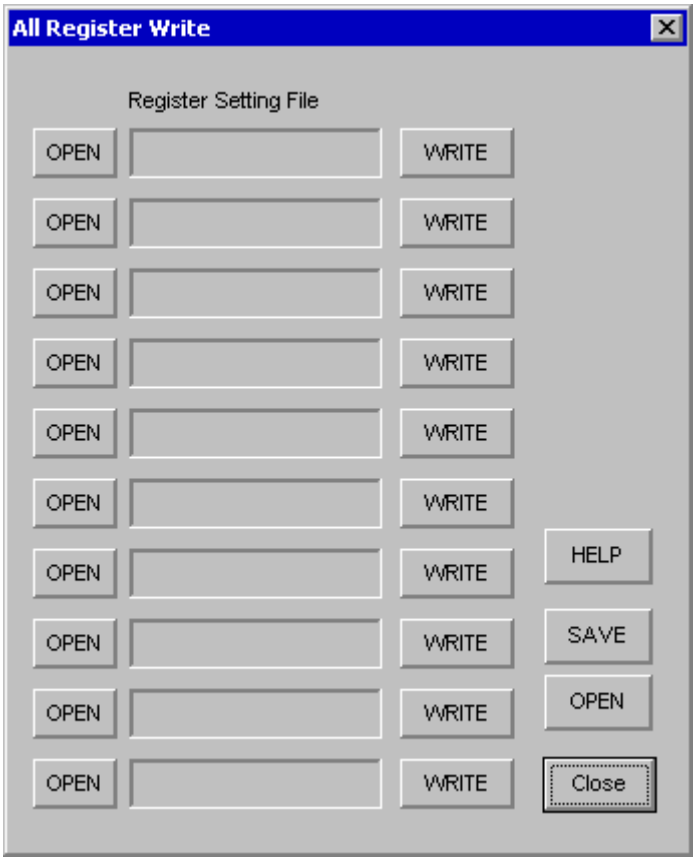


Figure 11. [F5] window

7-1. [OPEN] buttons on left side and [WRITE] button

(1) Click [OPEN] button and select the register setting file (*.akr).

The register setting file name is displayed as shown in Figure 12.

(2) Click [WRITE] button, then the register setting is executed.

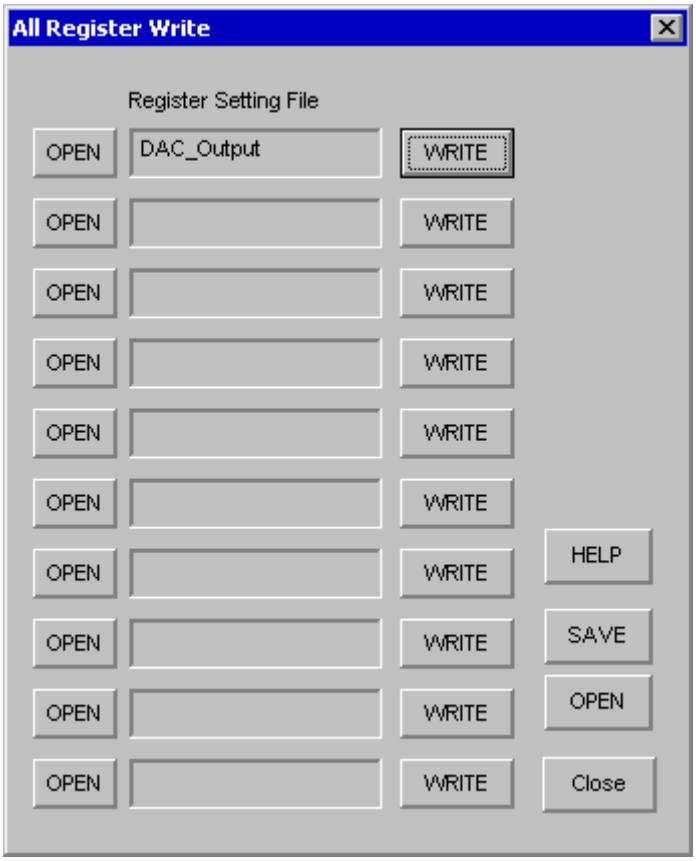


Figure 12. [F5] windows(2)

7-2. [SAVE] and [OPEN] buttons on right side

[SAVE] : The register setting file names assign can be saved. The file name is *.ak5.

[OPEN] : The register setting file names assign that are saved in *.ak5 are loaded.

7-3. Note

(1) All files need to be in same folder used by [SAVE] and [OPEN] function on right side.

(2) When the register setting is changed by [Save] Button in main window, the file should be loaded again in order to reflect the change.

8. [Filter Dialog]

This dialog can easily set the AK4645A's programmable filter.

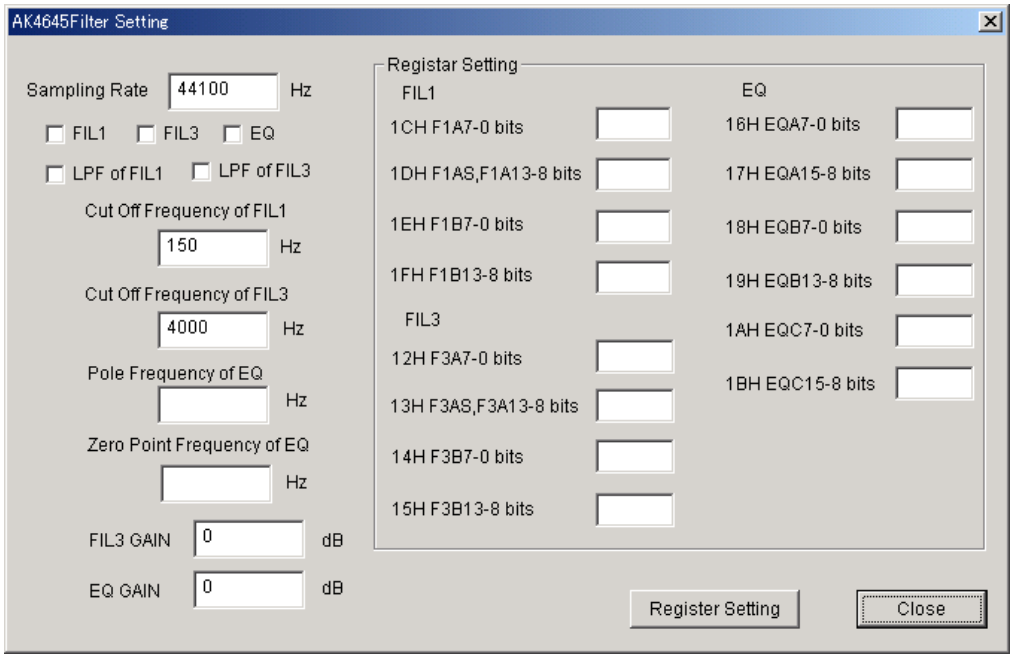


Figure 13 . [Filter] window

8-1. Value input columns on left side

[Sampling Rate] → Input value of sampling frequency [unit : Hz] <default : 44100>
[Cut Off Frequency of FIL1] → Input value of cut off frequency of FIL1 [unit : Hz] <default : 150>
[Cut Off Frequency of FIL3] → Input value of cut off frequency of FIL3 [unit : Hz] <default : 4000>
[Pole Frequency of EQ] → Input value of pole frequency of EQ [unit : Hz]
[Zero Frequency of EQ] → Input value of zero frequency of EQ [unit : Hz]
[FIL3 GAIN] → Input value of gain of FIL3 (0~−10dB) [unit : dB]
[EQ GAIN] → Input value of gain of EQ (+12~0dB) [unit : dB]

8-2. Check box on left side

Check Box	Check	Check off
FIL1	FIL1 bit =“1”	FIL1 bit =“0”
FIL3	FIL3 bit =“1”	FIL3 bit =“0”
EQ	EQ bit =“1”	EQ bit =“0”
LPF of FIL1	F1AS bit =“1”(LPF)	F1AS bit =“0”(HPF)
LPF of FIL3	F3AS bit =“1”(LPF)	F3AS bit =“0”(HPF)

8-2. [Register Setting] panel and [Register Setting] button on right side

Click [Register setting] button, then filter coefficient set by 8-1 and 8-2 is written on [Register setting] panel. (It is also written to the actual control register of the AK4645A.)

MEASUREMENT RESULTS

1. EXT mode (slave mode)

[Measurement condition]

- Measurement unit: Audio Precision, System two Cascade
- EXT Slave Mode
- MCLK: 256fs
- BICK: 64fs
- Bit: 16bit
- Measurement Frequency: 20Hz ~ 20kHz
- Power Supply: AVDD=DVDD=HVDD=TVDD=3.3V
- Temperature: Room
- Input Frequency: 1kHz
- Sampling Frequency: 44.1kHz

[Measurement Results]

ADC (LIN2/RIN2) characteristics (IVOL=0dB, ALC1 = OFF, LIN2/RIN2 → ADC → IVOL)

		L[dB]		R[dB]	
MIC-Amp Gain		0dB	+20dB	0dB	+20dB
S/(N+D)	20kHzLPF (−1dB)	90.1	84.1	89.7	83.7
DR	20kHzLPF + A-weighted	95.6	87.4	95.7	87.4
S/N	20kHzLPF + A-weighted	95.9	87.4	95.9	87.4

DAC (LOUT/ROUT) characteristics (R_L=20kΩ, DAC → LOUT/ROUT)

		L[dB]	R[dB]
S/(N+D)	20kHzLPF (−3dB)	88.7	88.9
S/N	20kHzLPF + A-weighted	94.3	94.1

DAC (HPL/ HPR) characteristics (R_L=22.8Ω, DAC → HPL/ HPR)

		L[dB]	R[dB]
S/(N+D)	20kHzLPF (−3dB)	66.8	67.3
S/N	20kHzLPF + A-weighted	91.3	91.4

2. PLOT DATA

2-1 ADC (LIN2/RIN2 → ADC) (0dB)

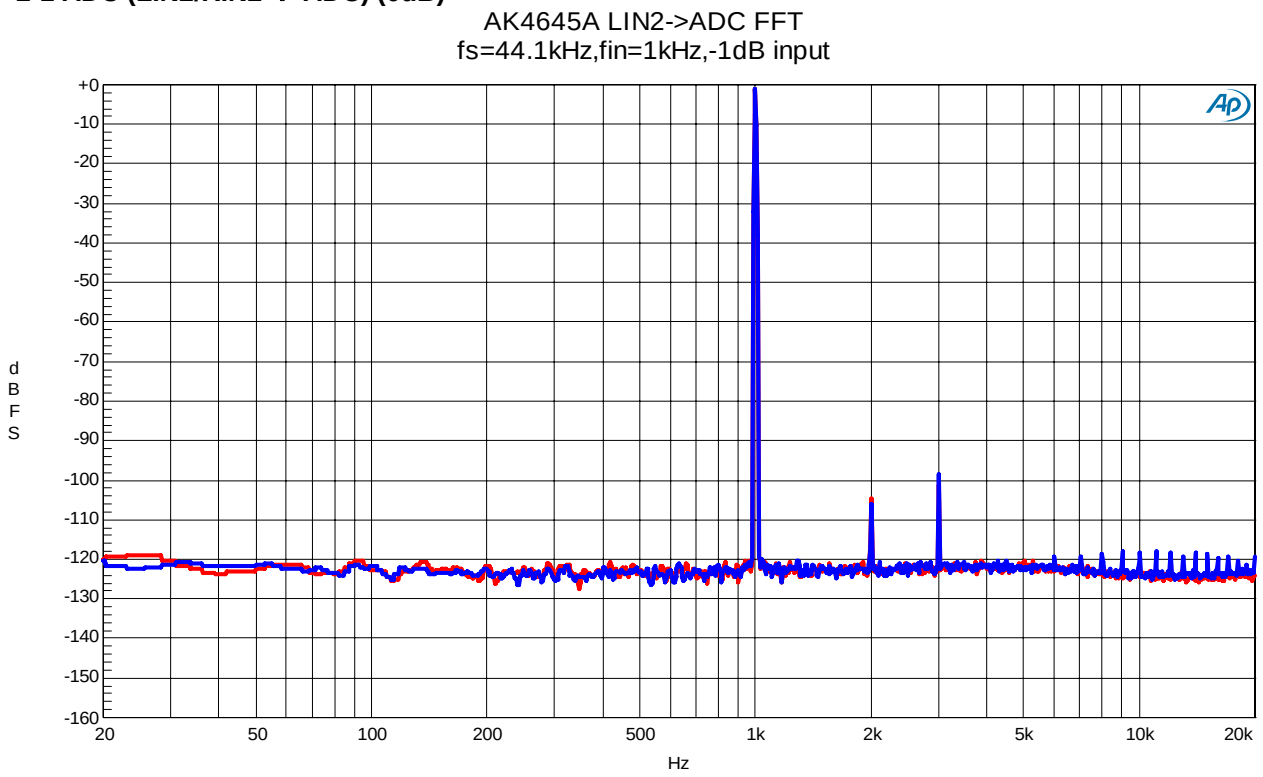


Figure 14. FFT Plot (Input level= 0dBFs)

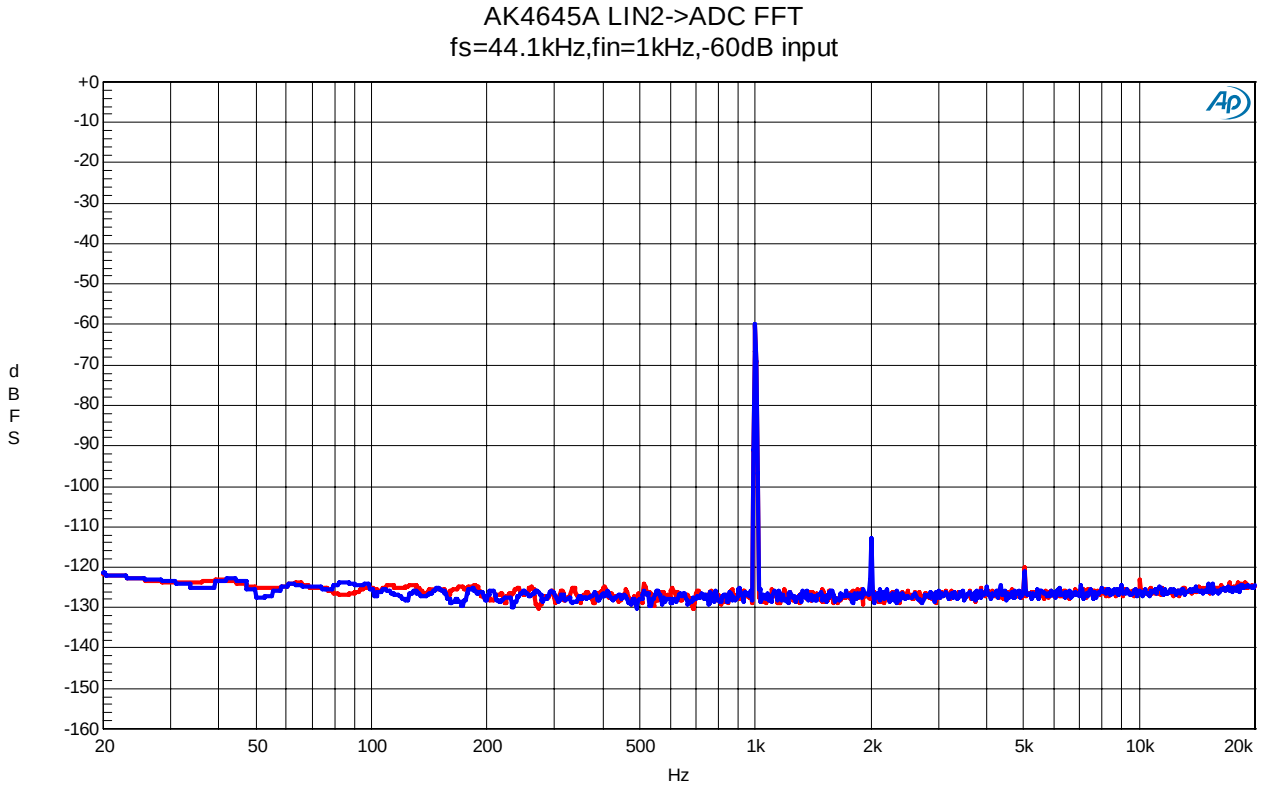


Figure 15. FFT Plot (Input level= -60dBFs)

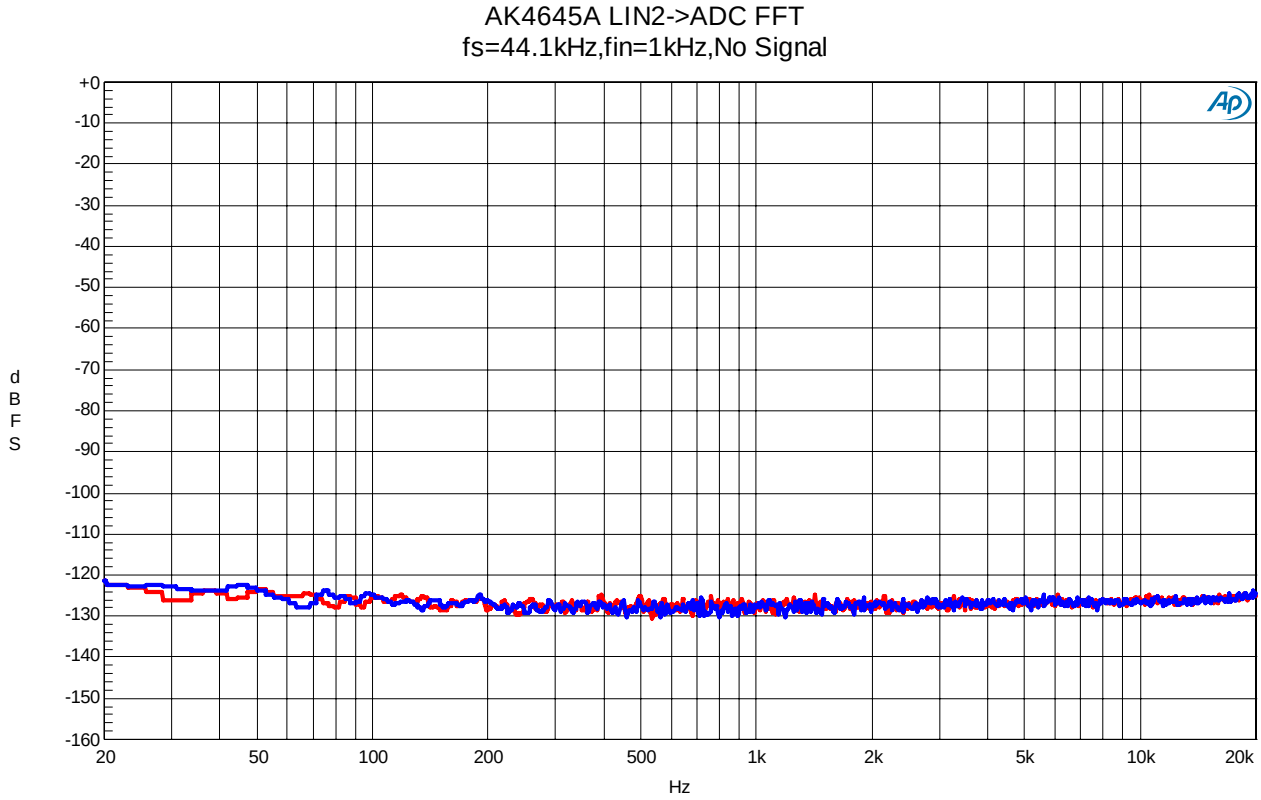


Figure 16. FFT Plot (No signal)

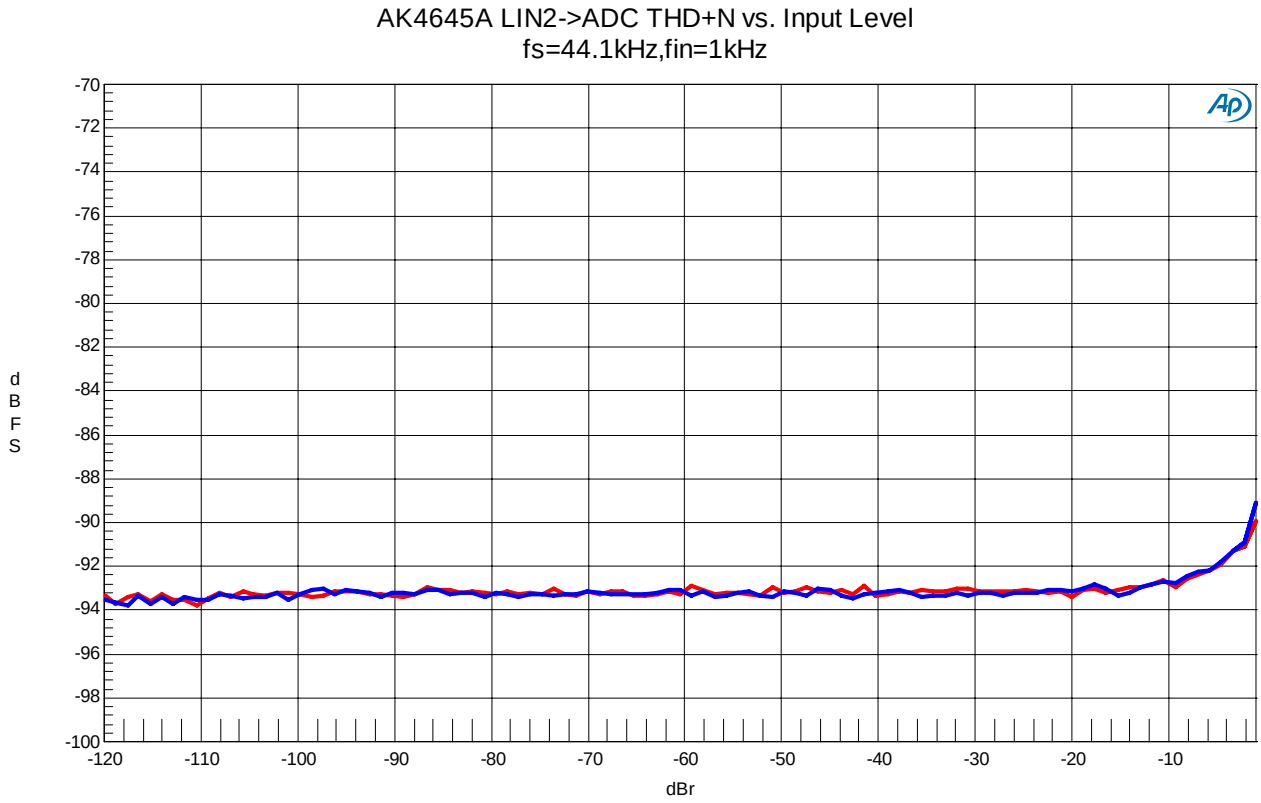


Figure 17. THD+N vs. Input Level

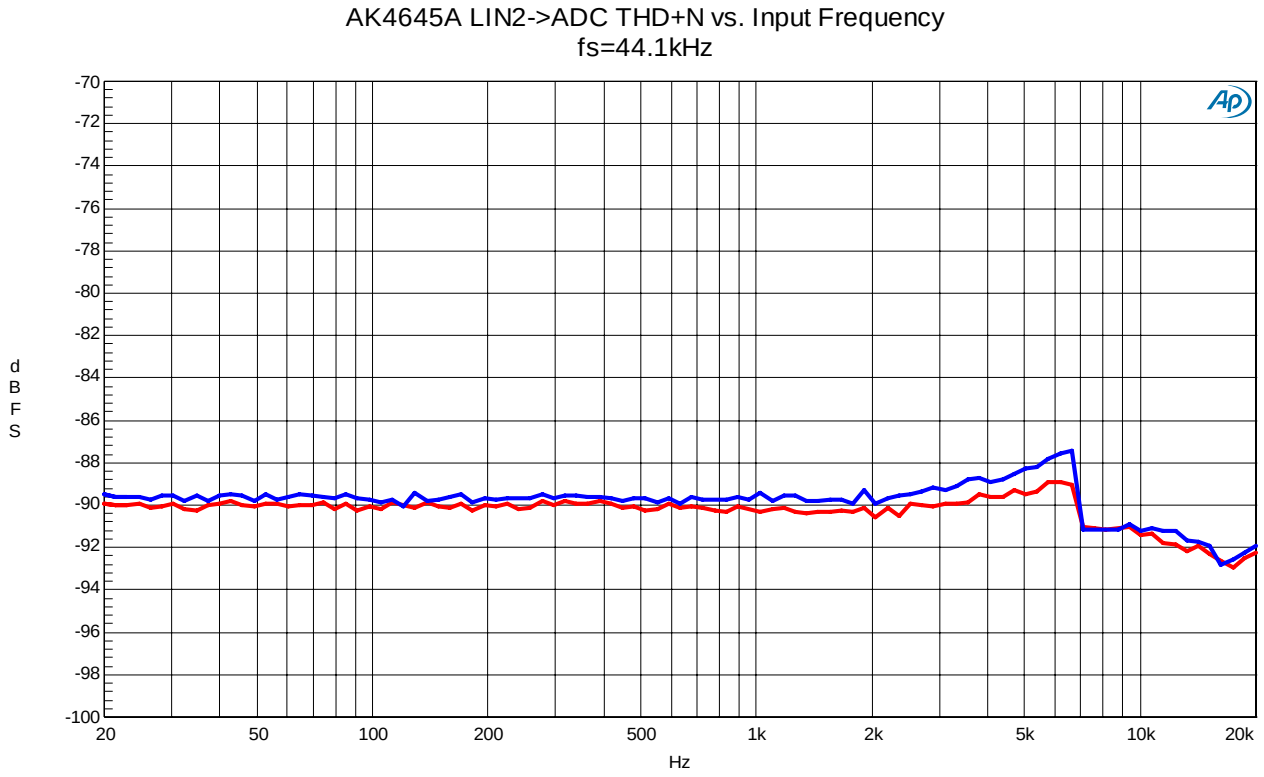


Figure 18. THD+N vs. Input Frequency

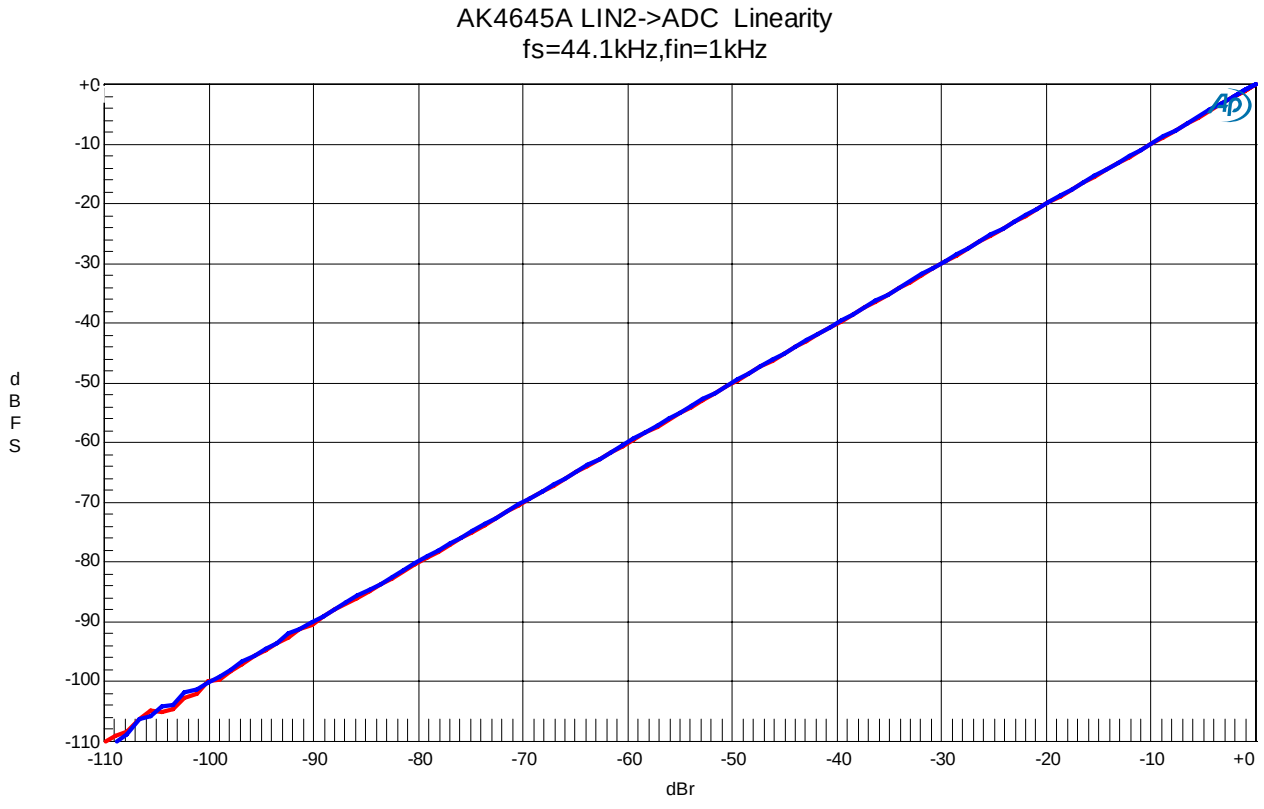


Figure 19. Linearity

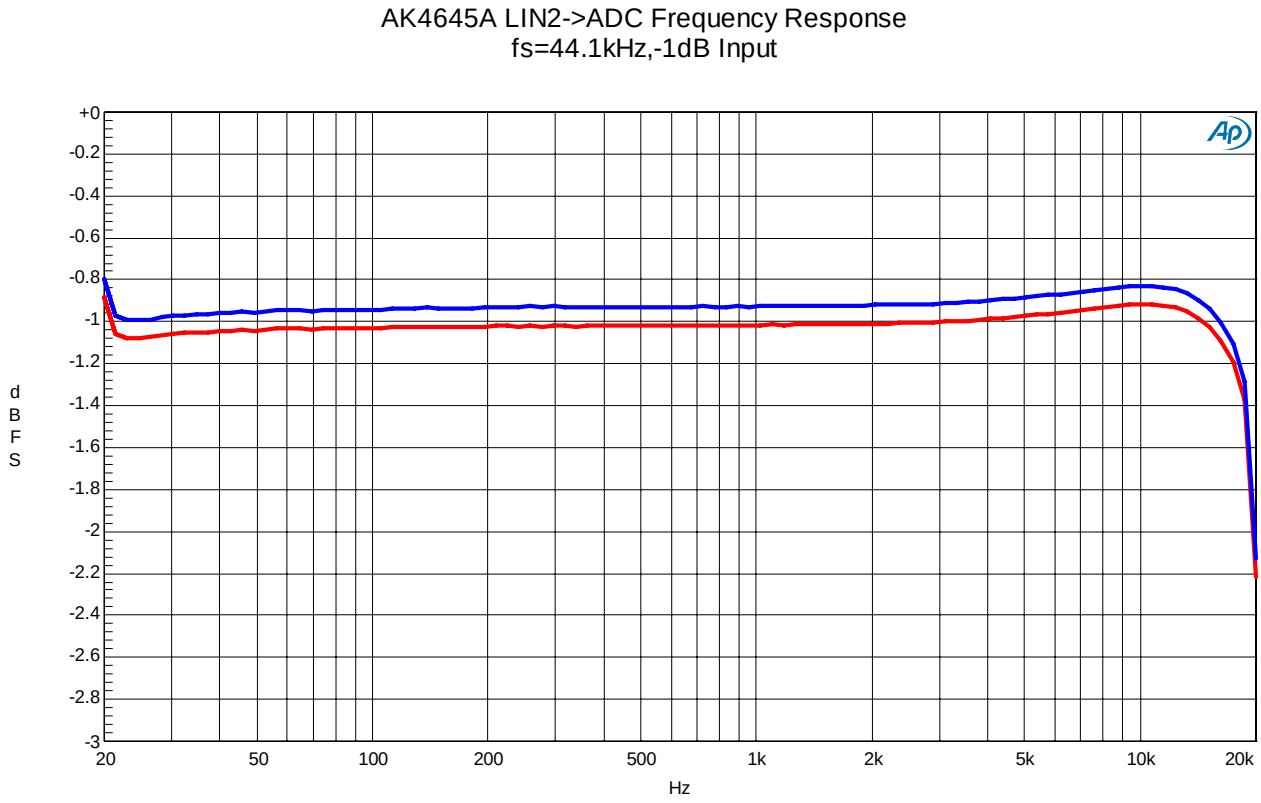


Figure 20. Frequency Response

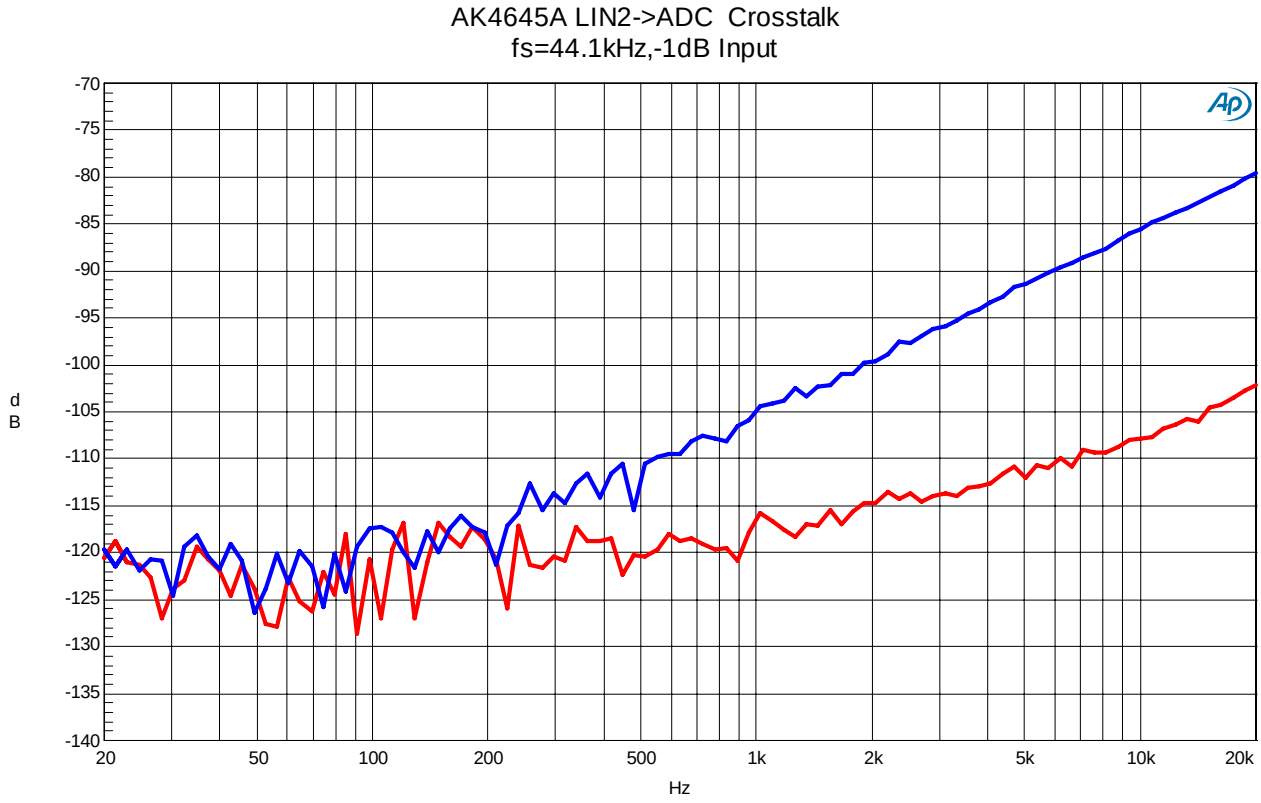


Figure 21. Crosstalk Plot

2-2 ADC (LIN2/RIN2 → ADC) (+20dB)

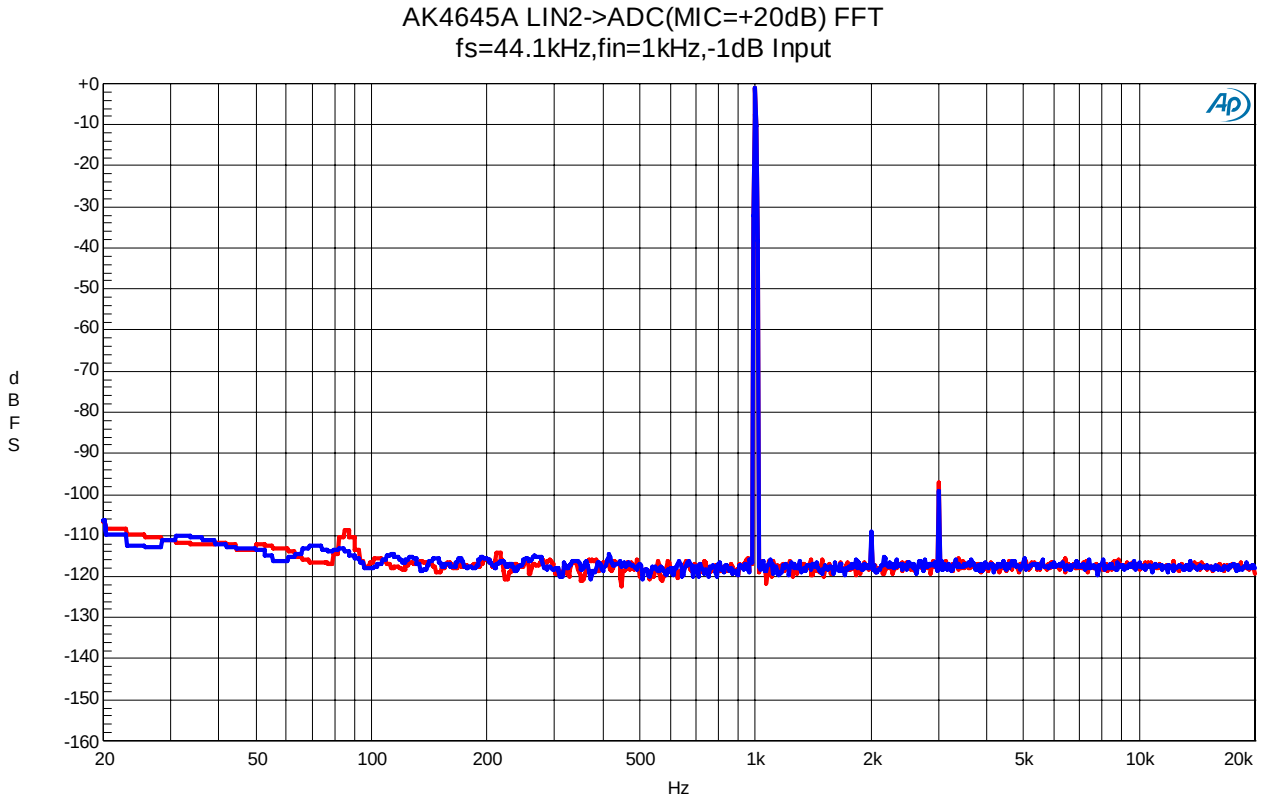


Figure 22. FFT Plot (Input level= 0dBFs)

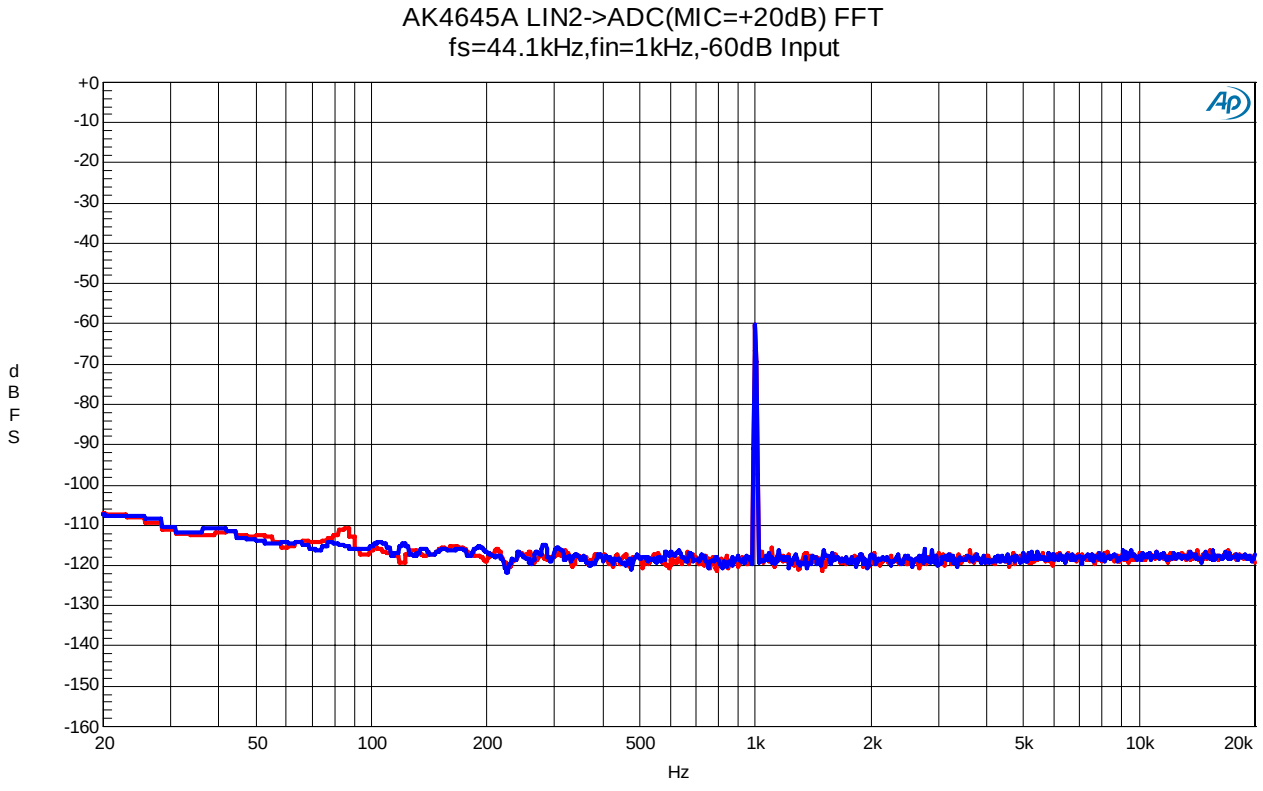


Figure 23. FFT Plot (Input level= -60dBFs)

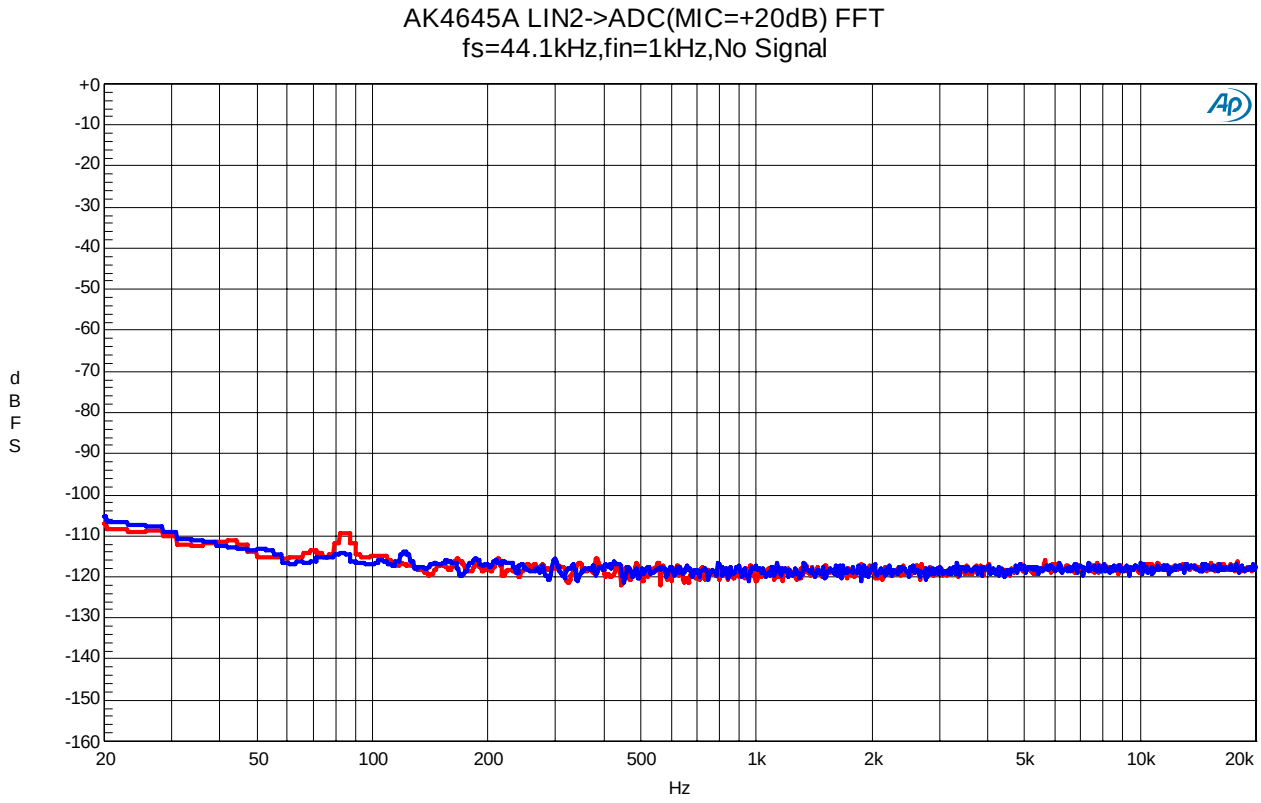


Figure 24. FFT Plot (No signal)

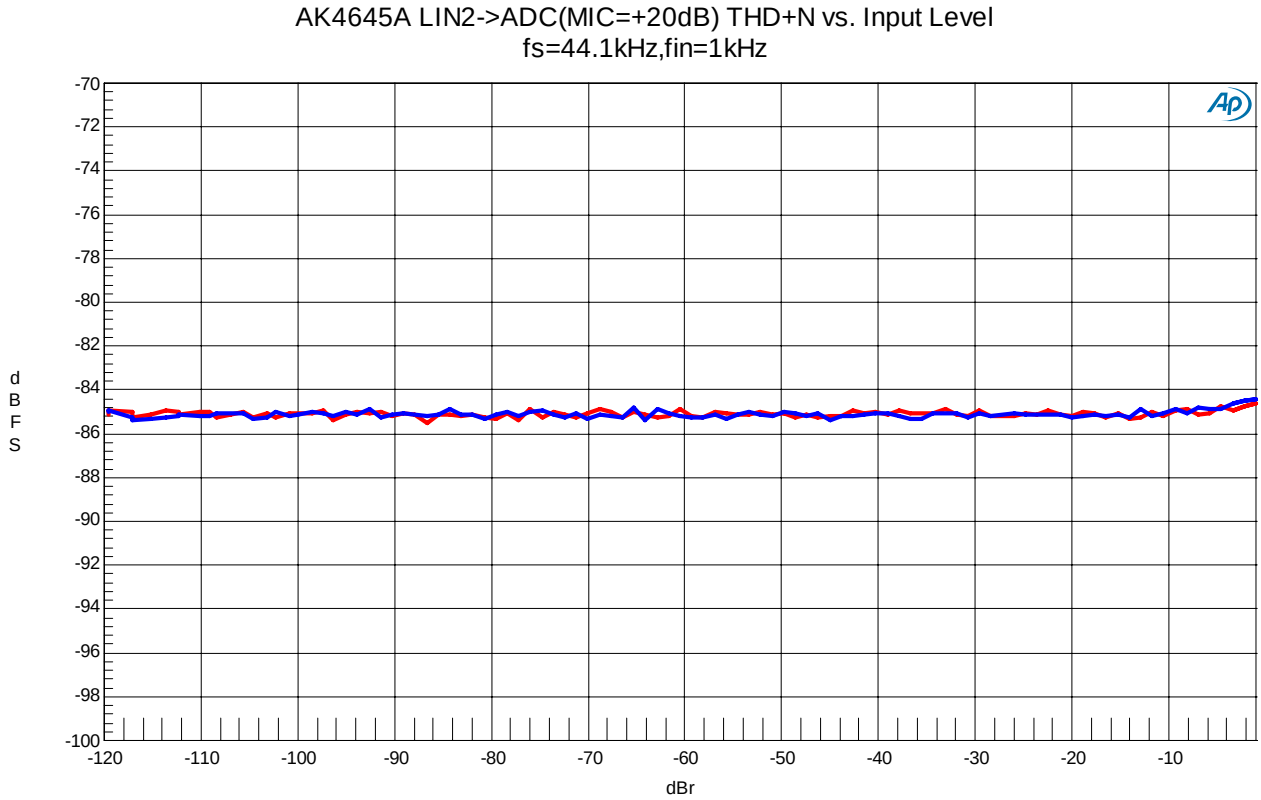


Figure 25. THD+N vs. Input Level

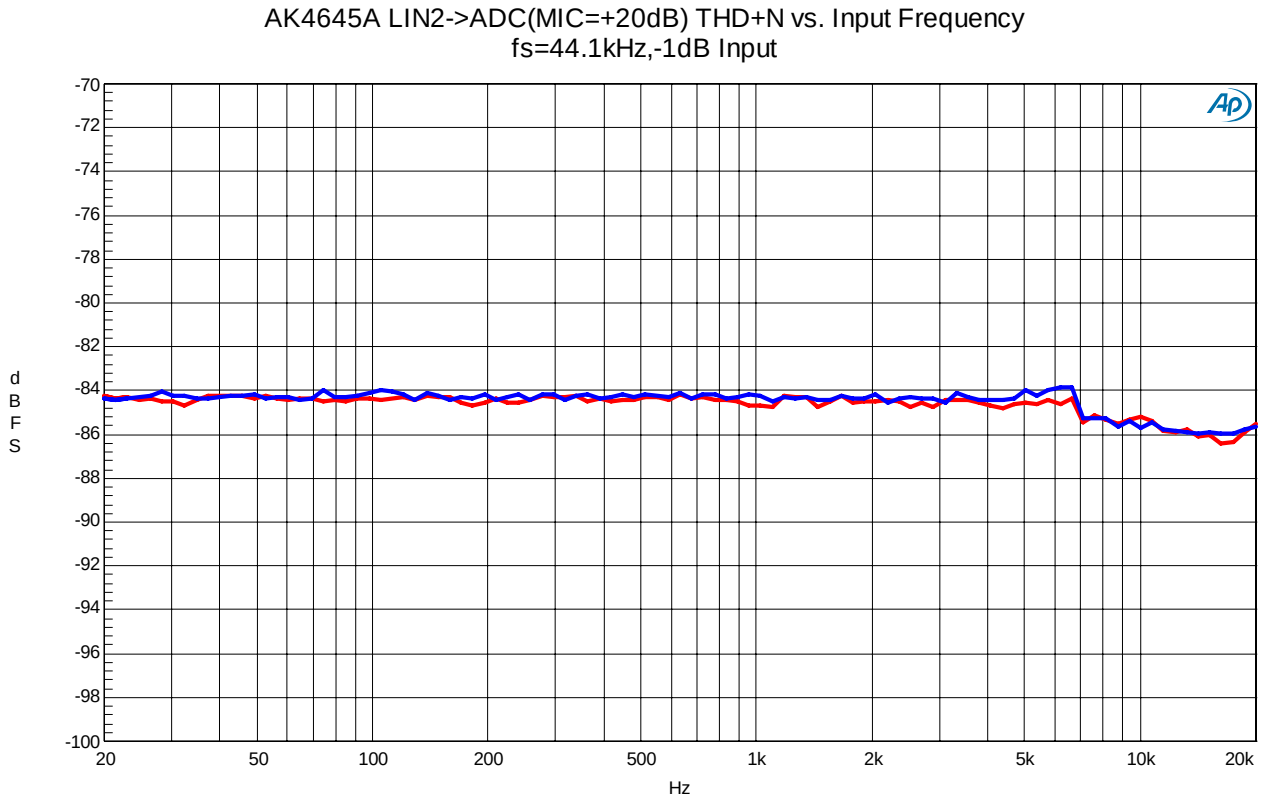


Figure 26. THD+N vs. Input Frequency

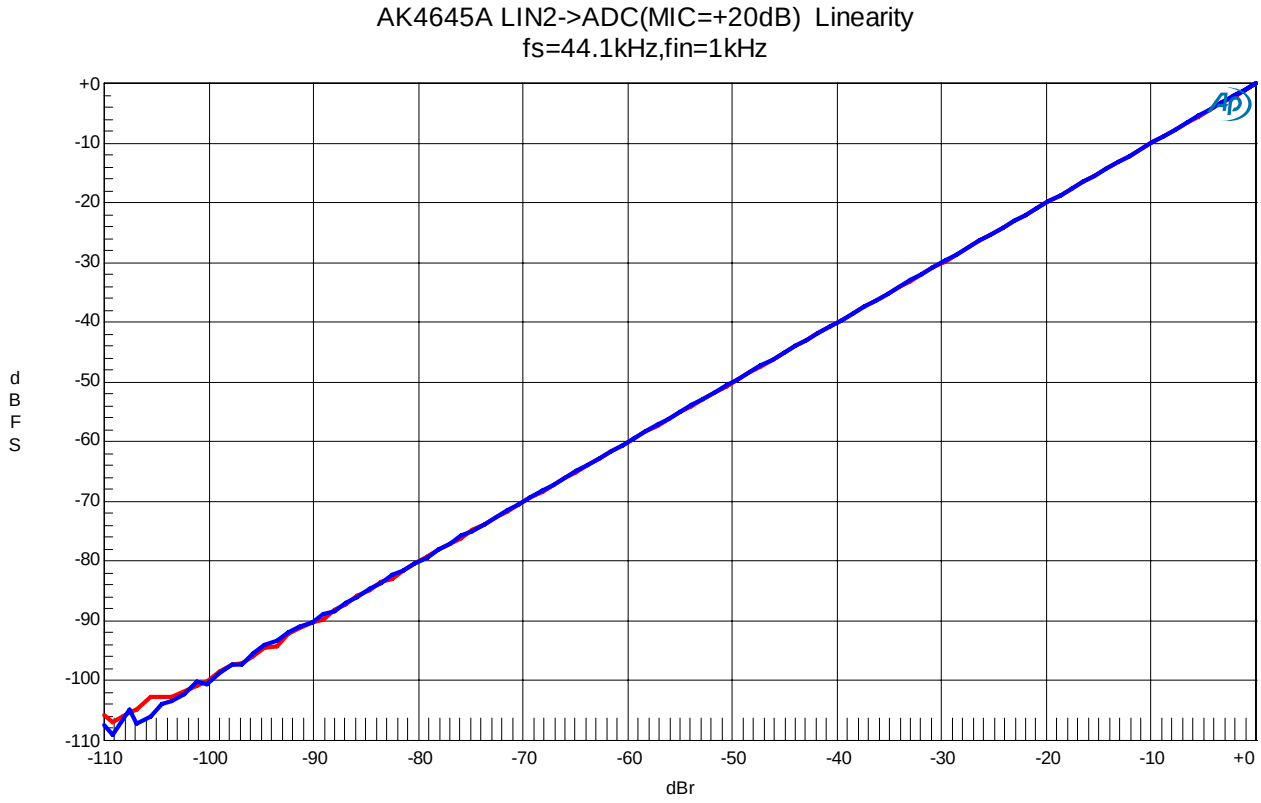


Figure 27. Linearity

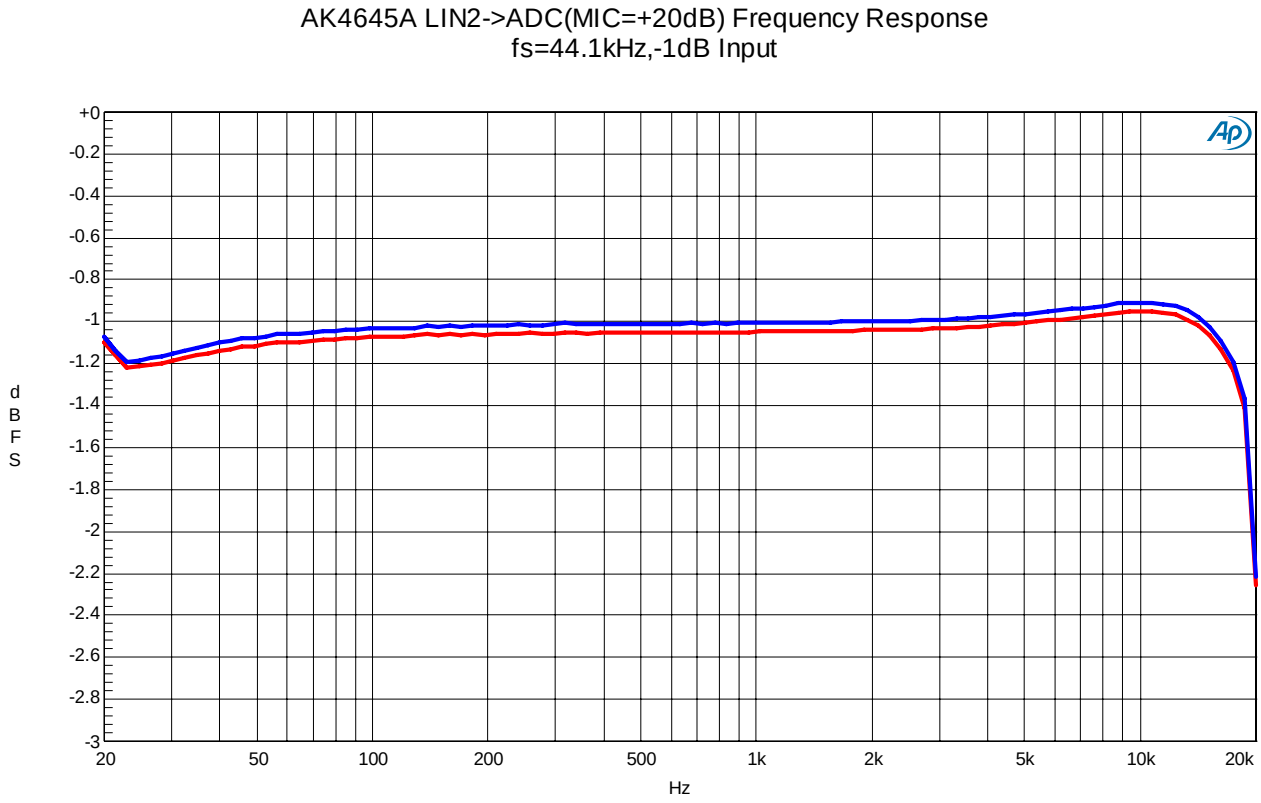


Figure 28. Frequency Response

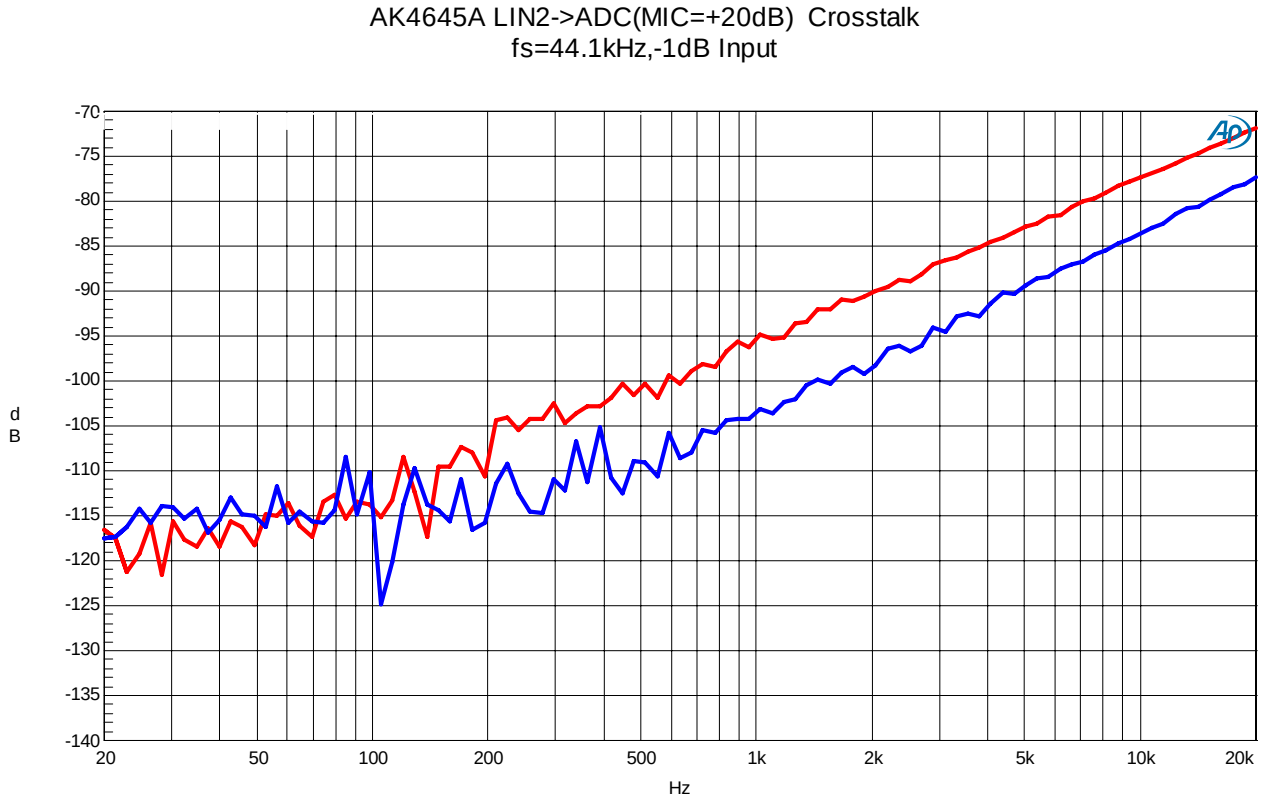


Figure 29. Crosstalk Plot

2-3 DAC (DAC→ LOUT/ROUT)

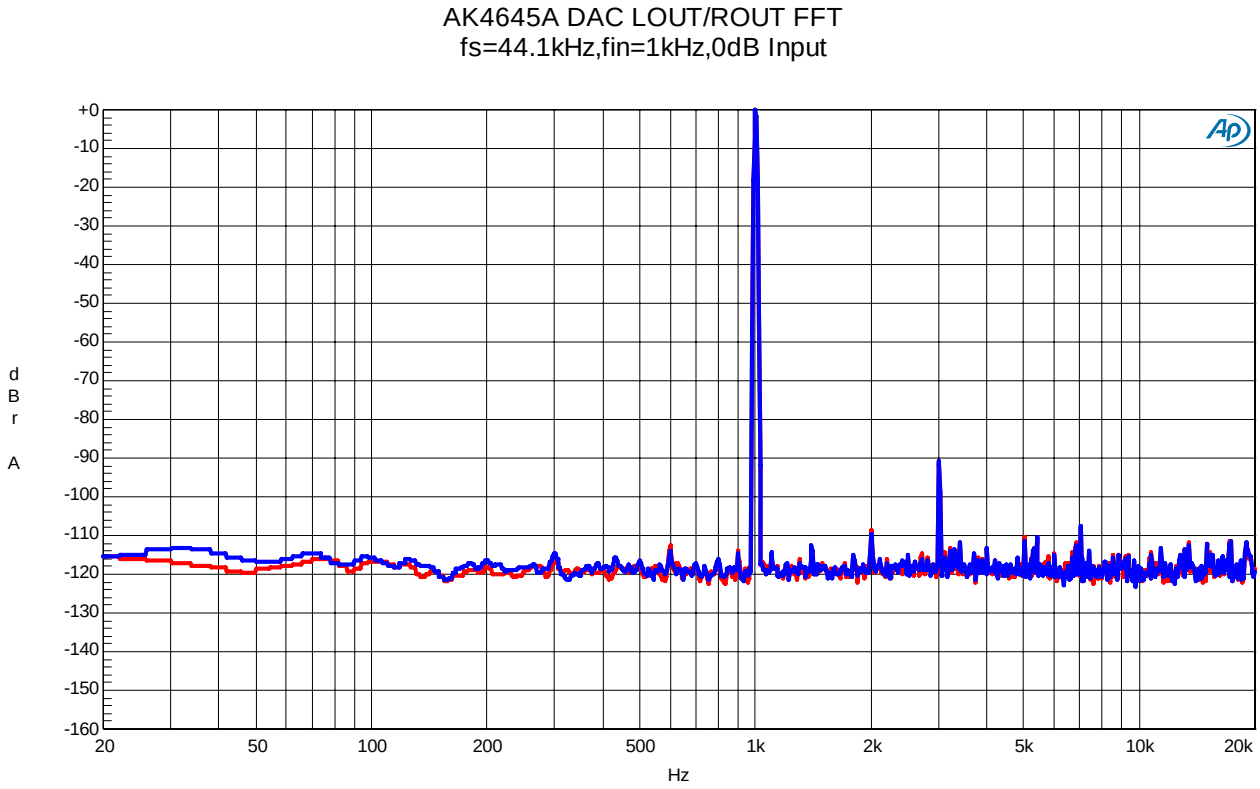


Figure 30. FFT Plot (Input level= 0dBFs)

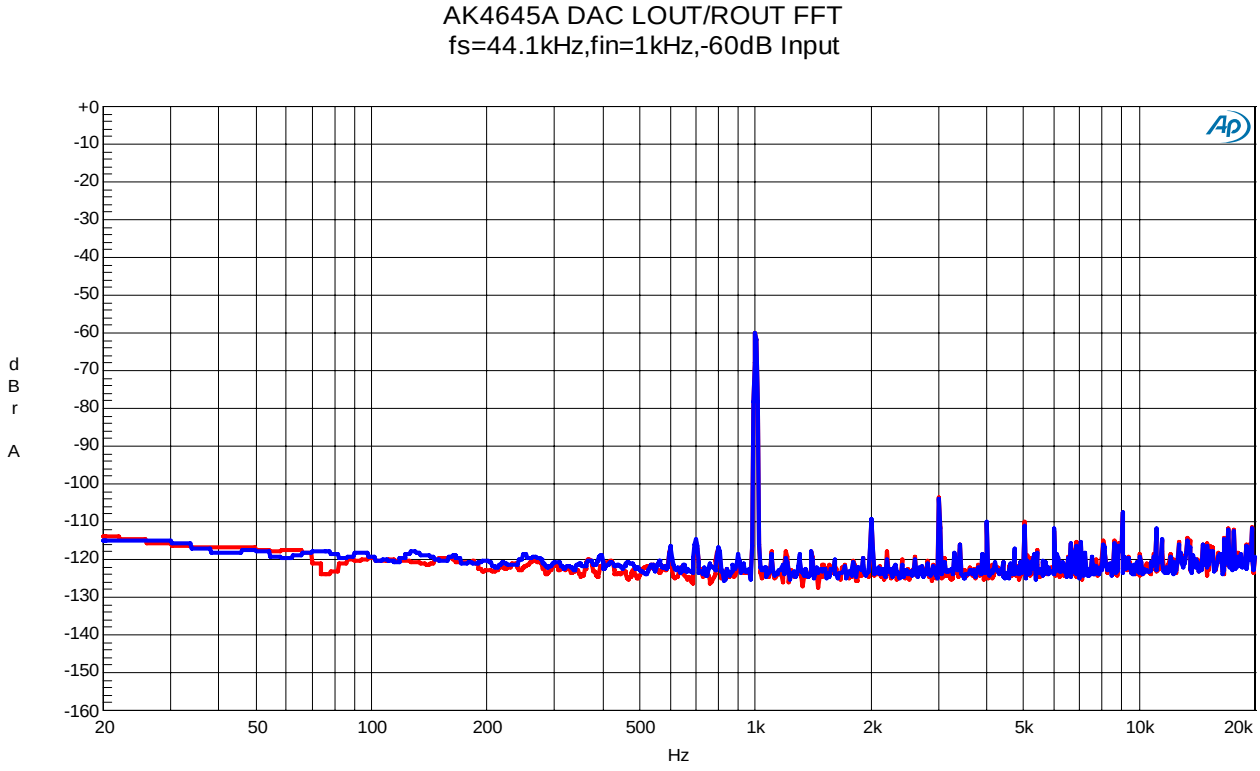


Figure 31. FFT Plot (Input level= -60dBFs)

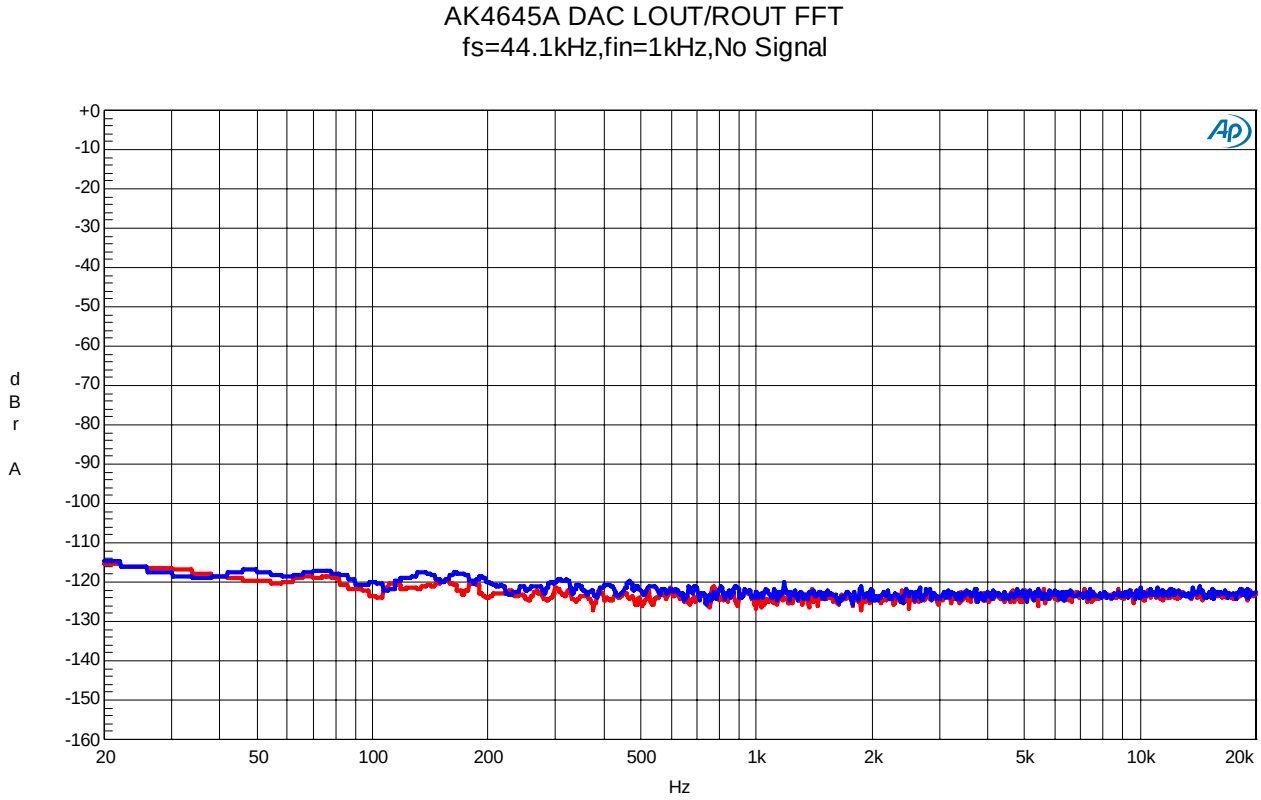


Figure 32. FFT Plot (No signal)

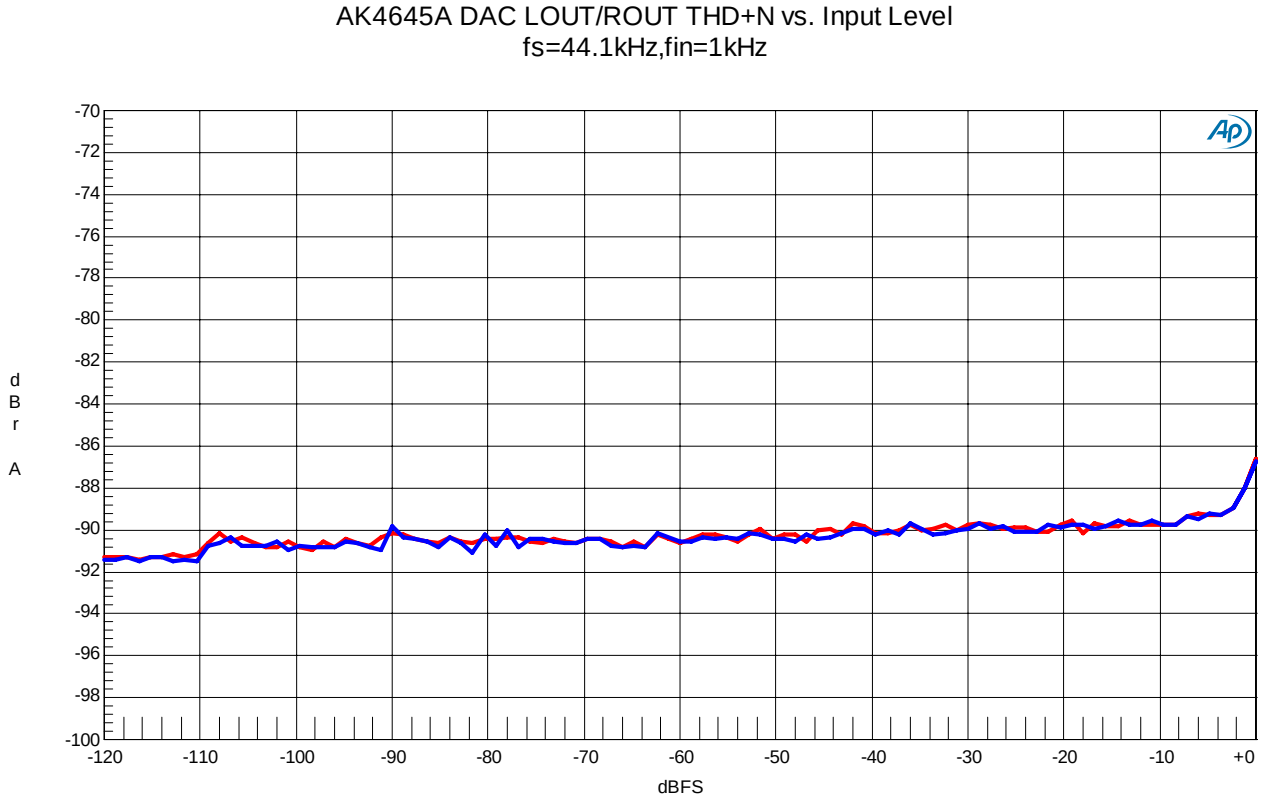


Figure 33. THD+N vs. Input Level

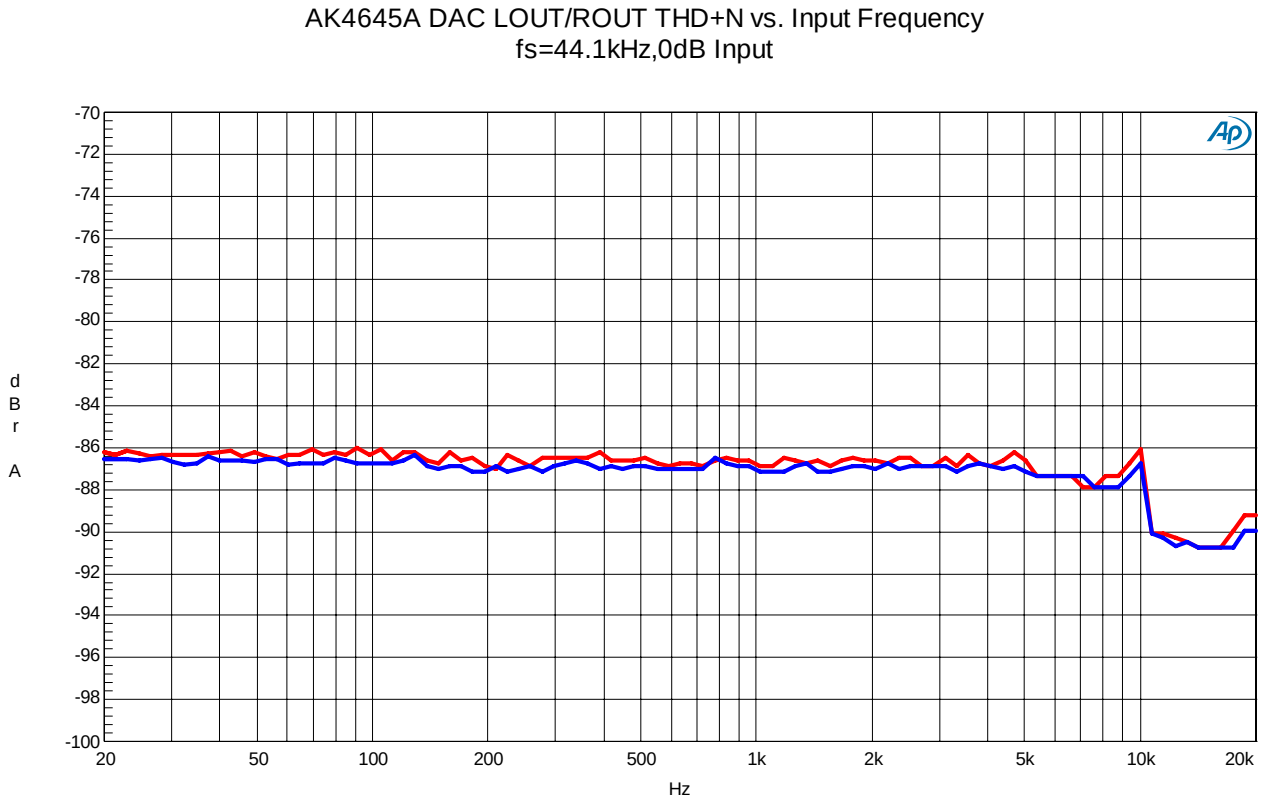


Figure 34. THD+N vs. Input Frequency

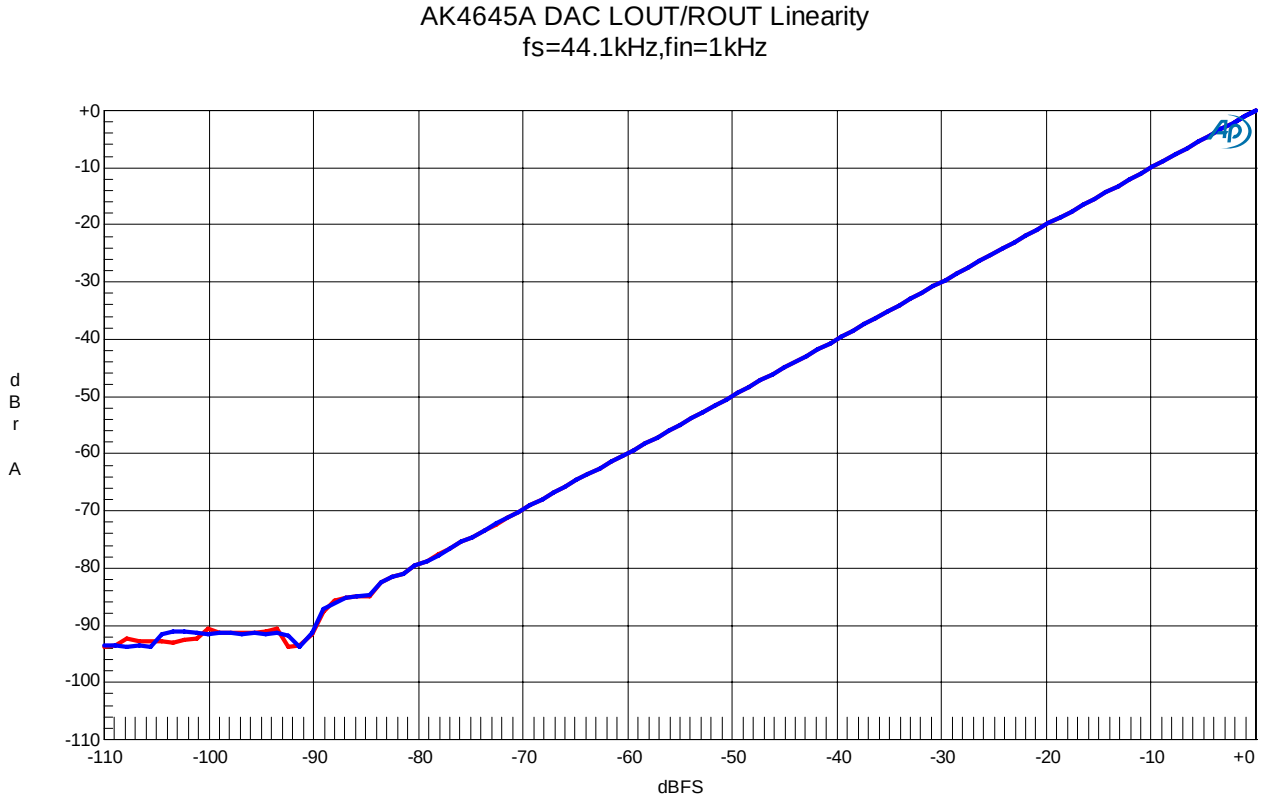


Figure 35. Linearity

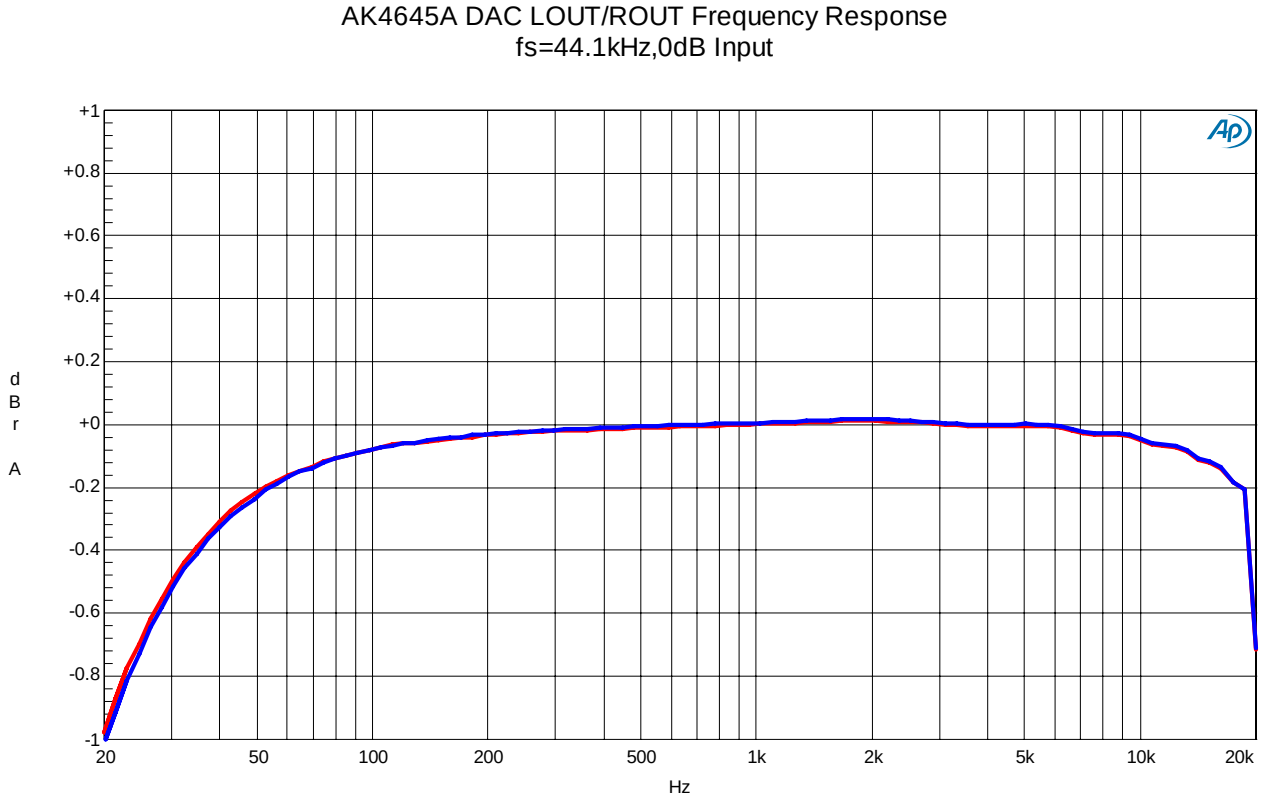


Figure 36. Frequency Response

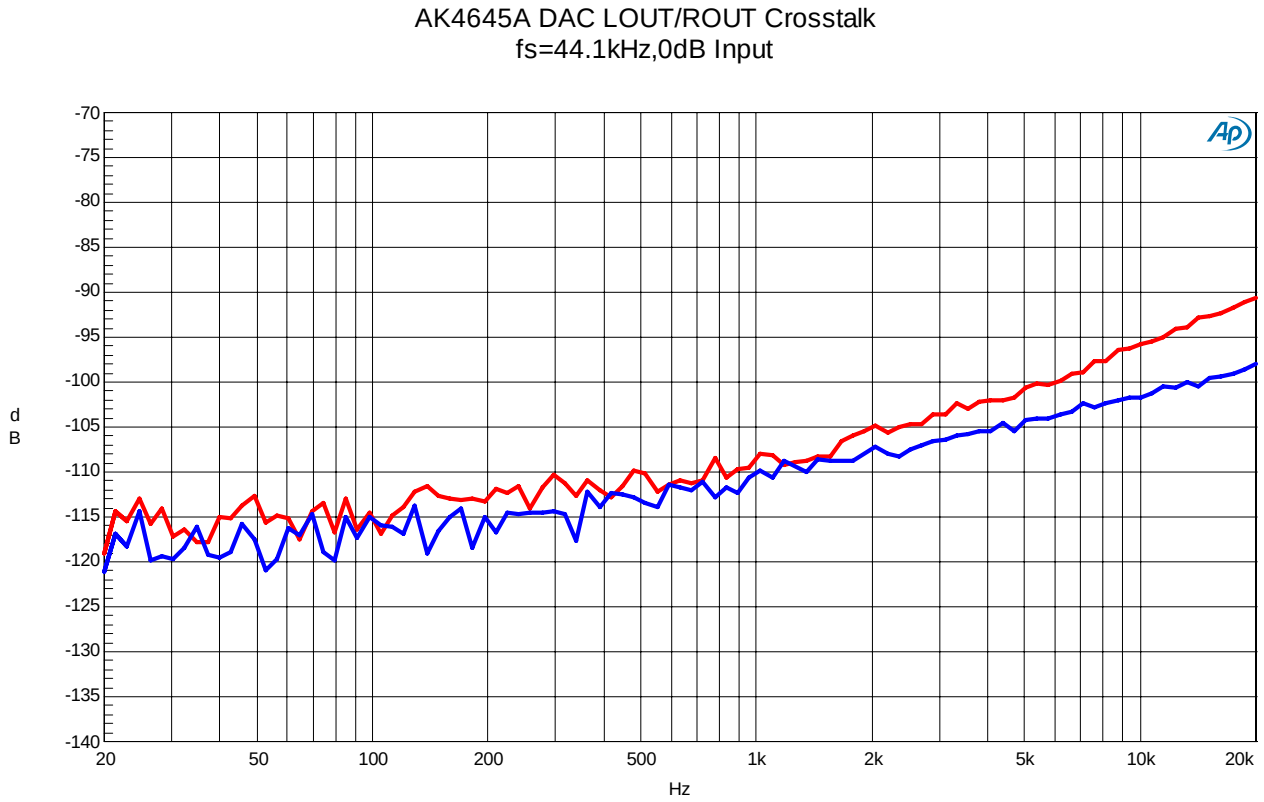


Figure 37. Crosstalk Plot

2-4 DAC (DAC→ HPL/HPR)

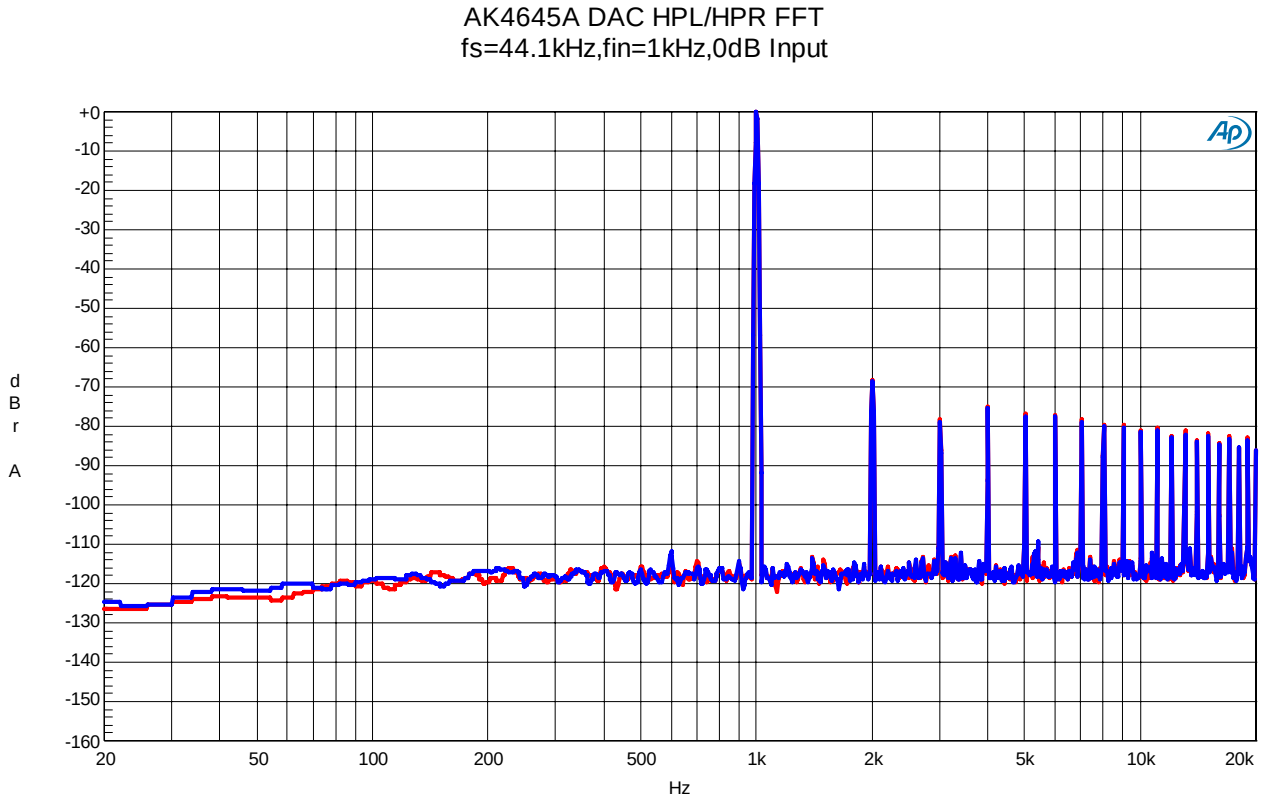


Figure 38. FFT Plot (Input level= 0dBFs)

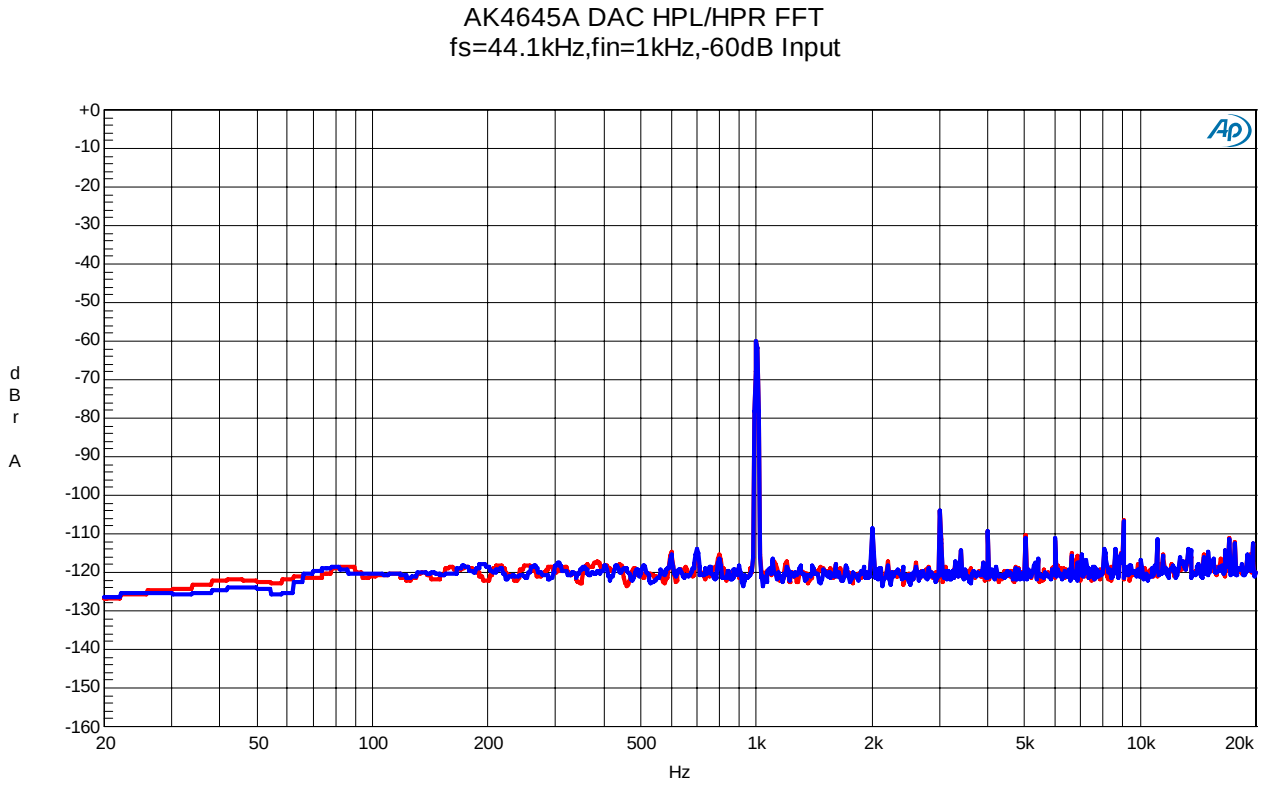


Figure 39. FFT Plot (Input level= -60dBFs)

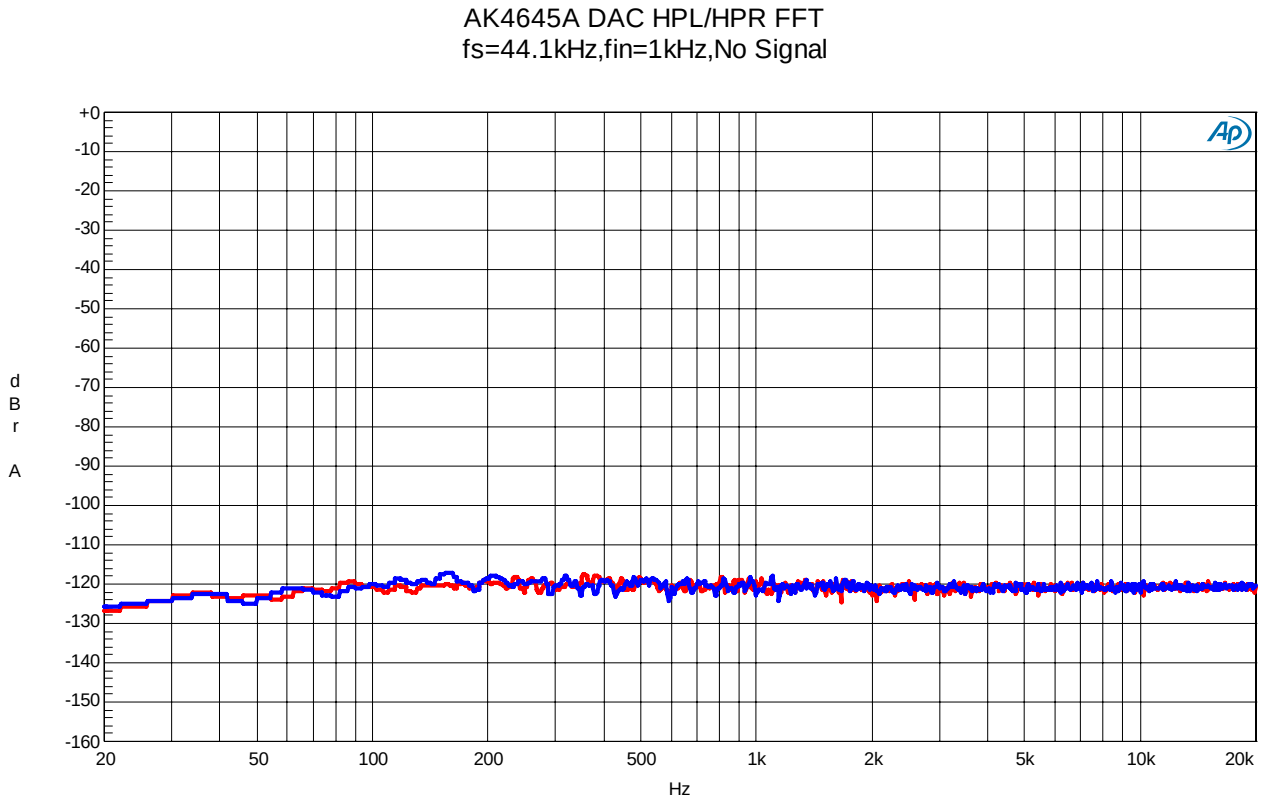


Figure 40. FFT Plot (No signal)

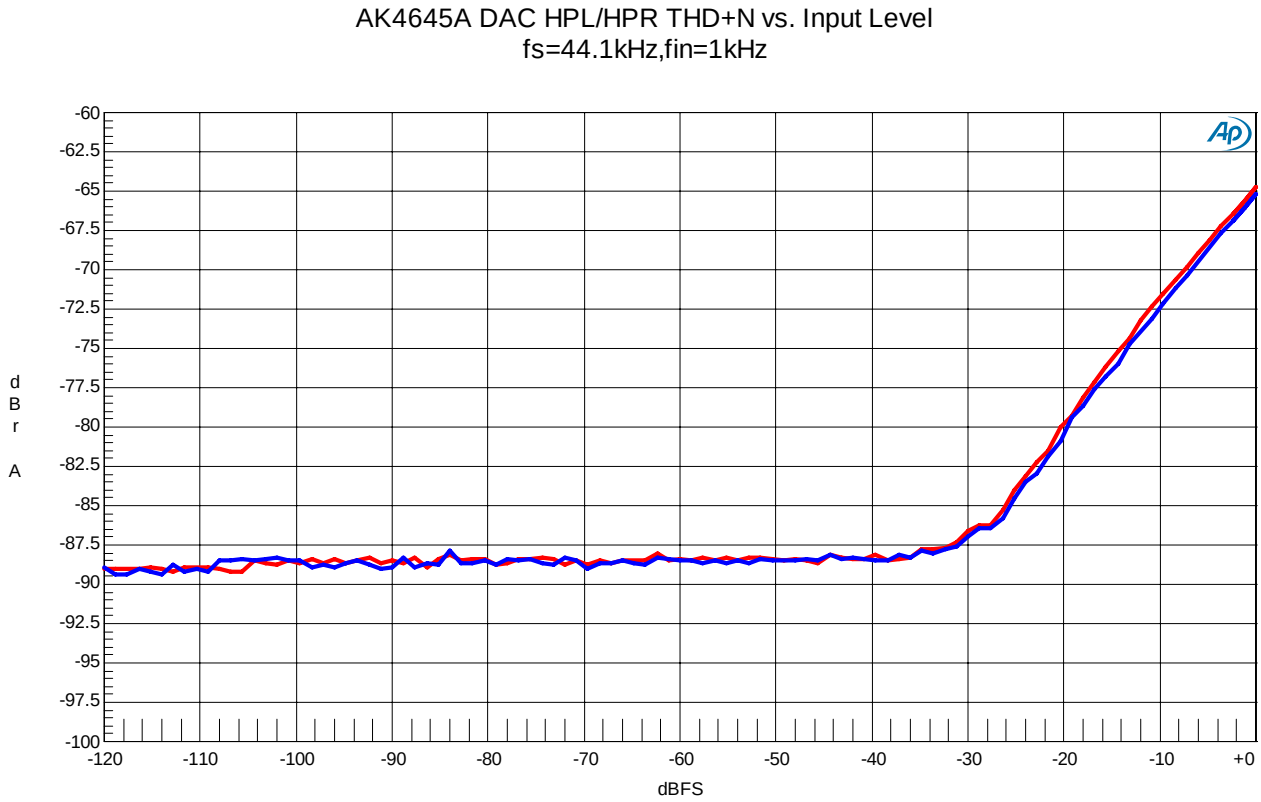


Figure 41. THD+N vs. Input Level

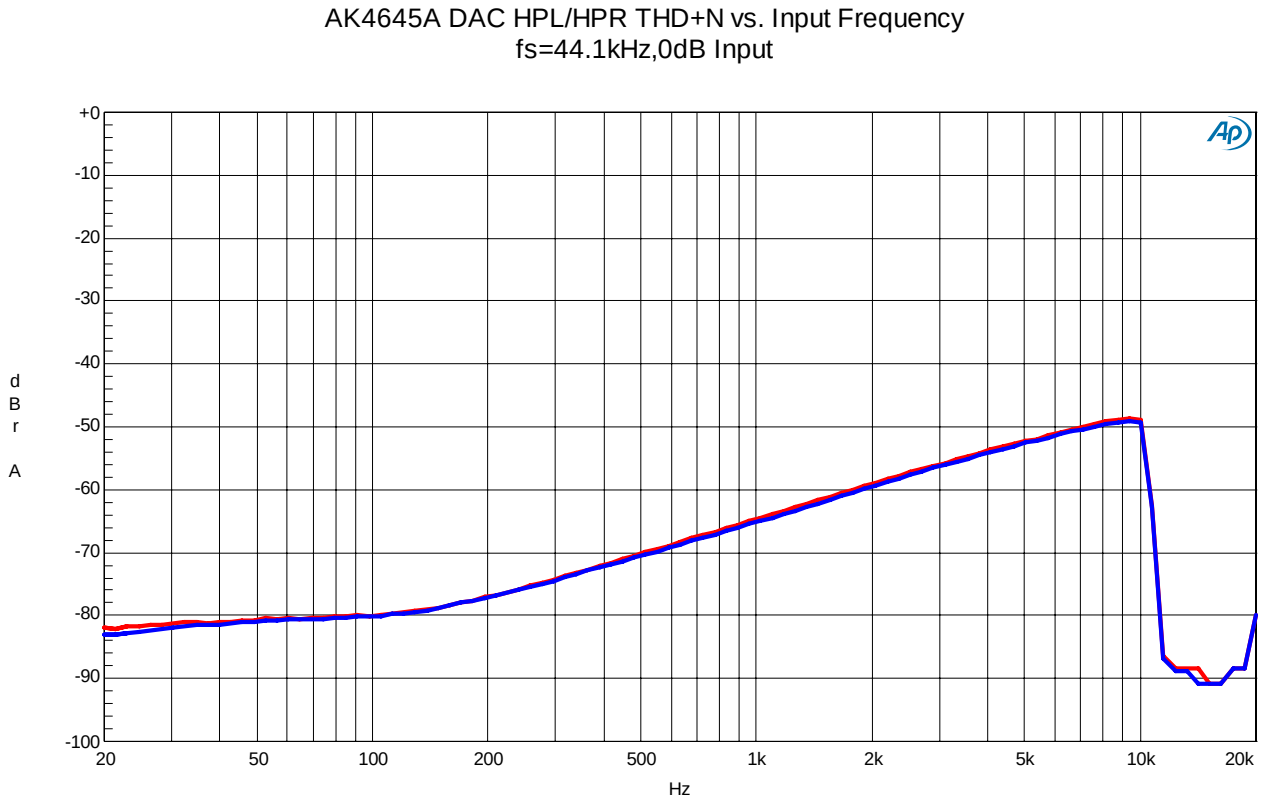


Figure 42. THD+N vs. Input Frequency

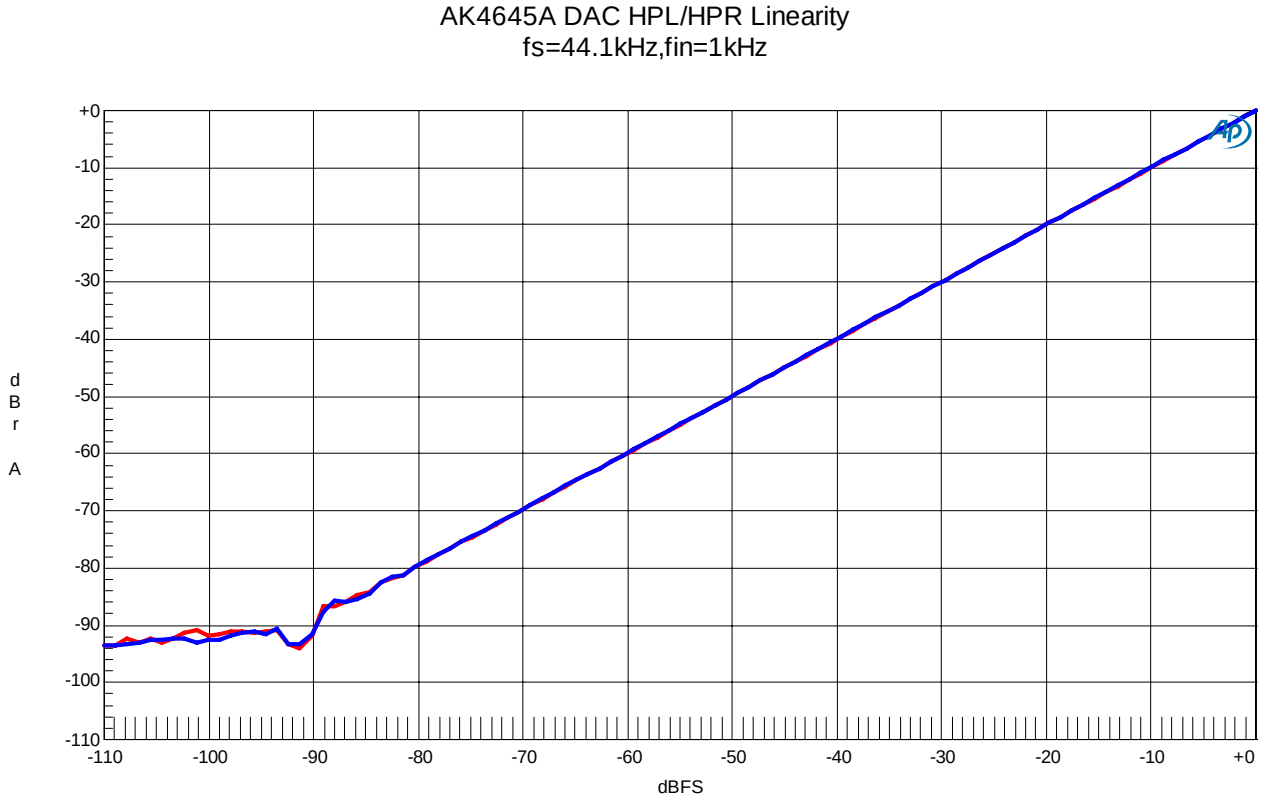
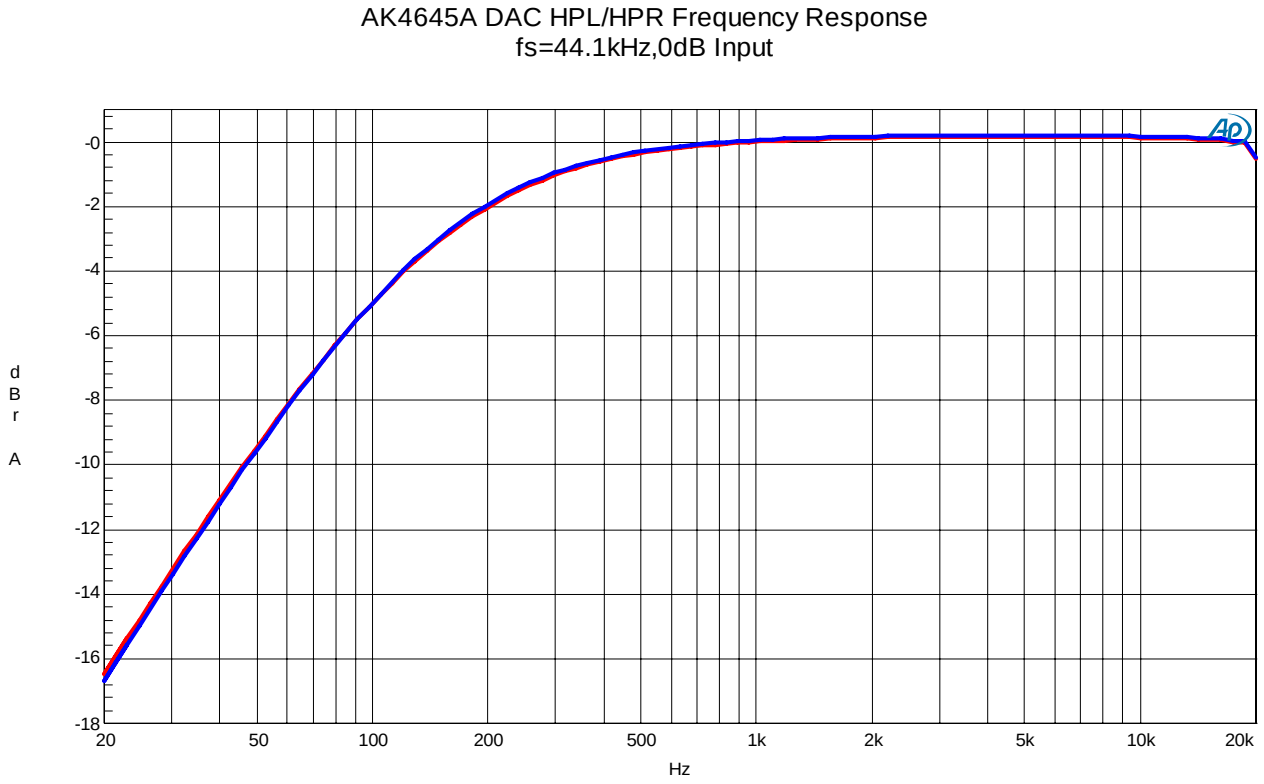


Figure 43. Linearity



*Cut-off frequency of HPF on board: 148.5Hz

Figure 44. Frequency Response

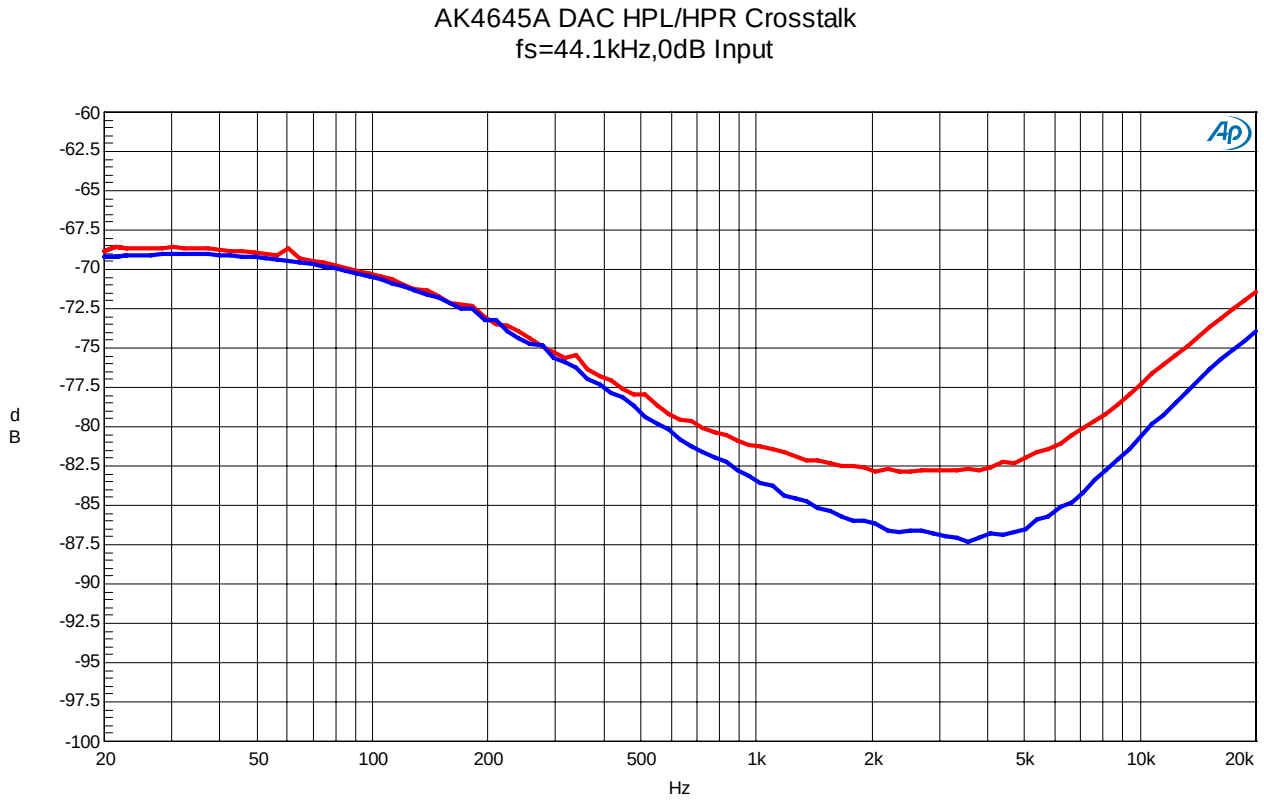
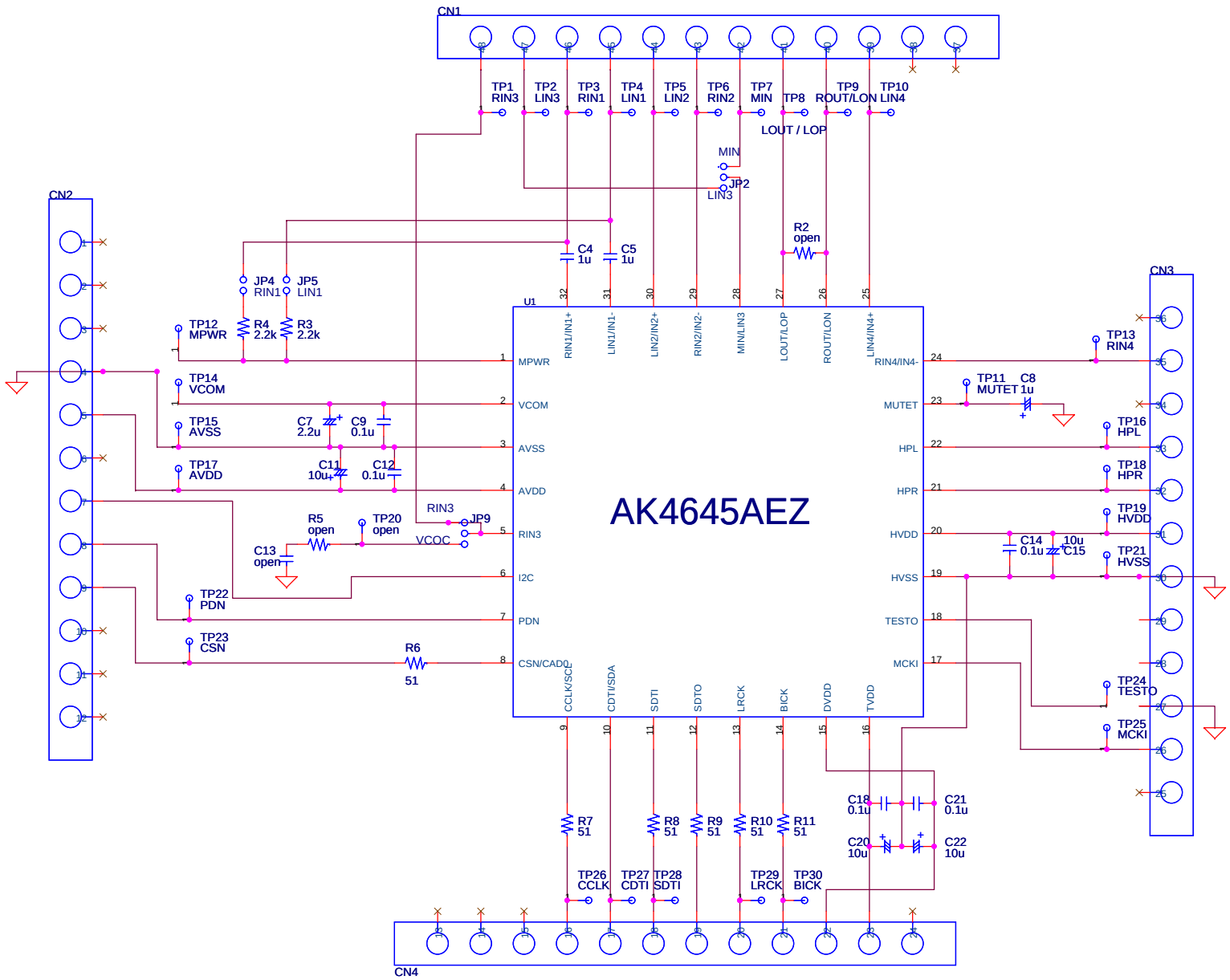


Figure 45. Crosstalk Plot

Revision History

Date (YY/MM/DD)	Manual Revision	Board Revision	Reason	Contents
08/05/29	KM094900	0	First edition	
09/10/15	KM094901	1	Change	A block diagram was modified. Circuit diagram were changed. R5,C13,TP20:Open. Measurement results and Plots were updated. Default Jumper settings were changed.



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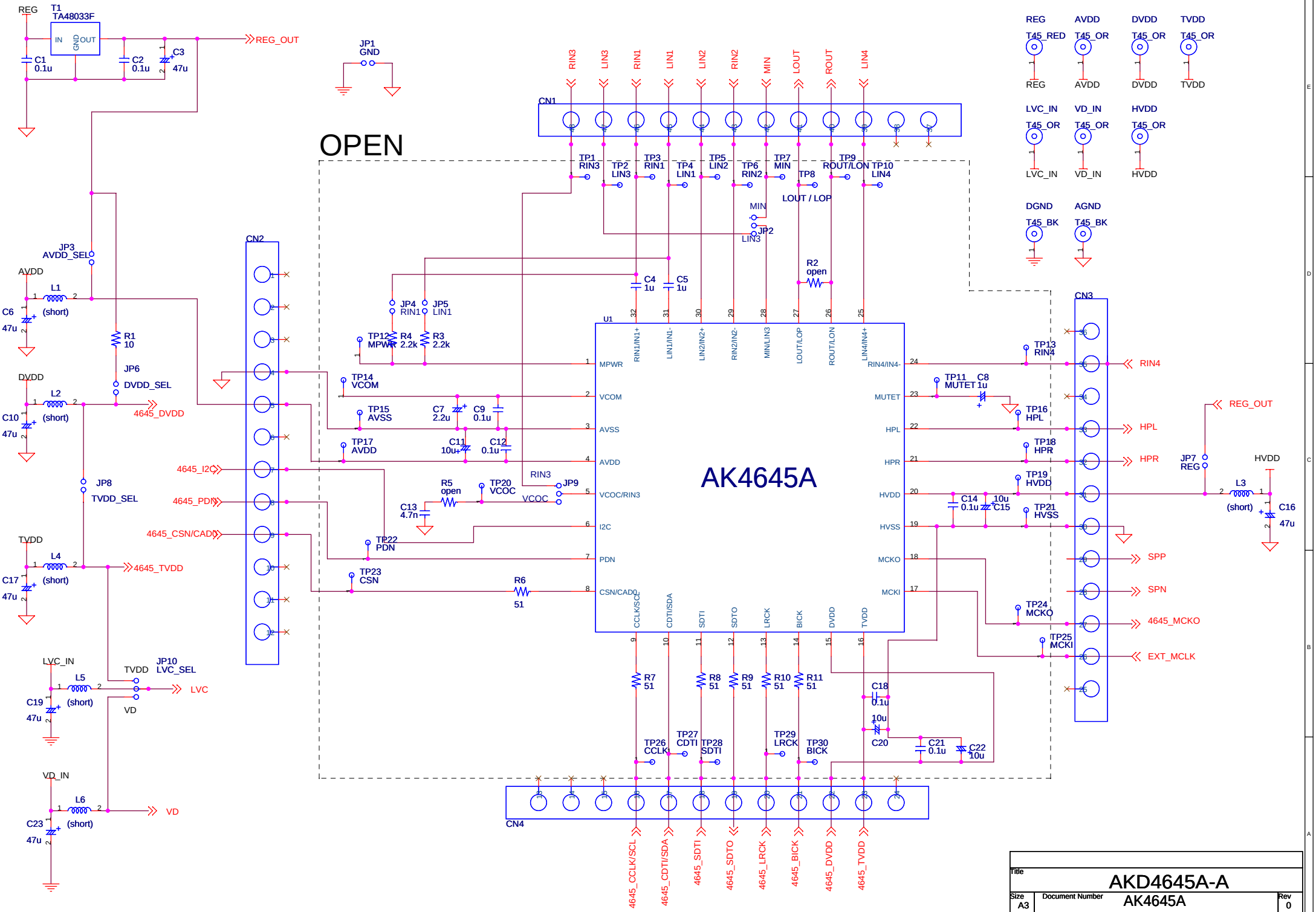
Size: A3	Document Number: AK4645AEZ	Rev: 0
Date: Monday, August 31, 2009	Sheet 1 of 1	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TA48033F
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GND
OUT
C1
0.1u
C2
0.1u
C3
47u
REG_OUT
JP1
GND
CN1
RIN3
LIN3
RIN1
LIN1
LIN2
RIN2
MIN
LOUT
ROUT
LIN4
TP1
RIN3
TP2
LIN3
TP3
RIN1
TP4
LIN1
TP5
LIN2
TP6
RIN2
TP7
MIN
TP8
LOUT / LOP
TP9
ROUT/LON
TP10
LIN4
MIN
JP2
LIN3
R2
open
C4
1u
C5
1u
JP4
RIN1
JP5
LIN1
TP12
MPWR
R4
2.2k
R3
2.2k
U1
MPWR
VCOM
AVSS
AVDD
VCOC/RIN3
I2C
PDN
CSN/CAD0
RIN1/IN1+
LIN1/IN1-
LIN2/IN2+
RIN2/IN2-
MIN/LIN3
LOUT/LOP
ROUT/LON
LIN4/IN4+
RIN4/IN4-
MUTET
HPL
HPR
HVDD
HVSS
MCKO
MCKI
CCLK/SCL
CDTI/SDA
SDTI
SDTO
LRCK
BICK
DVDD
TVDD
CN2
CN3
CN4
REG
T45_RED
AVDD
T45_OR
DVDD
T45_OR
TVDD
T45_OR
LVC_IN
T45_OR
VD_IN
T45_OR
HVDD
T45_OR
DGND
T45_BK
AGND
T45_BK
JP3
AVDD_SEL
AVDD
L1
(short)
C6
47u
R1
10
JP6
DVDD_SEL
4645_DVDD
DVDD
L2
(short)
C10
47u
JP8
TVDD_SEL
TVDD
L4
(short)
C17
47u
4645_TVDD
LVC_IN
L5
(short)
C19
47u
TVDD
JP10
LVC_SEL
LVC
VD
VD_IN
L6
(short)
C23
47u
VD
4645_I2C
4645_PDN
4645_CSN/CAD0
TP14
VCOM
TP15
AVSS
TP17
AVDD
C7
2.2u
C9
0.1u
C11
10u
C12
0.1u
R5
open
TP20
VCOC
JP9
RIN3
VCOC
C13
4.7n
TP22
PDN
TP23
CSN
R6
51
TP13
RIN4
RIN4
TP11
MUTET
C8
1u
TP16
HPL
HPL
TP18
HPR
HPR
TP19
HVDD
C14
0.1u
10u
C15
TP21
HVSS
REG_OUT
JP7
REG
HVDD
L3
(short)
C16
47u
SPP
SPN
4645_MCKO
TP24
MCKO
TP25
MCKI
EXT_MCKLK
R7
51
R8
51
R9
51
R10
51
R11
51
C18
0.1u
10u
C20
C21
0.1u
C22
10u
TP26
CCLK
TP27
CDTI
TP28
SDTI
TP29
LRCK
TP30
BICK
4645_CCLK/SCL
4645_CDTI/SDA
4645_SDTI
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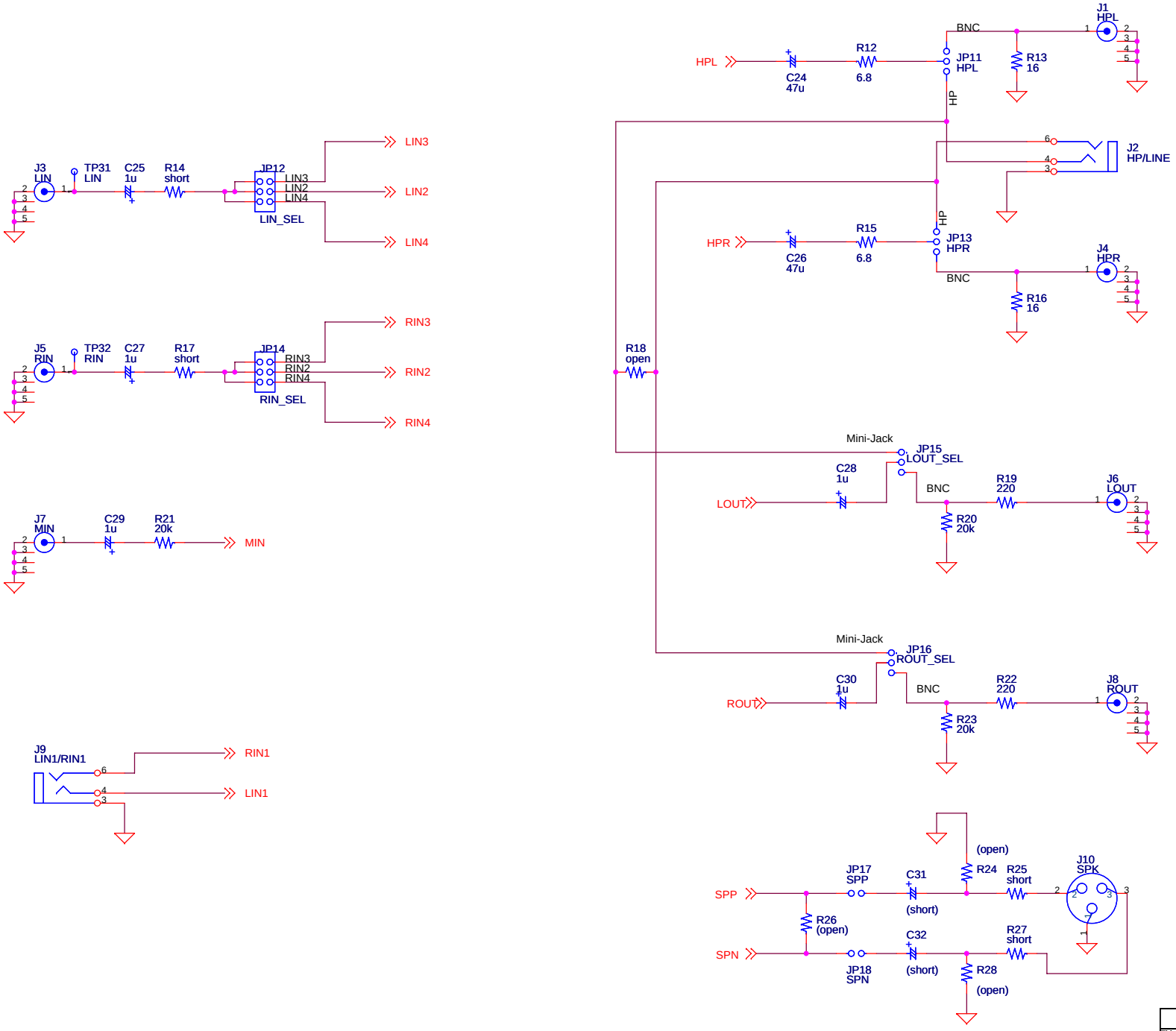

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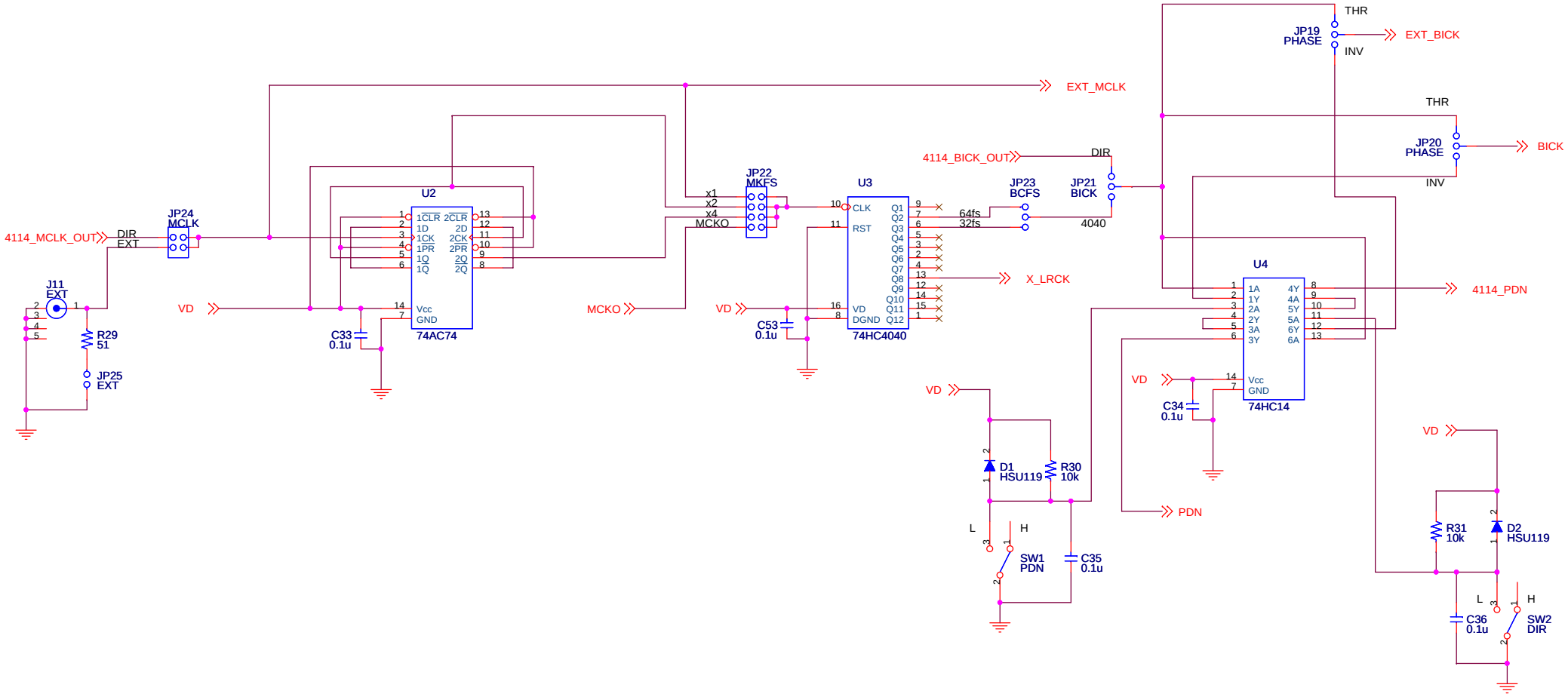
Date: Friday, August 28, 2009	Sheet 2 of 5	



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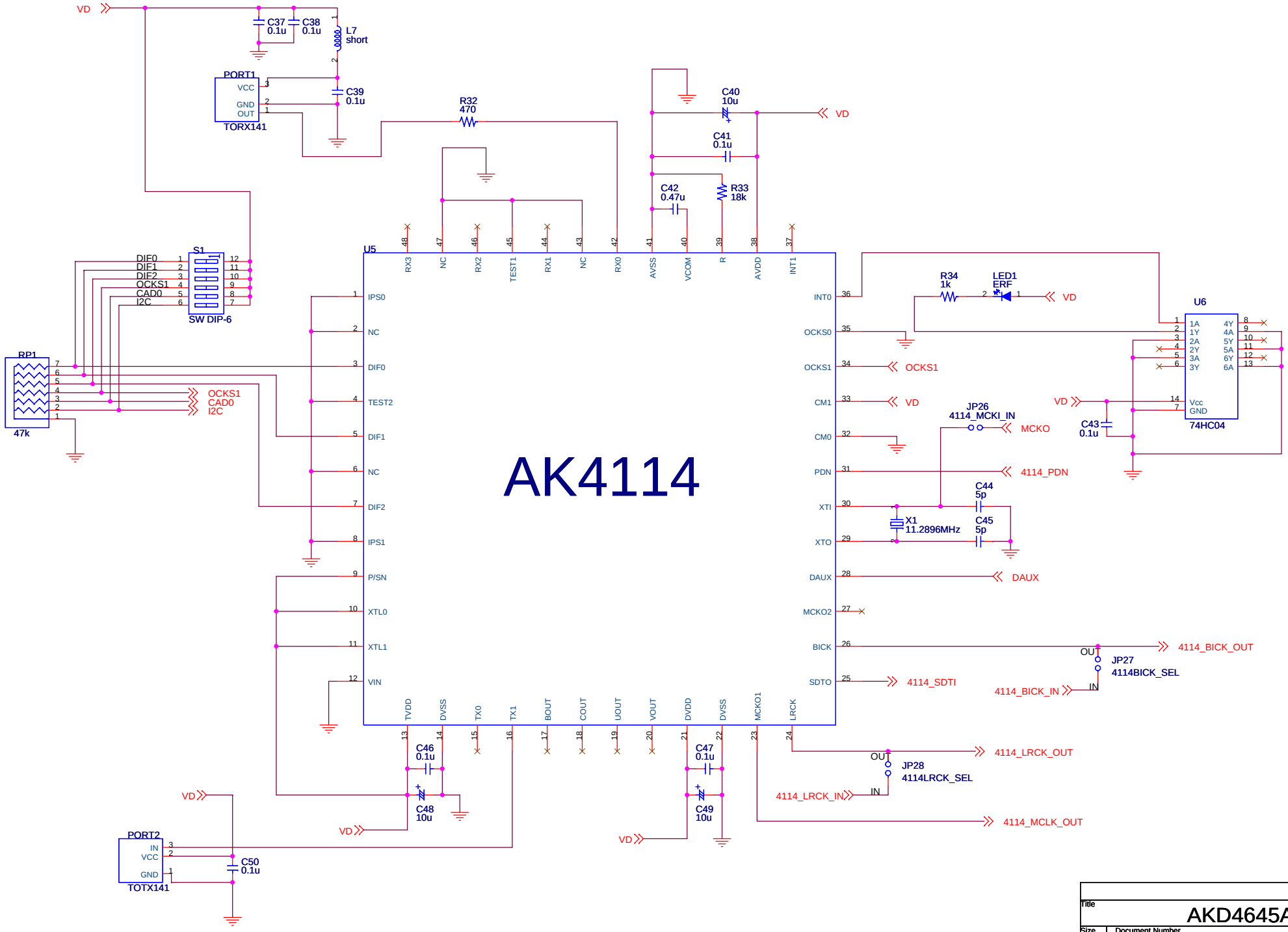
Size: A3	Document Number: CLOCK	Rev: 0
Date: Friday, August 28, 2009	Sheet 3 of 5	



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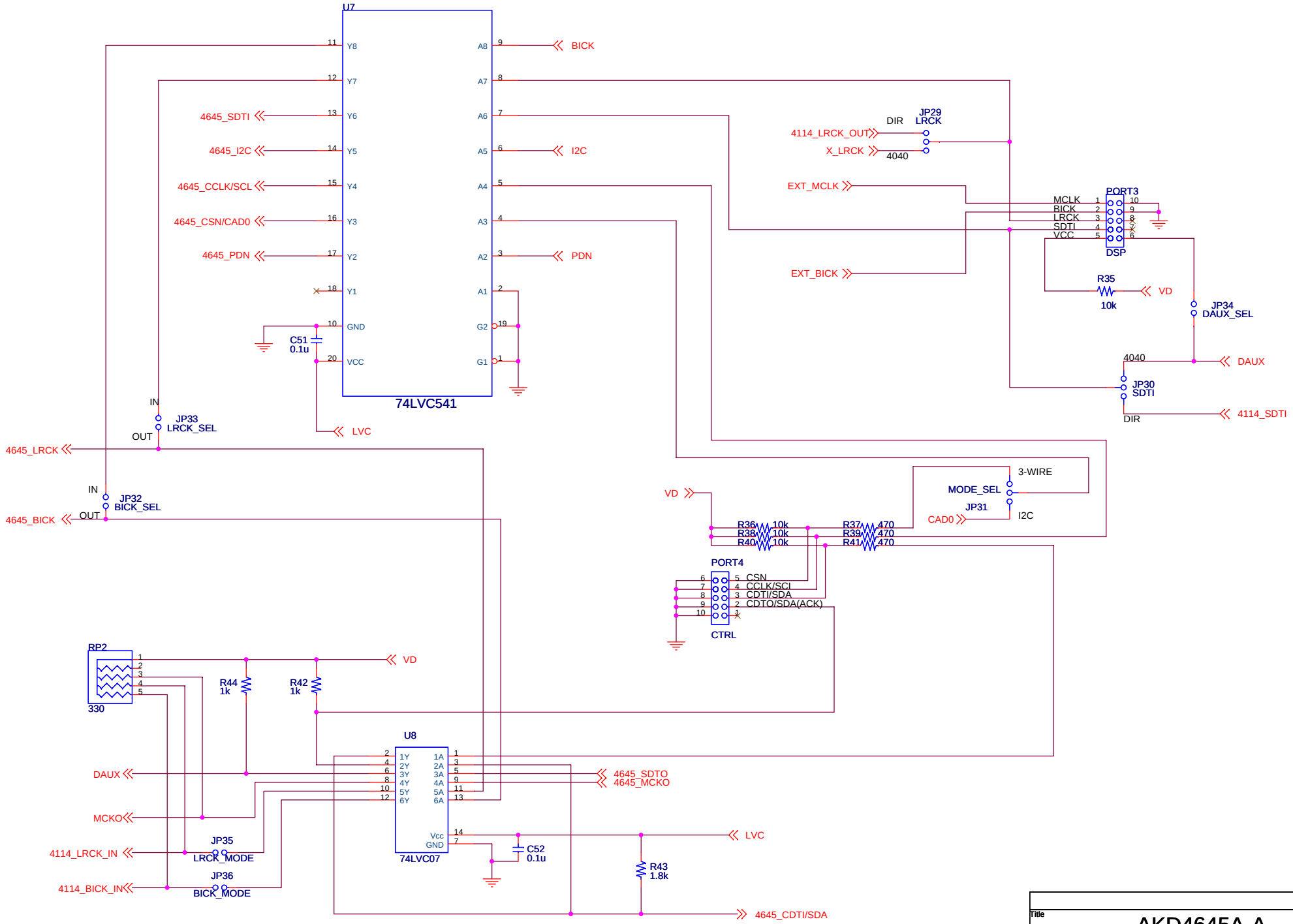
Size A3	Document Number DIR/DIT	Rev 0
Date: Monday, August 31, 2009	Sheet 4 of 5	



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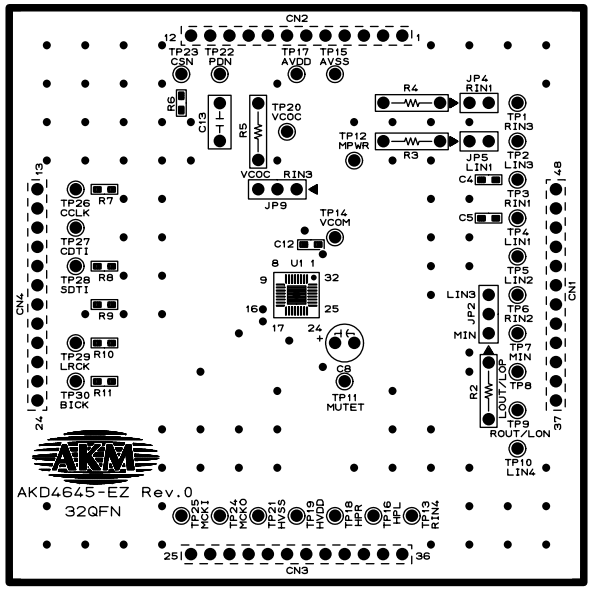
Date: Friday, August 28, 2009	Sheet 5 of 5	



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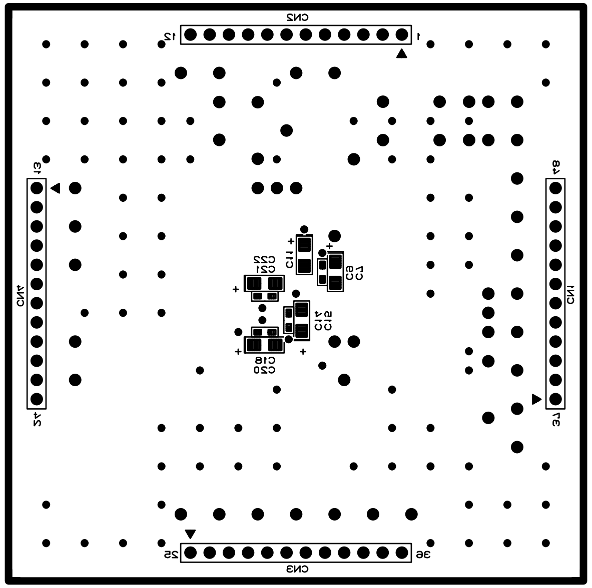

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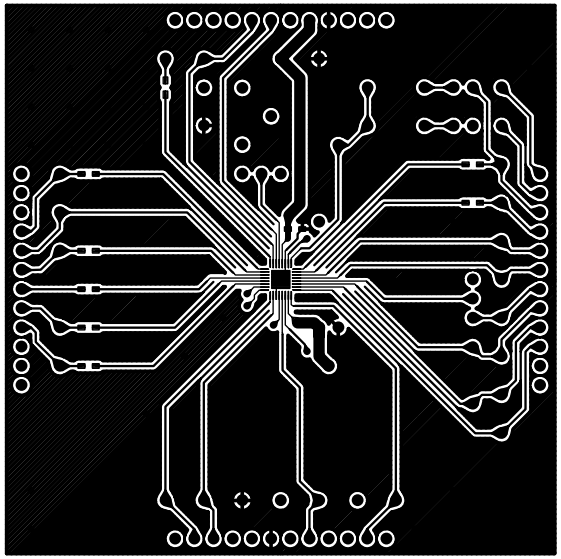

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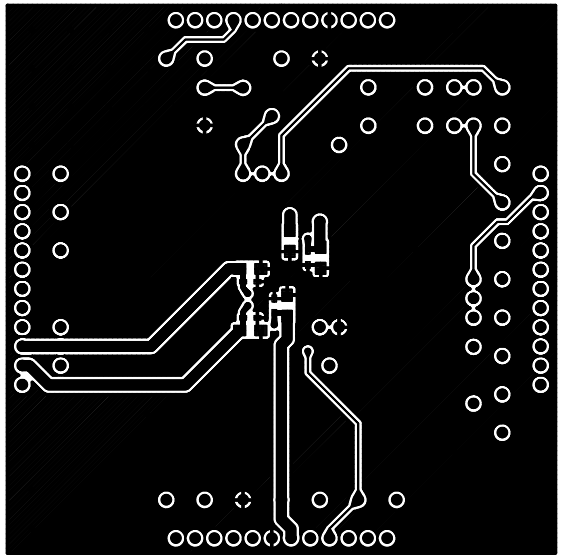

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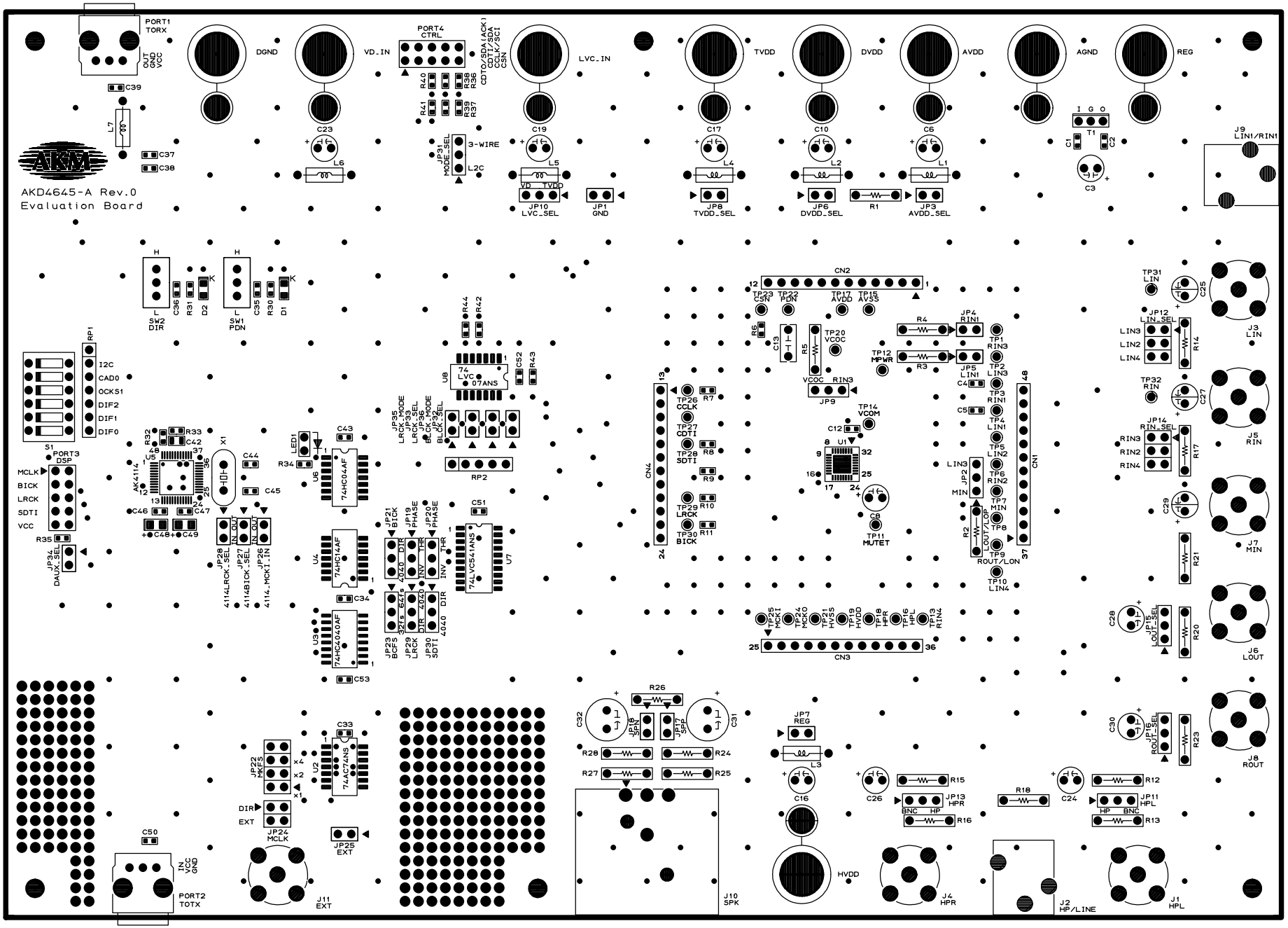

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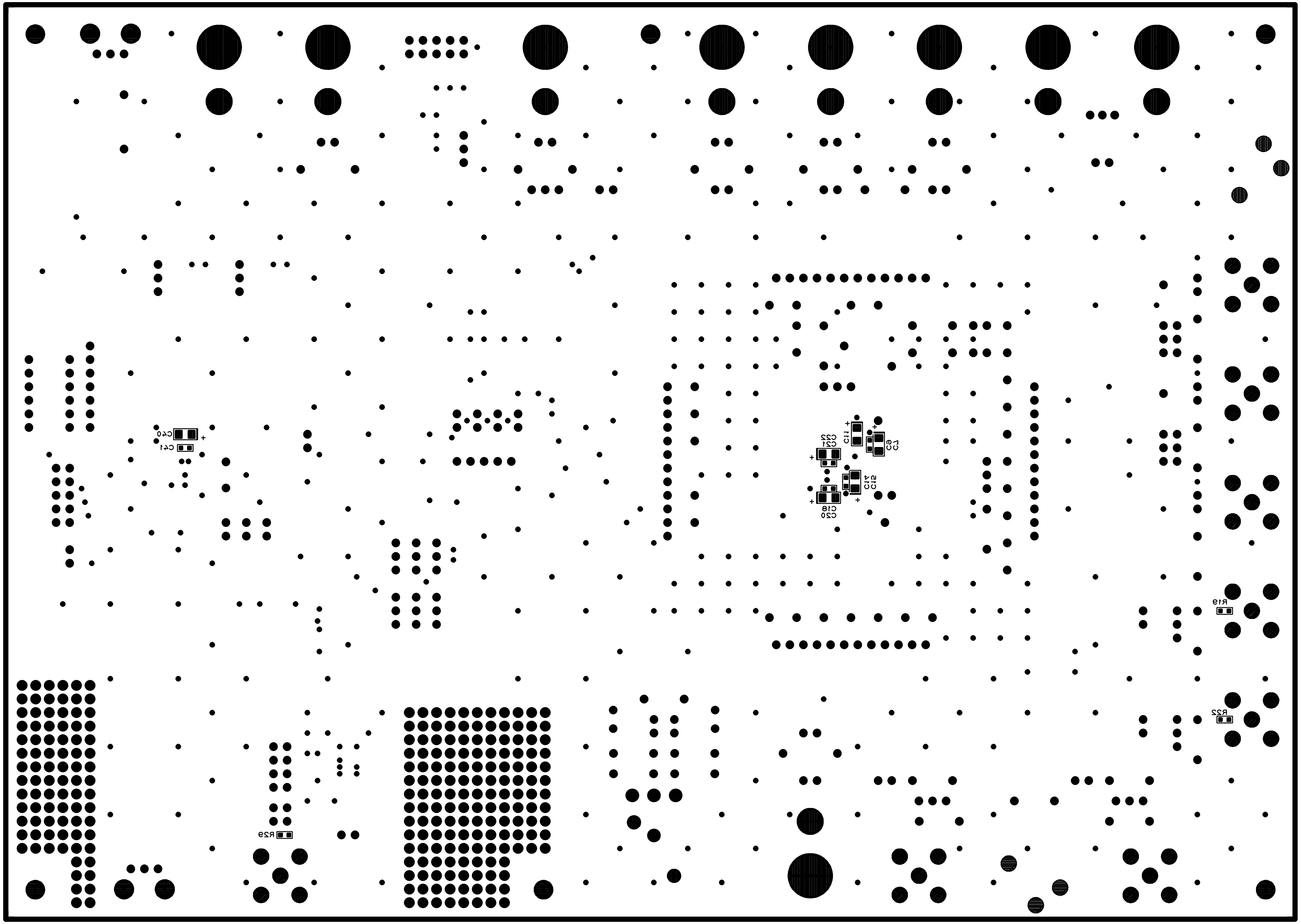

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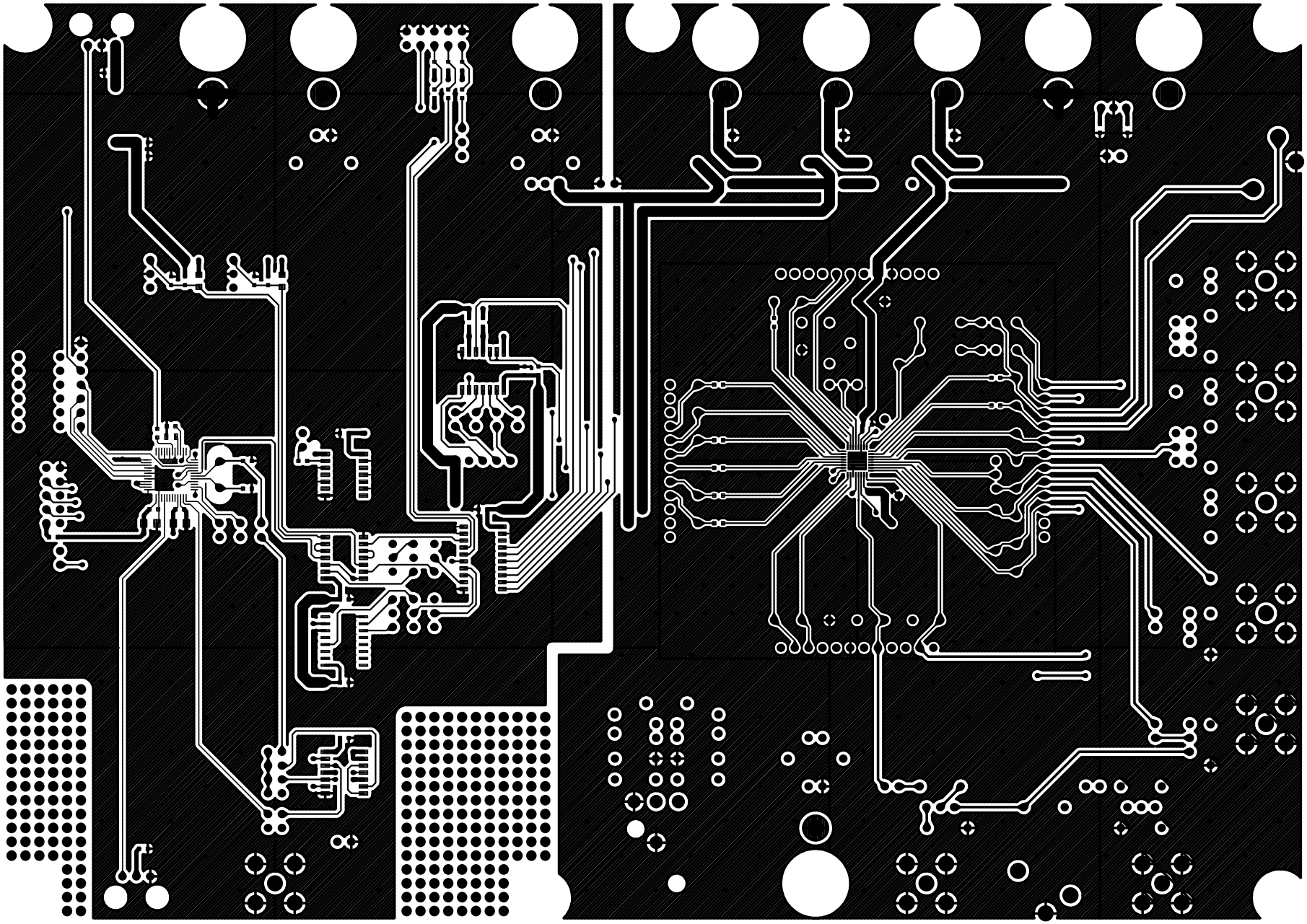

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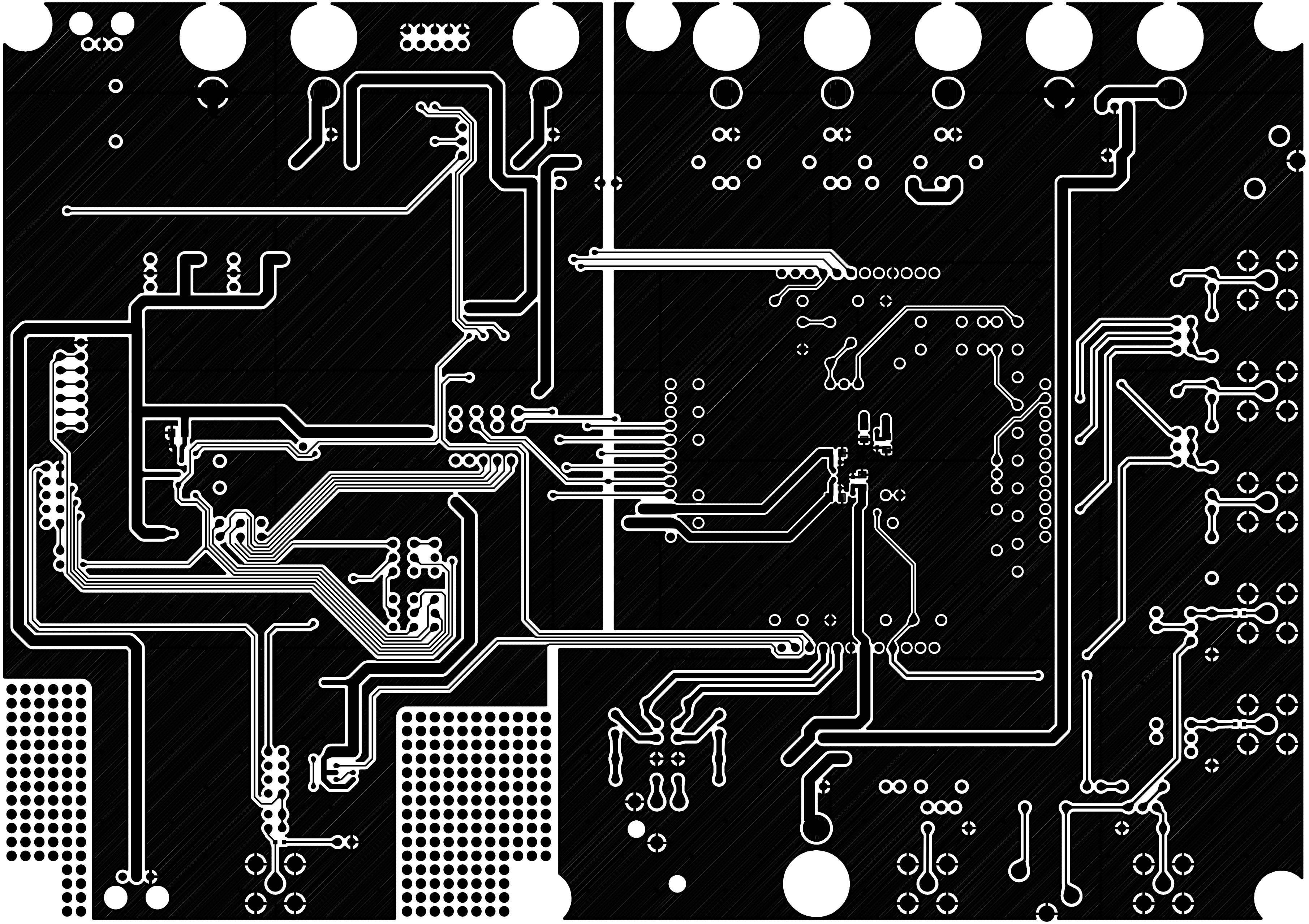

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