

AKM

AKD4687-A

Evaluation board Rev.2 for AK4687

GENERAL DESCRIPTION

AKD4687-A is an evaluation board for AK4687, which is a single chip 24bit CODEC with a 2ch ADC and a 2ch DAC. It is possible to evaluate not only A/D and D/A of the AK4687, but also asynchronous operation characteristics. Also, the board could be connected to a digital's audio equipment easily with S/PDIF connectors.

Ordering guide

AKD4687-A --- Evaluation board for AK4687
 (Cable for connecting with printer port of IBM-AT compatible PC and control software are packed with this. This control software does not operate on Windows NT.)

FUNCTION

- Compatible with 2 types of digital audio interface
 - BNC (S/PDIF) input/output with DIT/DIR (AK4118A)
 - 10pin headers for interfacing with external data source
- Separate power supply or regulator power supply
- 10pin header for register control

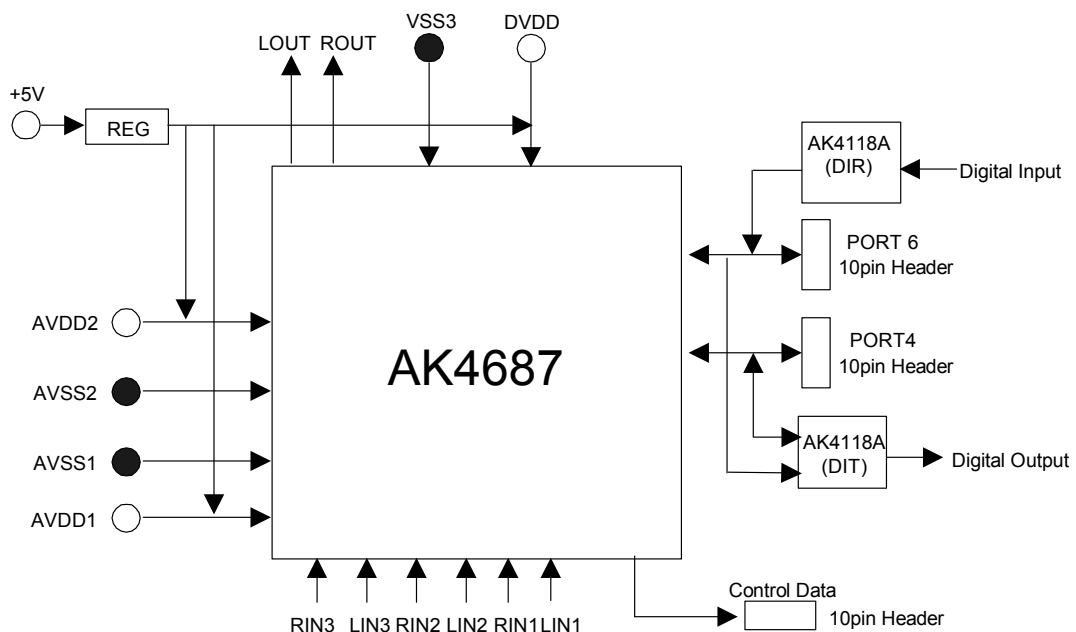


Figure 1. AKD4687 Block Diagram

* Circuit diagram and PCB layout are attached at the end of this manual.

Board Outline Chart

■ Outline Chart

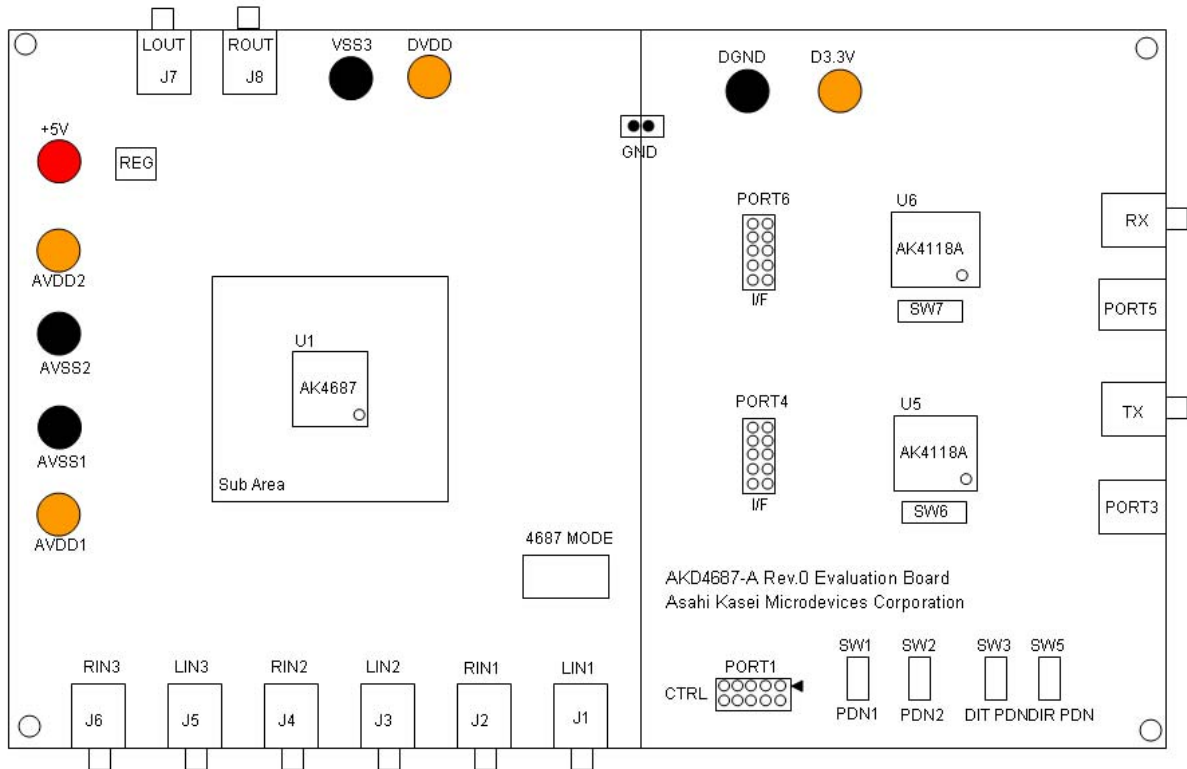


Figure 2. AKD4687-A Outline Chart

■ Comment

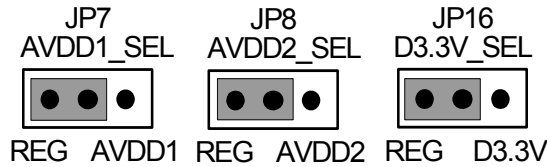
- (1) J1, J2, J3, J4, J5, J6, J7, J8, J10, J11 (RCA JACKS)
 - J1, J3, J5 (white): Analog signal input RCA-Jacks. The signals are input to LIN1/LIN2/LIN3 pins.
 - J2, J4, J6 (red): Analog signal input RCA-Jacks. The signals are input to RIN1/RIN2/RIN3 pins.
 - J7 (white): An analog signal output RCA-Jack. The signal is output from LOUT pin.
 - J8 (red): An analog signal output RCA-Jack. The signal is output from ROUT pin.
 - J10 (black): A digital signal output RCA-Jack. The signal is output from U5 (AK4118A).
 - J11 (black): A digital signal input RCA-Jack. The signal is input to U6 (AK4118A).
- (2) +5V, AVDD1, AVDD2, DVDD, D3.3V, AVSS1, AVSS2, VSS3, DGND
The power supply connectors which should be connected to power supplies.
Refer to the setup of power supply in P3 for more details.
- (3) PORT1 (10 pin header)
Control port. Connect the 10 wire flat cable bundled to this port.
- (4) PORT4, PORT6 (10 pin header)
Audio Interfaces that clocks and data can be input and output with.
- (5) PORT3, PORT5 (Optical Connector)
 - PORT5 (Input): Optical digital signal is input to U6 (AK4118A).
 - PORT3 (Output): Optical digital signal is output from U5 (AK4118A).

■ Operation sequence

1) Set up the power supply lines.

1-1) When AVDD1, AVDD2, DVDD and D3.3V are supplied from the regulator. <Default>

Set up the jumper pins.



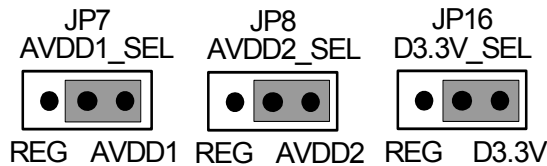
Set up the power supply lines.

Name	Color	Voltage	Comments
+5V	Red	+5V	Power supply for the regulator.
AVDD1	Orange	Open	Power supply for AVDD1 of AK4687.
AVDD2	Orange	Open	Power supply for AVDD2 of AK4687.
DVDD	Orange	Open	Power supply for DVDD of AK4687.
D3.3V	Orange	Open	Power supply for logic circuit.
AVSS1	Black	0V	Analog ground of AK4687's ADC.
AVSS2	Black	0V	Analog ground of AK4687's DAC.
VSS3	Black	0V	Analog ground of AK4687.
DGND	Black	0V	Logic circuit ground.

Table 1 Setup of power supply

1-2) When AVDD1, AVDD2, DVDD, and D3.3V are supplied from the power supply connectors.

Set up the jumper pins.



Set up the power supply lines.

Name	Color	Voltage	Comments
+5V	Red	Open	The regulator is not used.
AVDD1	Orange	3.0V~3.6V (typ3.3V)	Power supply for AVDD1 of AK4687.
AVDD2	Orange	3.0V~3.6V (typ3.3V)	Power supply for AVDD2 of AK4687.
DVDD	Orange	3.0V~3.6V (typ3.3V)	Power supply for DVDD of AK4687.
D3.3V	Orange	3.0V~3.6V (typ3.3V)	Power supply for logic circuit.
AVSS1	Black	3.0V~3.6V (typ3.3V)	Analog ground of AK4687's ADC.
AVSS2	Black	0V	Analog ground of AK4687's DAC.
VSS3	Black	0V	Analog ground of AK4687.
DGND	Black	0V	Logic circuit ground.

Table 2 Setup of power supply

- * Each supply line should be distributed from the power supply unit.
- AVDD1 and AVDD2 should be supplied as the same voltage level.
- The difference of voltage level between AVDD1, AVDD2 and DVDD should be under 0.3V.

2) Set up the evaluation mode, jumper pins and DIP switches. (See the followings.)

3) Power on.

AK4687 and AK4118A should be reset once bringing SW1, SW2, SW3, SW5 “L” upon power-up.

■ Evaluation mode

In case of AK4687 evaluation by using AK4118A, it is necessary to correspond to audio interface format for AK4687 and AK4118A. About AK4687's audio interface format, refer to the datasheet of AK4687. About AK4118A's audio interface format, refer to the datasheet of AK4118A.

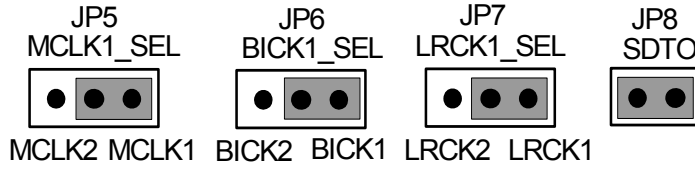
Applicable Evaluation Mode

- (1) Evaluation of A/D and D/A by using DIR/DIT: Asynchronous mode <Default>
- (2) All interface signals are fed externally.

(1) Evaluation of A/D and D/A by using DIR/DIT: Asynchronous mode <Default>

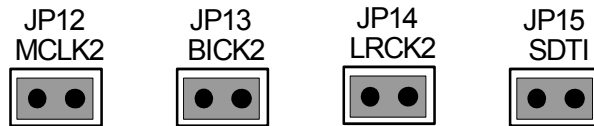
a) Set up of A/D

J10 TX (RCA-Jack) or PORT3 (Optical connector) is used.
Nothing should be connected to PORT4.



b) Set up of D/A

J11 RX (RCA-Jack) or PORT5 (Optical connector) is used.
Nothing should be connected to PORT6.

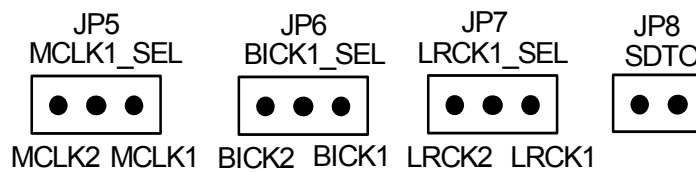


(2) All interface signals are fed externally.

In case of evaluating A/D and D/A of the AK4687 on synchronous mode, synchronize clock signals and data signals between A/D and D/A.

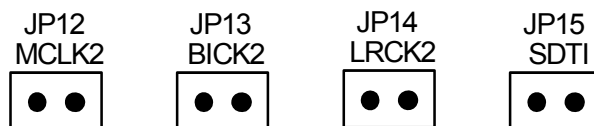
a) Set up A/D

PORT4 is used.
Nothing should be connected to J10 TX (RCA-Jack) or PORT3 (Optical connector).



b) Set up of D/A

PORT6 is used.
Nothing should be connected to J11 RX (RCA-Jack) or PORT5 (Optical connector).



■ DIP Switch set up

[SW4] (4687 Mode): Mode settings of AK4687

No.	Name	OFF ("L")	ON ("H")	Default
1	I2C	H/W Control	I2C Control	L
2	AIN1	Analog Input Selector Control (I2C = "L") (Refer to Table 7)		L
3	AIN0			L
4	MSN	ADC Slave Mode	ADC Master Mode	L
5	CAD0/CKS	CAD Address pin Control (I2C = "H") ADC Master Clock Speed Control (I2C = "L")		L
6	TEST1	For AK4687's TEST MODE (Fixed to "L")		L
7	TEST2	For AK4687's TEST MODE (Fixed to "L")		L

Table 3. Mode settings of AK4687

AK4687 Register Settings		AK4118A (U5) SW6 Settings		Audio I/F Format	
MSN pin	DIF1 bit	DIF1	DIF0		
L	0	L	L	24bit, Left justified	<Default>
L	1	L	H	24bit, I ² S	
H	0	H	L	24bit, Left justified	
H	1	H	H	24bit, I ² S	

Table 4. ADC Audio I/F Format Settings

AK4687 Register Settings		AK4118A (U6) SW7 Settings			Audio I/F Format	
DIF21 bit	DIF20 bit	DIF2	DIF1	DIF0		
0	0	L	L	L	16bit, Right justified	<Default>
0	1	L	H	H	24bit, Right justified	
1	0	H	L	L	24bit, Left justified	
1	1	H	L	H	24bit, I ² S	

Table 5. DAC Audio I/F Format Settings

No.	OCKS1	OCKS0	MCKO1	X'tal	fs (max)
0	L	L	256fs	256fs	96kHz
1	L	H	256fs	256fs	96kHz
2	H	L	512fs	512fs	48kHz
3	H	H	128fs	128fs	192kHz

Table 6. AK4118A Master Clock Speed Control

AIN1 pin	AIN0 pin	Input Selector	
L	L	LIN1 / RIN1	<Default>
L	H	LIN2 / RIN2	
H	L	LIN3 / RIN3	
H	H	Reserved	

Table 7. ADC Input Selector Control (H/W Control Mode)

CKS pin	Master Clock Speed	
H	256fs	<Default>
L	768fs	

Table 8. ADC Master Clock Speed Control (Master Mode, H/W Control Mode)

■ Other jumper pins set up

1. JP1 (GND)
 - OPEN : Analog ground and digital ground are separated.
 - SHORT : Analog ground and digital ground are shorted. <Default>

2. JP1 (SCL/AIN0)
 - SCL : Control data clock on the I2C mode.
 - AIN0 : Analog input selector control on the H/W control mode. < Default >

3. JP2 (SDA/AIN1)
 - SDA : Control data on the I2C mode.
 - AIN1 : Analog input selector control on the H/W control mode. < Default >

4. JP9 (TX)
 - BNC : Digital signals are output via the BNC connector. < Default >
 - OPT : Digital signals are output via the optical connector.

5. JP10 (RX)
 - BNC : Digital signals are output via the BNC connector. < Default >
 - OPT : Digital signals are output via the optical connector.

■ The function of the toggle SW

- [SW1] (4687 PDN1) : Power down control of AK4687's ADC. Keep "H" during normal operation.
AK4687 should be reset once bringing SW1 "L" upon power-up.
- [SW2] (4687 PDN2) : Power down control of AK4687's DAC. Keep "H" during normal operation.
AK4687 should be reset once bringing SW1 "L" upon power-up.
- [SW3] (DIT PDN) : Power down control of U5 (AK4118A). Keep "H" during normal operation.
Keep "L" when AK4118A is not used.
- [SW5] (DIR PDN) : Power down control of U6 (AK4118A). Keep "H" during normal operation.
Keep "L" when AK4118A is not used.

■ **Serial Control**

The AK4687 can be controlled via the printer port (parallel port) of IBM-AT compatible PC. Connect PORT1 (CTRL) with PC by 10 wire flat cable packed with the AKD4687-A

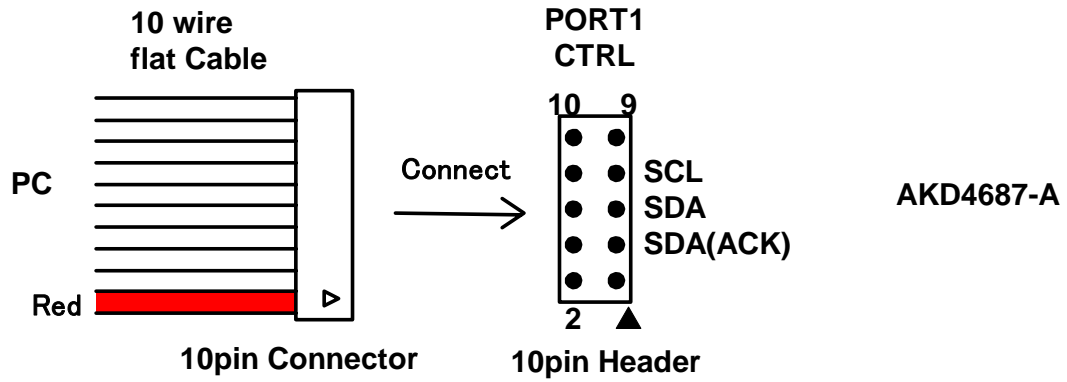


Figure 3. Connect of 10 wire flat cable

■ Analog Input/Output Circuits

(1) Input Circuits

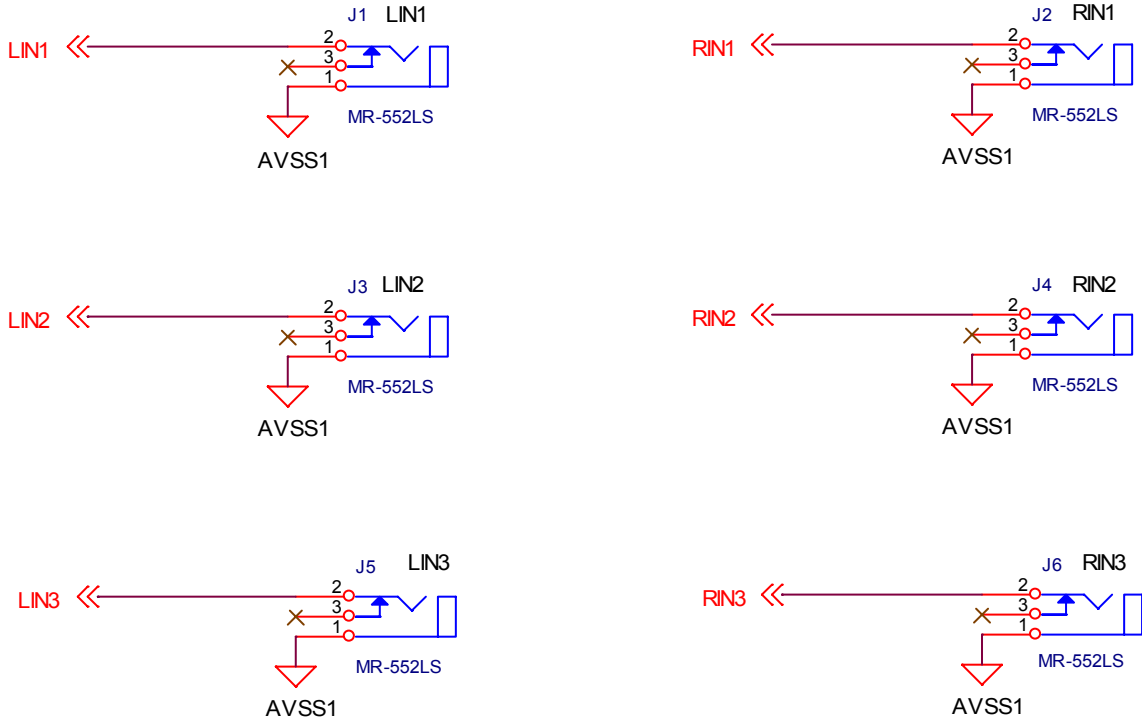


Figure 4. Analog Input Circuit

(2) Output Circuits

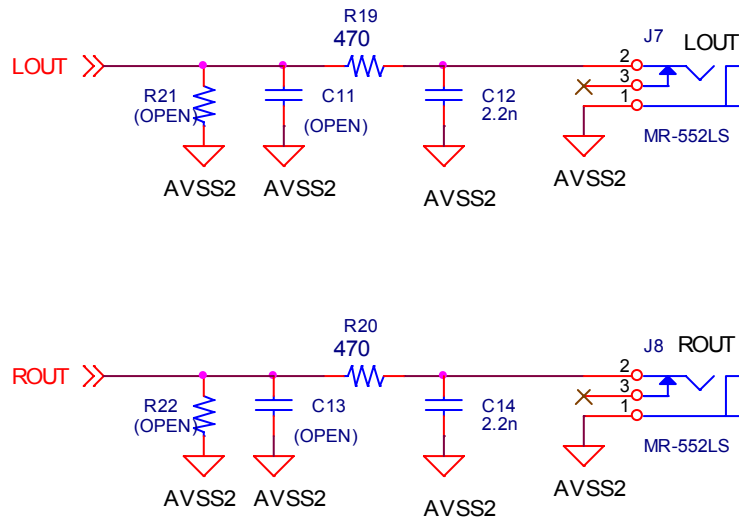


Figure 5. Analog Output Circuit

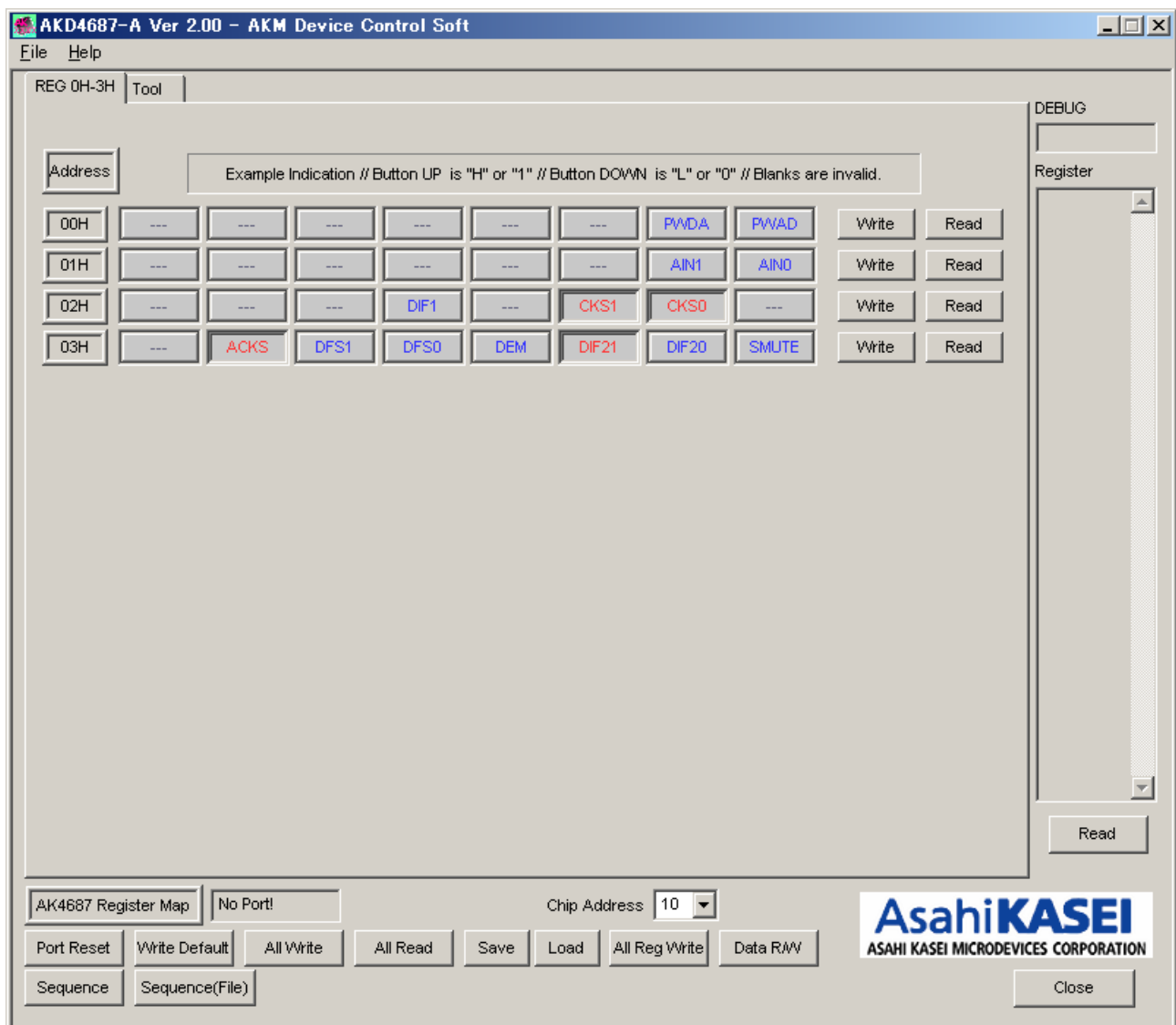
Control Soft Manual

■ Evaluation Board and Control Soft Settings

1. Set an evaluation board properly.
2. Connect the evaluation board to an IBM PC/AT compatible PC by a 10 wire flat cable. Be care of the direction of the 10pin header. Before running this control soft on Windows 2000/XP, the driver included in the CD must be installed. Refer to the “Driver Control Install Manual for AKM Device Control Software” for installation of the driver. When running this control soft on Windows 95/98/ME or via an AKDUSBIF-B interface board, driver installing is not necessary.
3. Continue to evaluate by following steps.

■ Operation Screen

1. Start up the control program, and the operation screen is shown below.



■ Operation Overview

Register map and testing tool can be controlled by this control soft. These controls are selected by upper tabs.

Buttons which are frequently used such as register initializing button “Write Default”, are located outside of the switching tab window. Refer to the “■ Dialog Boxes” for details of each dialog box setting.

1. [Port Reset]: For when connecting to USB I/F board (AKDUSBIF-A)
Click this button after the control soft starts up when connecting USB I/F board (AKDUSBIF-A).
2. [Write Default]: Register Initializing
When the device is reset by a hardware reset, use this button to initialize the registers.
3. [All Write]: Executing write commands for all registers displayed.
4. [All Read]: Executing read commands for all registers displayed.
5. [Save]: Saving current register settings to a file.
6. [Load]: Executing data write from a saved file.
7. [All Reg Write]: “All Reg Write” dialog box is popped up.
8. [Data R/W]: “Data R/W” dialog box is popped up.
9. [Sequence]: “Sequence” dialog box is popped up.
10. [Sequence(File)]: “Sequence(File)” dialog box is popped up.
11. [Read]: Reading current register settings and display on to the Register area (on the right of the main window).
This is different from [All Read] button, it does not reflect to a register map, only displaying hexadecimal.

■ Tab Functions

1. [REG 0H~5H]: Register Map

This tab is for register writing and reading.

Each bit on the register map is a push-button switch.

Button Down indicates “H” or “1” and the bit name is in red (when read only it is in deep red).

Button Up indicates “L” or “0” and the bit name is in blue (when read only it is in gray)

The registers which is not defined in the datasheet are indicated as “---”.

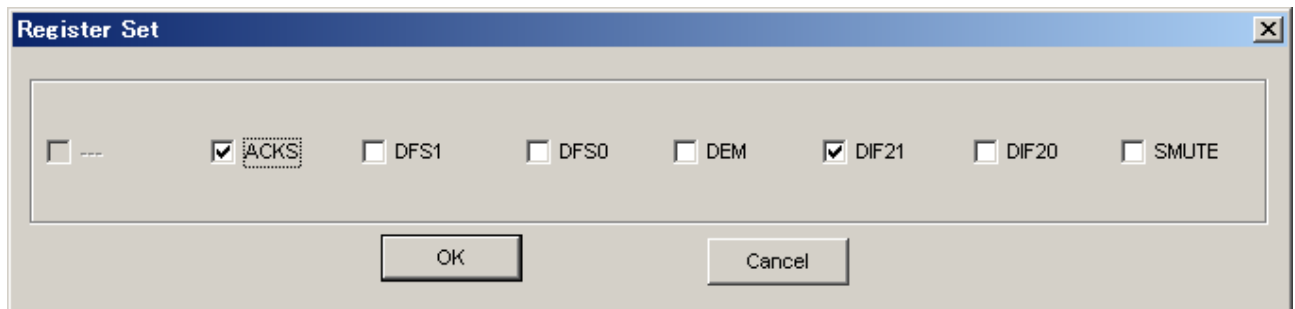
00H	---	---	---	---	---	---	PWDA	PWAD	Write	Read
01H	---	---	---	---	---	---	AIN1	AIN	Write	Read
02H	---	---	---	DIF1	---	CKS1	CKS0	---	Write	Read
03H	---	ACKS	DFS1	DFS0	DEM	DIF21	DIF20	SMUTE	Write	Read

[Write]: Data Writing Dialog

It is for when changing two or more bits on the same address at the same time.

Click [Write] button located on the right of the each corresponded address for a pop-up dialog box.

When checking the checkbox, the register will be “H” or “1”, when not checking the register will be “L” or “0”.
Click [OK] to write setting value to the registers, or click [Cancel] to cancel this setting.

**[Read]: Data Read**

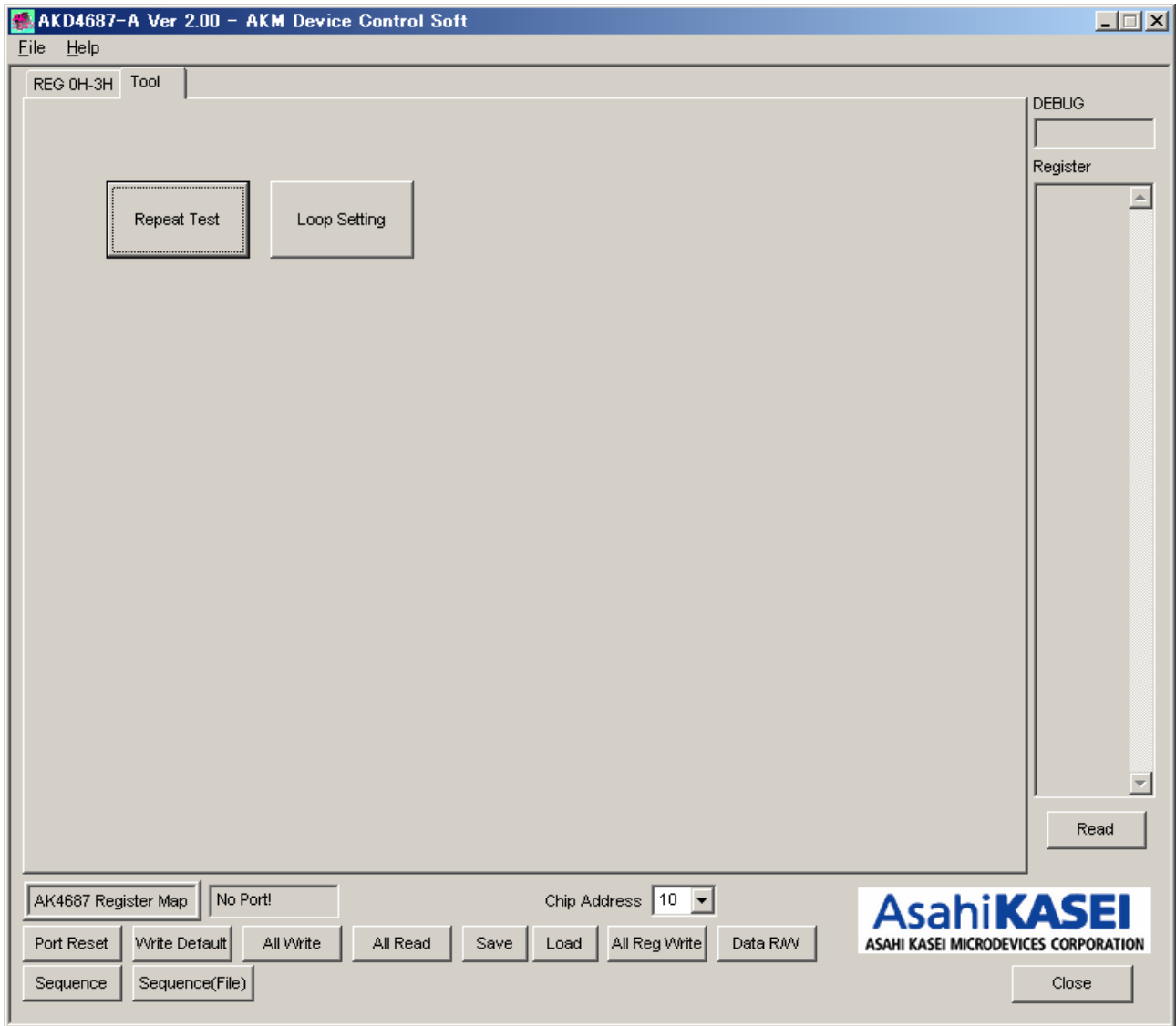
Click [Read] button located on the right of the each corresponded address to execute register reading.

After register reading, the display will be updated regarding to the register status.
Button Down indicates “H” or “1” and the bit name is in red (when read only it is in deep red).
Button Up indicates “L” or “0” and the bit name is in blue (when read only it is in gray)

Please be aware that button statuses will be changed by Read command.

2. [Tool]: Testing Tools

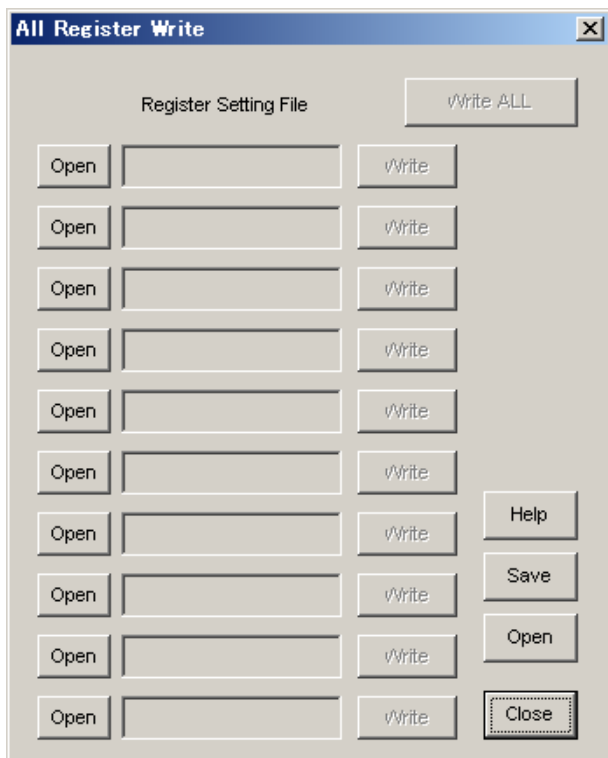
This tab screen is for evaluation testing tool.
Click buttons for each testing tool.



■ Dialog Boxes

1. [All Req Write]: All Req Write dialog box

Click [All Reg Write] button in the main window to open register setting files.
Register setting files saved by [SAVE] button can be applied.



[Open (left)]: Selecting a register setting file (*.akr).

[Write]: Executing register writing.

[Write All]: Executing all register writings.

Writings are executed in descending order.

[Help]: Help window is popped up.

[Save]: Saving the register setting file assignment. The file name is "*.mar".

[Open (right)]: Opening a saved register setting file assignment "*.mar".

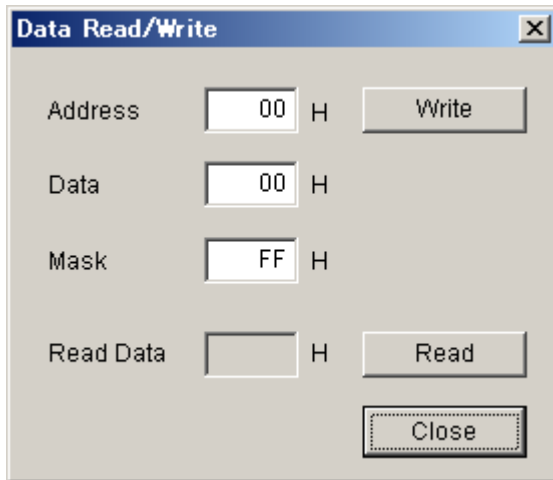
[Close]: Closing the dialog box and finish the process.

*Operating Suggestions

- (1) Those files saved by [Save] button and opened by [Open] button on the right of the dialog "*.mar" should be stored in the same folder.
- (2) When register settings are changed by [Save] button in the main window, re-read the file to reflect new register settings.

2. [Data R/W]: Data R/W Dialog Box

Click the [Data R/W] button in the main window for data read/write dialog box.
Data write is available to specified address.



Address Box: Input data address in hexadecimal numbers for data writing.

Data Box: Input data in hexadecimal numbers.

Mask Box: Input mask data in hexadecimal numbers.

This is “AND” processed input data.

[Write]: Writing to the address specified by “Address” box.

[Read]: Reading from the address specified by “Address” box.

The result will be shown in the Read Data Box in hexadecimal numbers.

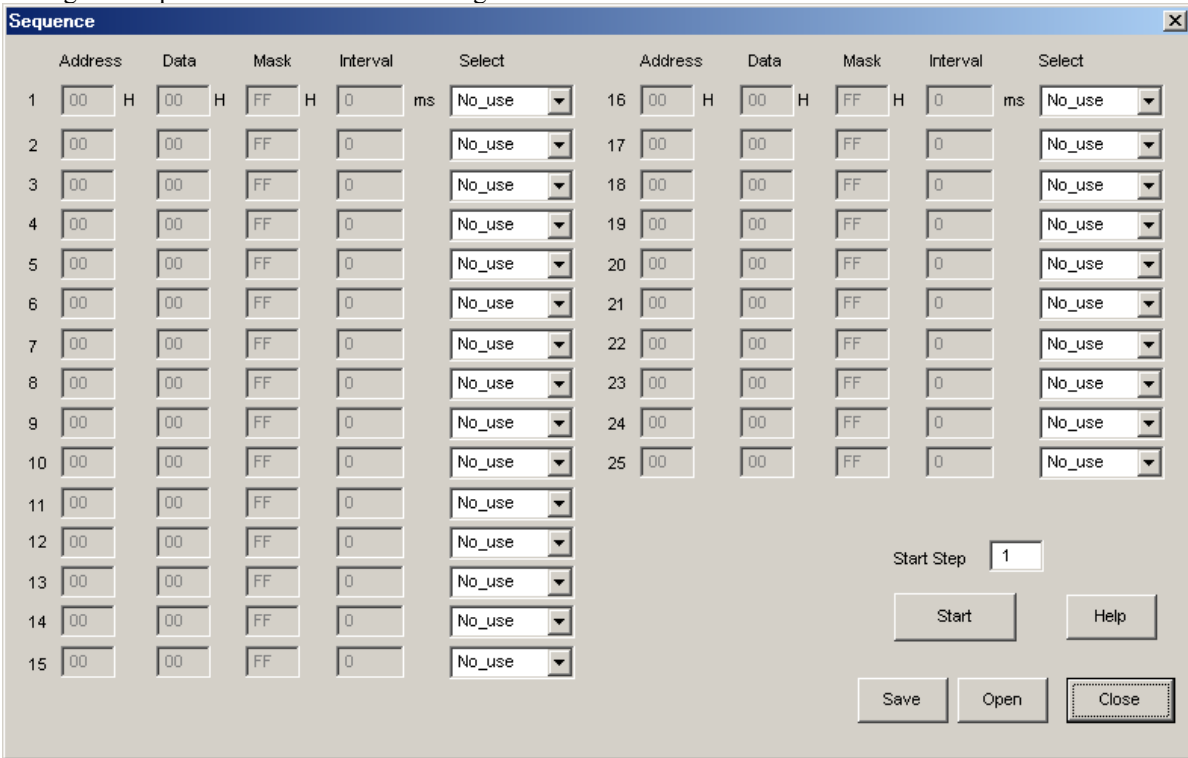
[Close]: Closing the dialog box and finish the process.

Data writing can be cancelled by this button instead of [Write] button.

*The register map will be updated after executing [Write] or [Read] commands.

3. [Sequence]: Sequence Dialog Box

Click [Sequence] button to open register sequence setting dialog box.
 Register sequence can be set in this dialog box.



Sequence Setting

Set register sequence by following process bellow.

(1) Select a command

Use [Select] pull-down box to choose commands.
 Corresponding boxes will be valid.

< Select Pull-down menu >

- No_use: Not using this address
- Register: Register writing
- Reg(Mask): Register writing (Masked)
- Interval: Taking an interval
- Stop: Pausing the sequence
- End: Finishing the sequence

(1) Input sequence

[Address]: Data address

[Data]: Writing data

[Mask]: Mask

[Data] box data is ANDed with [Mask] box data. This is the actual writing data.
 When Mask = 0x00, current setting is hold.

When Mask = 0xFF, the 8bit data which is set in the [Data] box is written.

When Mask = 0x0F, lower 4bit data which is set in the [Data] box is written.
 Upper 4bit is hold to current setting.

[Interval]: Interval time

Valid boxes for each process command are shown bellow.

- No_use: None
- Register: [Address], [Data], [Interval]
- Reg(Mask): [Address], [Data], [Mask], [Interval]
- Interval: [Interval]
- Stop: None
- End: None

Control Buttons

The function of Control Button is shown bellow.

[Start]: Executing the sequence

[Help]: Opening a help window

[Save]: Saving sequence settings as a file. The file name is “*.aks”.

[Open]: Opening a sequence setting file “*.aks”.

[Close]: Closing the dialog box and finish the process.

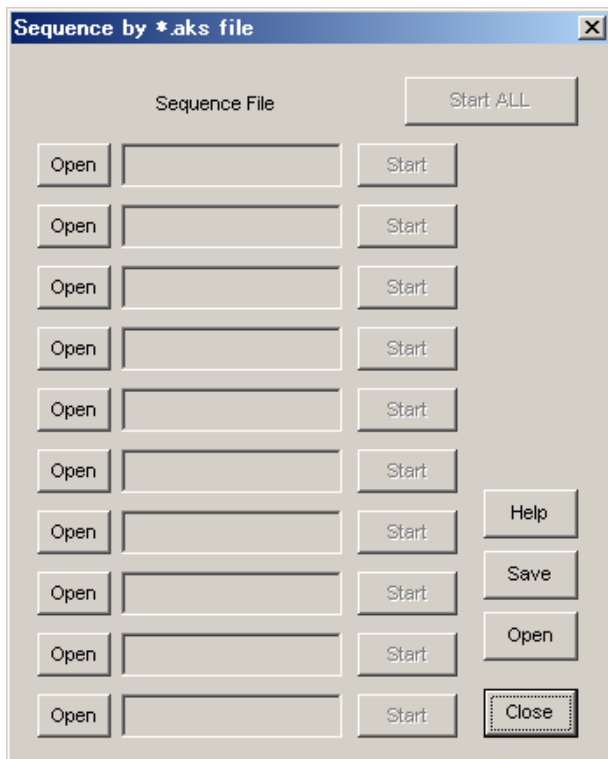
Stop of the sequence

When “Stop” is selected in the sequence, processing is paused and it starts again when [Start] button is clicked. Restarting step number is shown in the “Start Step” box. When finishing the process until the end of sequence, “Start Step” will return to “1”.

The sequence can be started from any step by writing the step number to the “Start Step” box. Write “1” to the “Start Step” box and click [Start] button, when restarting the process from the beginning.

4. [Sequence(File)]: Sequence Setting File Dialog Box

Click [Sequence(File)] button to open sequence setting file dialog box.
Those files saved in the “Sequence setting dialog” can be applied in this dialog.



[Open (left)]: Opening a sequence setting file (*.aks).

[Start]: Executing the sequence setting.

[Start All]: Executing all sequence settings.

Sequences are executed in descending order.

[Help]: Pop up the help window.

[Save]: Saving sequence setting file assignment. The file name is “*.mas”.

[Open(right)]: Opening a saved sequence setting file assignment “*. mas”.

[Close]: Closing the dialog box and finish the process.

*Operating Suggestions

- (1) Those files saved by [Save] button and opened by [Open] button on the right of the dialog “*.mas” should be stored in the same folder.
- (2) When “Stop” is selected in the sequence the process will be paused and a pop-up message will appear. Click “OK” to continue the process.



MEASUREMENT RESULTS

1. ADC part

[Measurement condition]

- Measurement unit : Audio Precision SYS-2722
- MCLK : 256fs
- BICK : 64fs
- fs : 48kHz
- BW : 20Hz~20kHz (fs=48kHz)
- Bit : 24bit
- Power Supply : AVDD1=AVDD2=DVDD=3.3V
- Temperature : Room
- Rf : 39k Ω
- Ri : 47k Ω
- Input Voltage : 2.34Vrms

Parameter	Input signal	Measurement filter	Results [dB]	
			Lch	Rch
S/(N+D)	1kHz, -1dBFS	20kHz LPF	83.1	82.7
DR	1kHz, -60dBFS	20kHz LPF, A-weighted	98.5	99.5
S/N	No signal	20kHz LPF, A-weighted	98.5	99.6

2. DAC part

[Measurement condition]

- Measurement unit : Audio Precision SYS-2722
- MCLK : 512fs (fs=48kHz), 256fs (fs=96kHz), 128fs (fs=192kHz)
- BICK : 64fs
- fs : 48kHz, 96kHz, 192kHz
- BW : 20Hz~20kHz (fs=48kHz), 20Hz~40kHz (fs=96kHz), 20Hz~40kHz (fs=192kHz)
- Resolution : 24bit
- Power Supply : AVDD1=AVDD2=DVDD=3.3V
- Temperature : Room

fs=48kHz

Parameter	Input signal	Measurement filter	Results [dB]	
			Lch	Rch
S/(N+D)	1kHz, 0dB	20kHz SPCL	95.0	95.1
DR	1kHz, -60dB	20kHz SPCL, A-weighted	105.5	105.7
S/N	“0” data	20kHz SPCL, A-weighted	105.7	105.8

fs=96kHz

Parameter	Input signal	Measurement filter	Results [dB]	
			Lch	Rch
S/(N+D)	1kHz, 0dB	40kHz SPCL	94.2	94.4
DR	1kHz, -60dB	40kHz SPCL, A-weighted	105.5	105.7
S/N	“0” data	40kHz SPCL, A-weighted	105.7	105.7

fs=192kHz

Parameter	Input signal	Measurement filter	Results [dB]	
			Lch	Rch
S/(N+D)	1kHz, 0dB	40kHz SPCL	93.1	93.3
DR	1kHz, -60dB	40kHz SPCL, A-weighted	105.6	105.6
S/N	“0” data	40kHz SPCL, A-weighted	105.7	105.5

1. ADC part

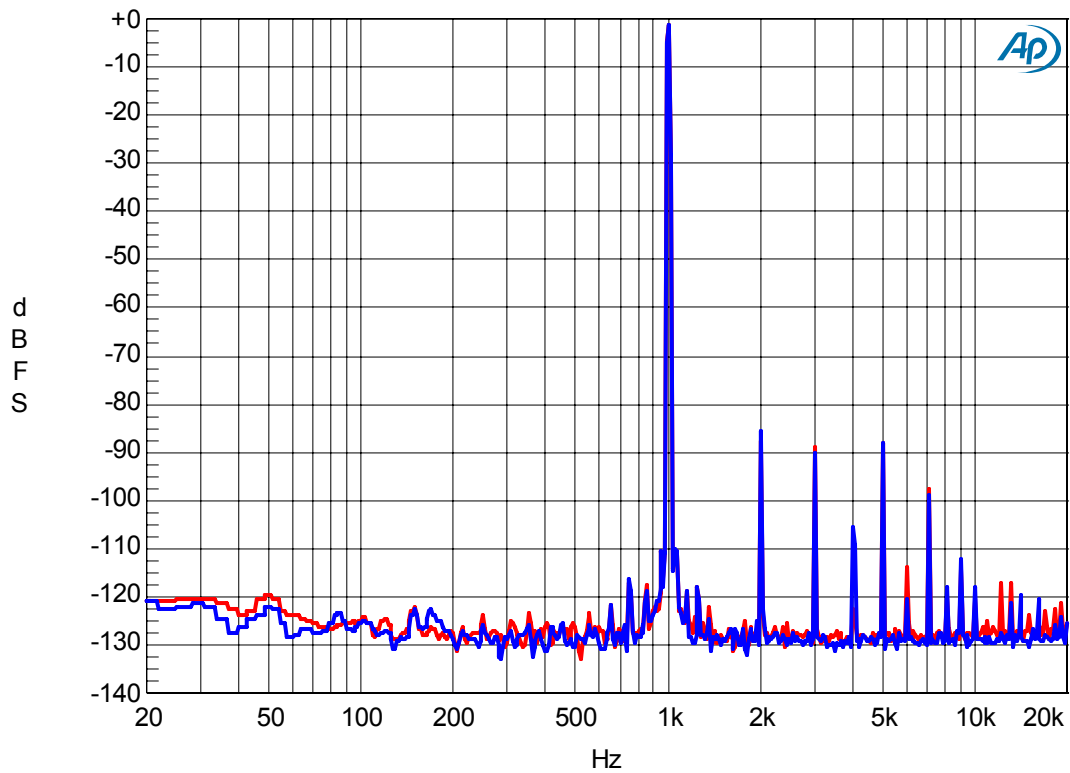


Figure 6. FFT (Input Frequency =1kHz, Input Level=-1dBFS)

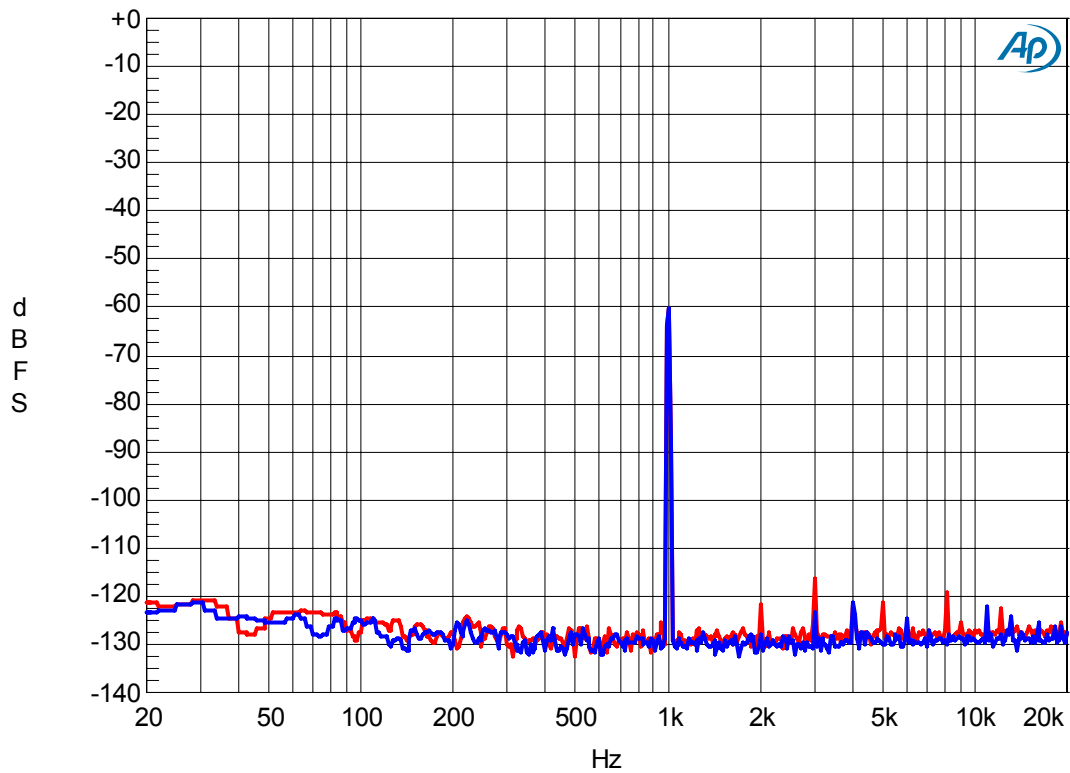


Figure 7. FFT(Input Frequency =1kHz, Input Level=-60dBFS)

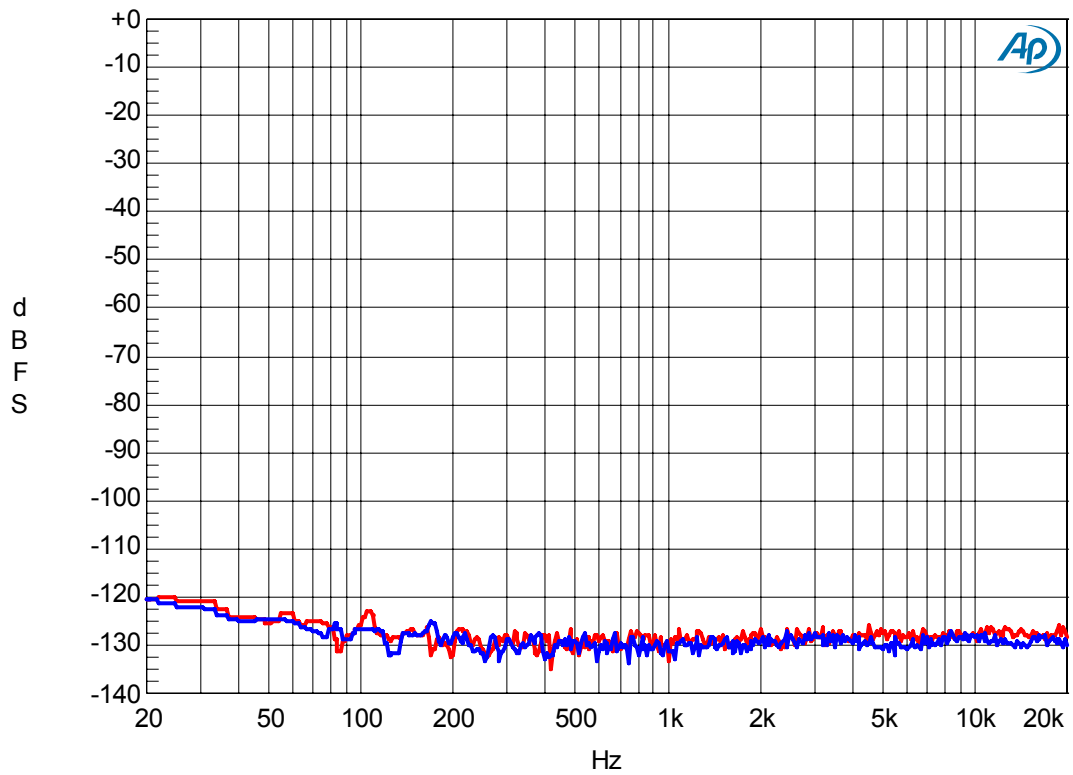


Figure 8. FFT(noise floor)

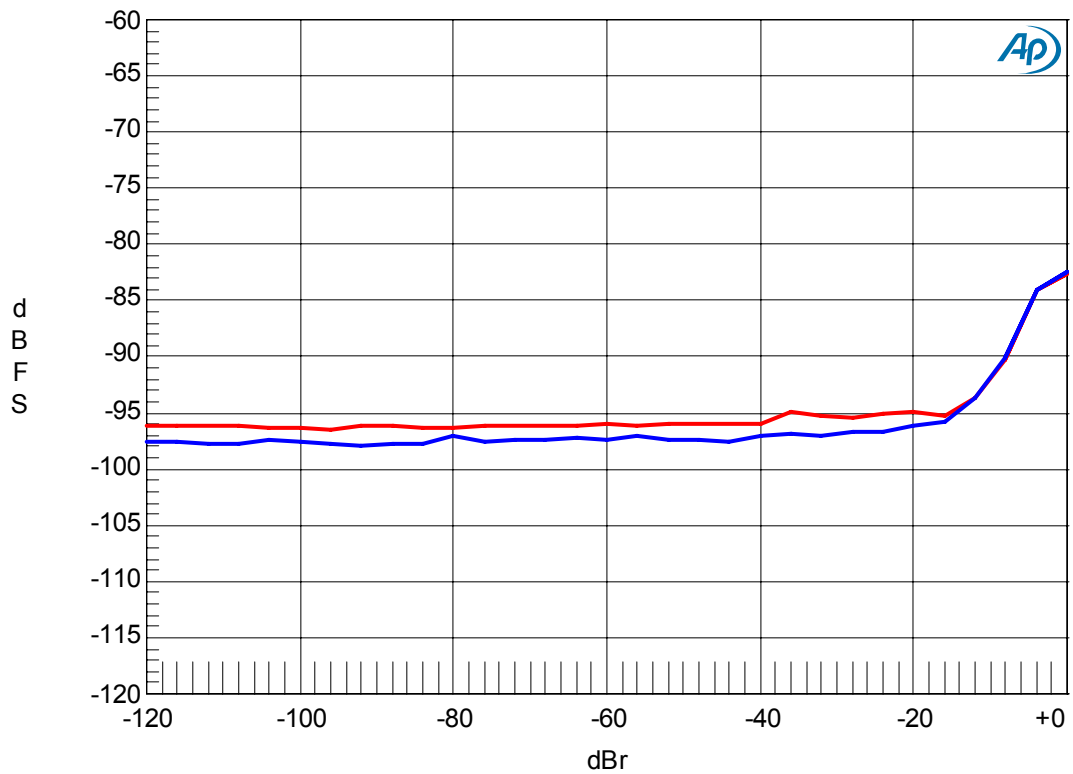


Figure 9. THD + N vs Input Level (Input Frequency =1kHz)

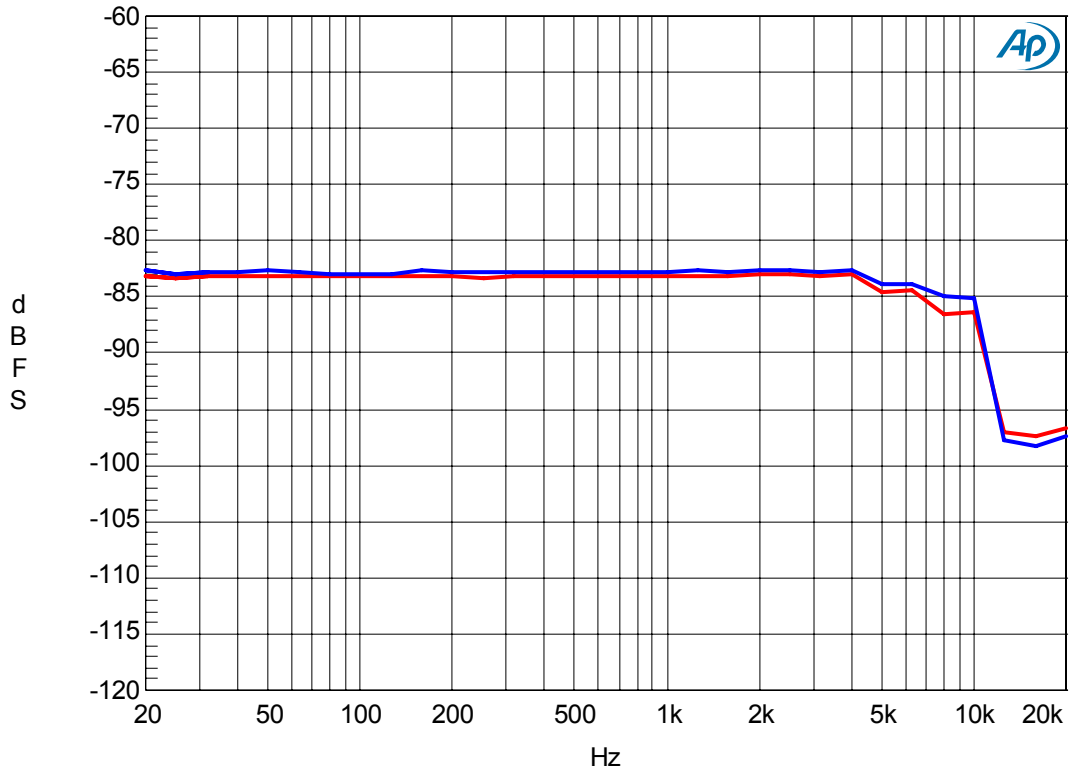


Figure 10. THD + N vs Input Frequency (Input Level=-1.0dBFS)

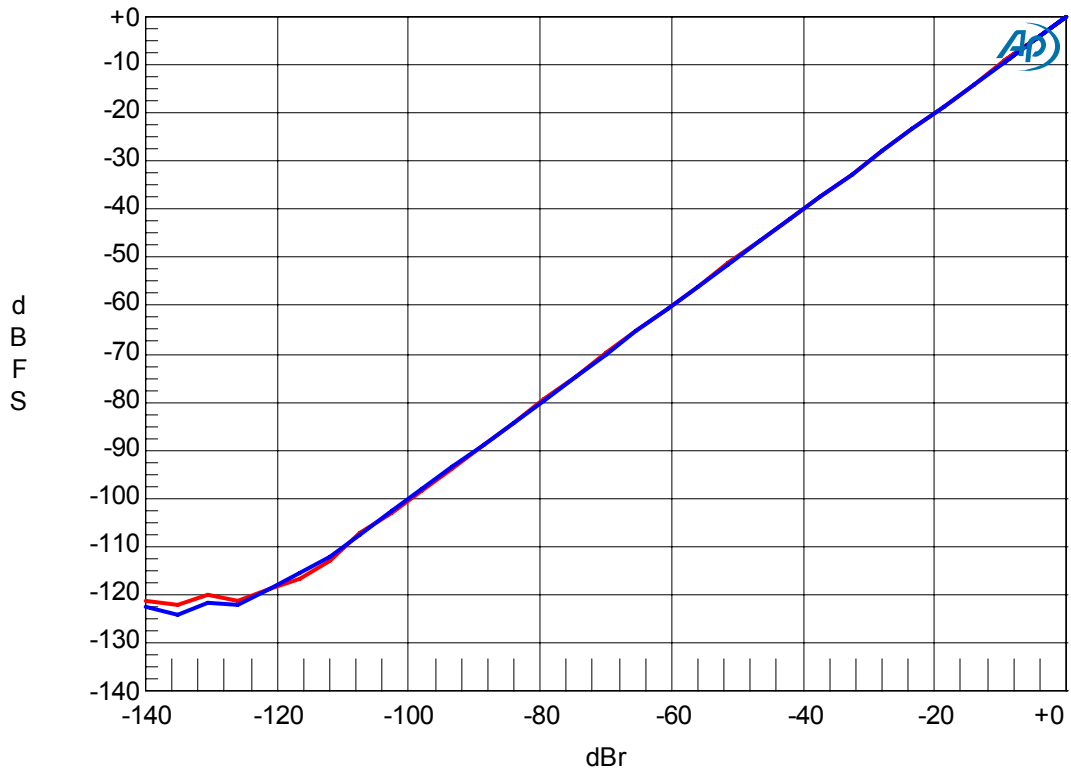


Figure 11. Linearity (Input Frequency =1kHz)

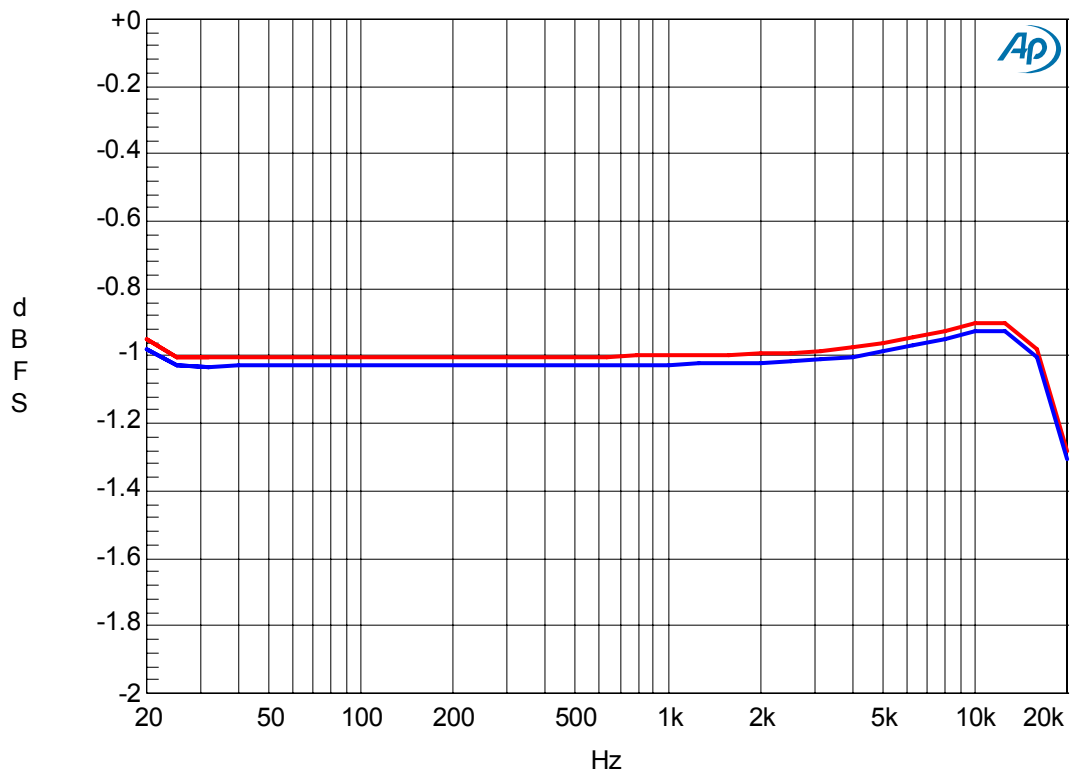


Figure 12. Frequency Response (Input Level=-1.0dBFS)

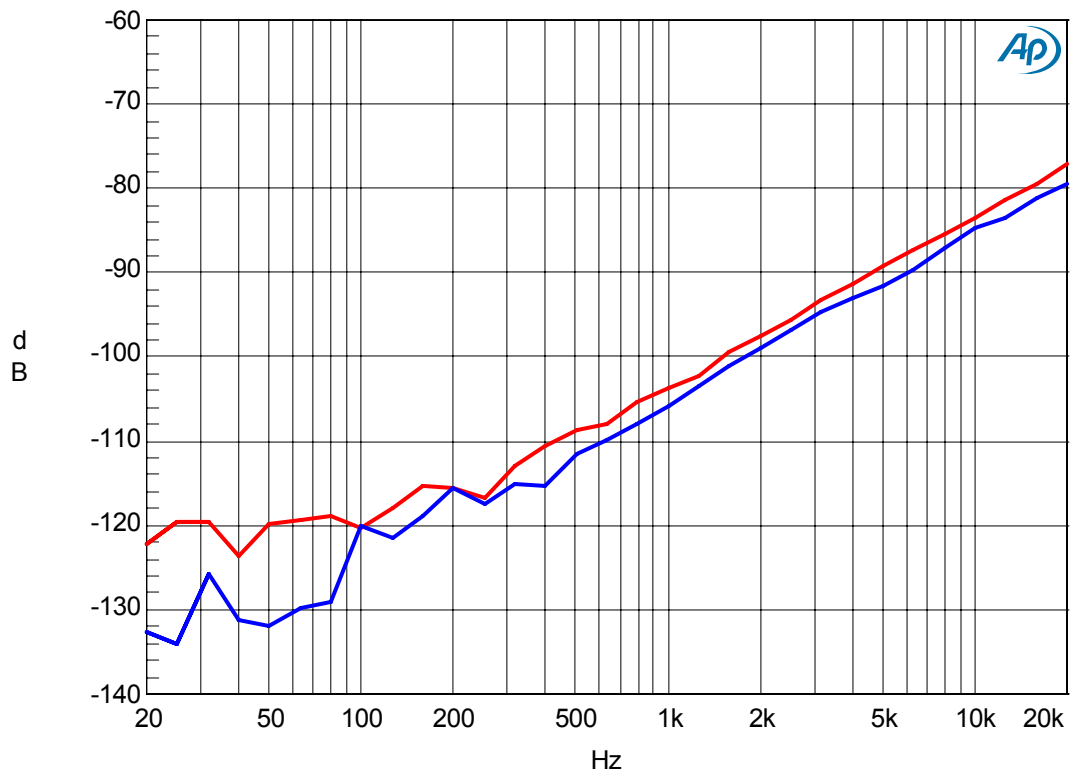


Figure 13. Crosstalk (Input Level=-1.0dBFS)

2-1. DAC part (fs=48kHz)

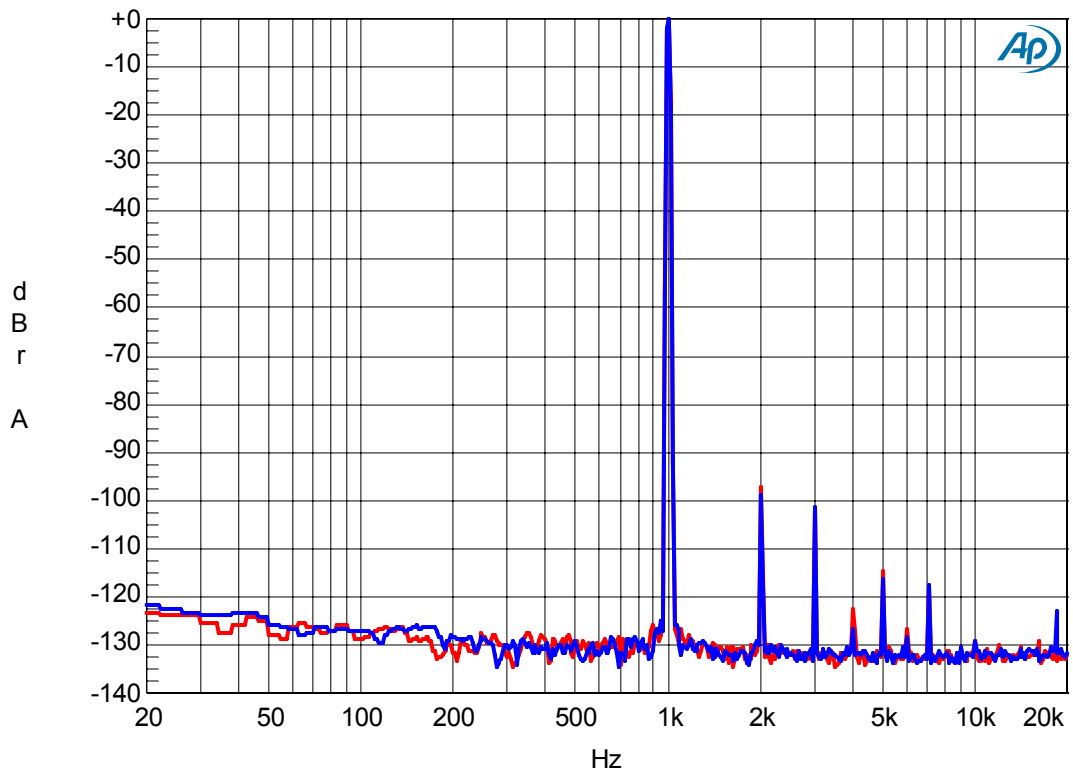


Figure 14. FFT(Input Frequency =1kHz, Input Level=0dBFS)

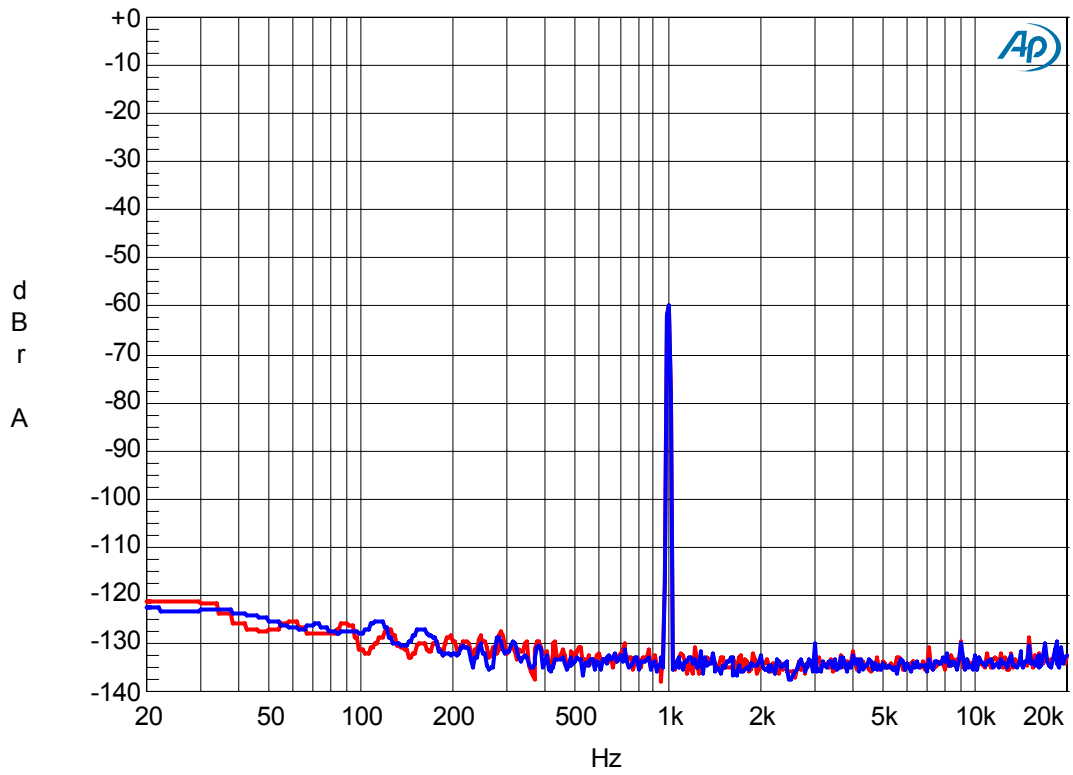


Figure 15. FFT(Input Frequency =1kHz, Input Level=-60dBFS)

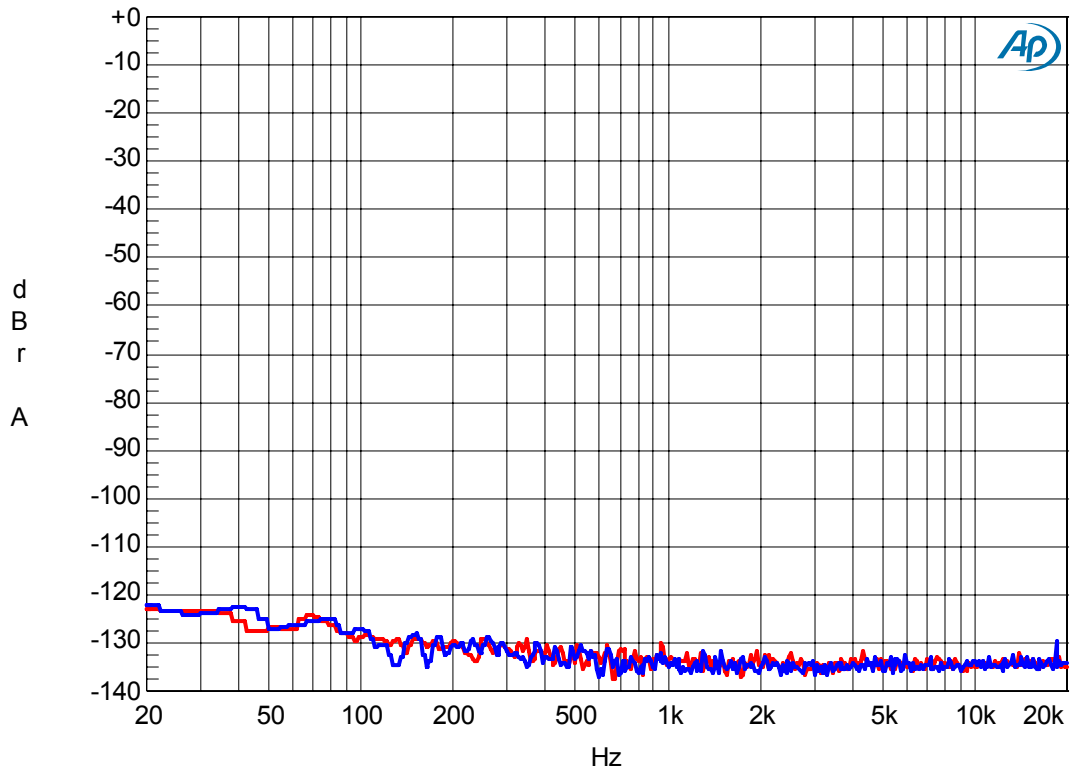


Figure 16. FFT(noise floor)

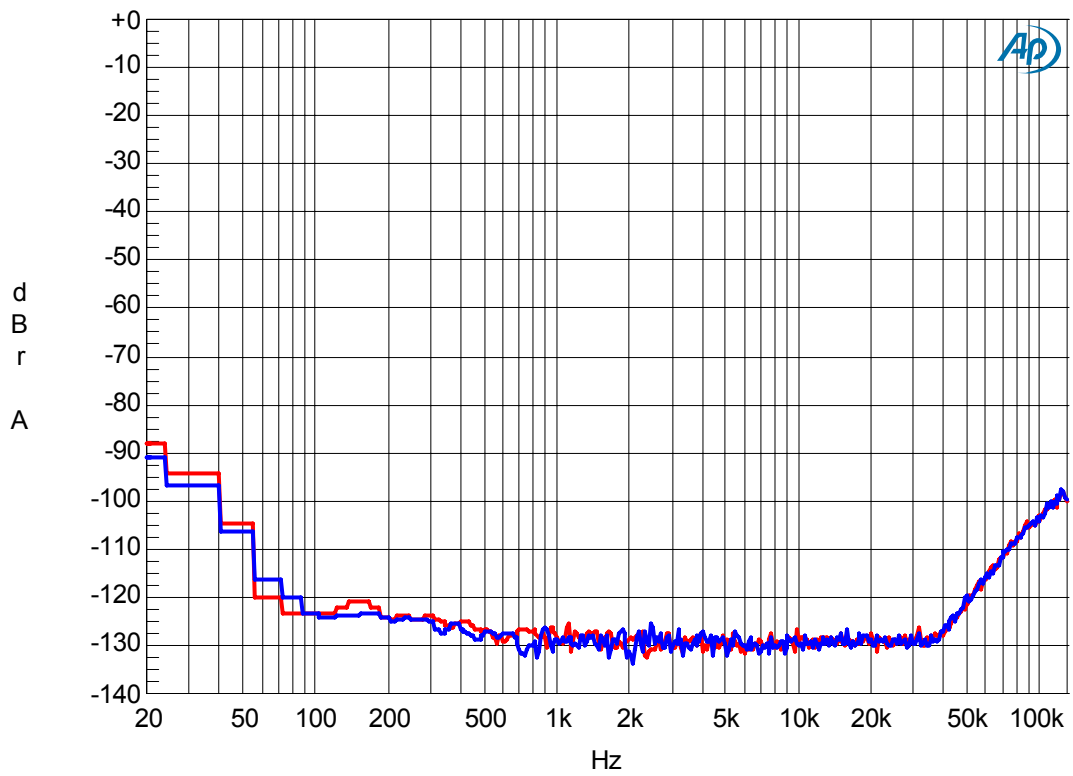


Figure 17. FFT(out-of-band noise)

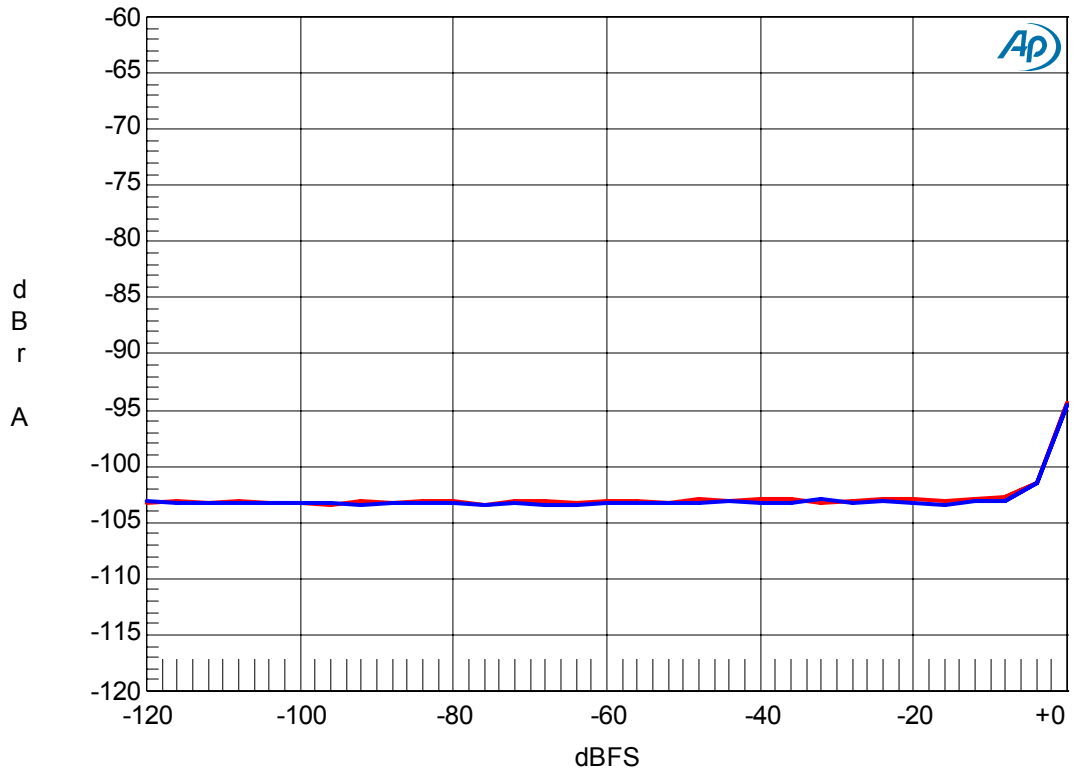


Figure 18. THD+N vs Input Level (Input Frequency =1kHz)

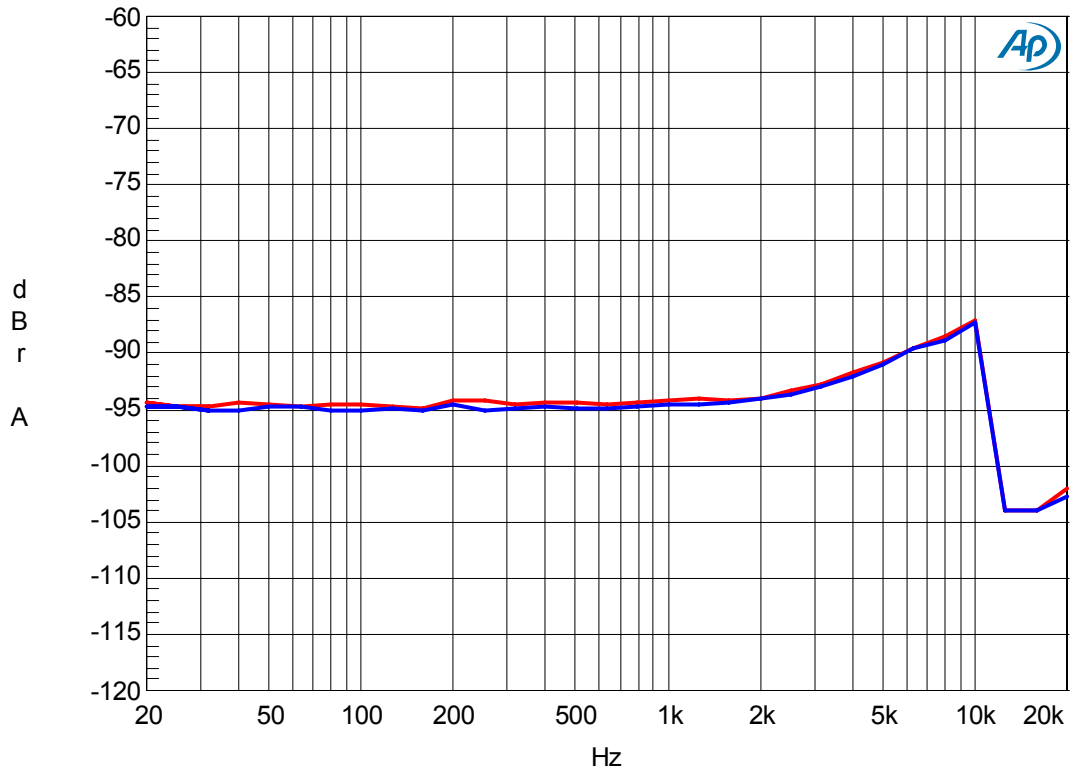


Figure 19. THD+N vs Input Frequency (Input Level=0dBFS)

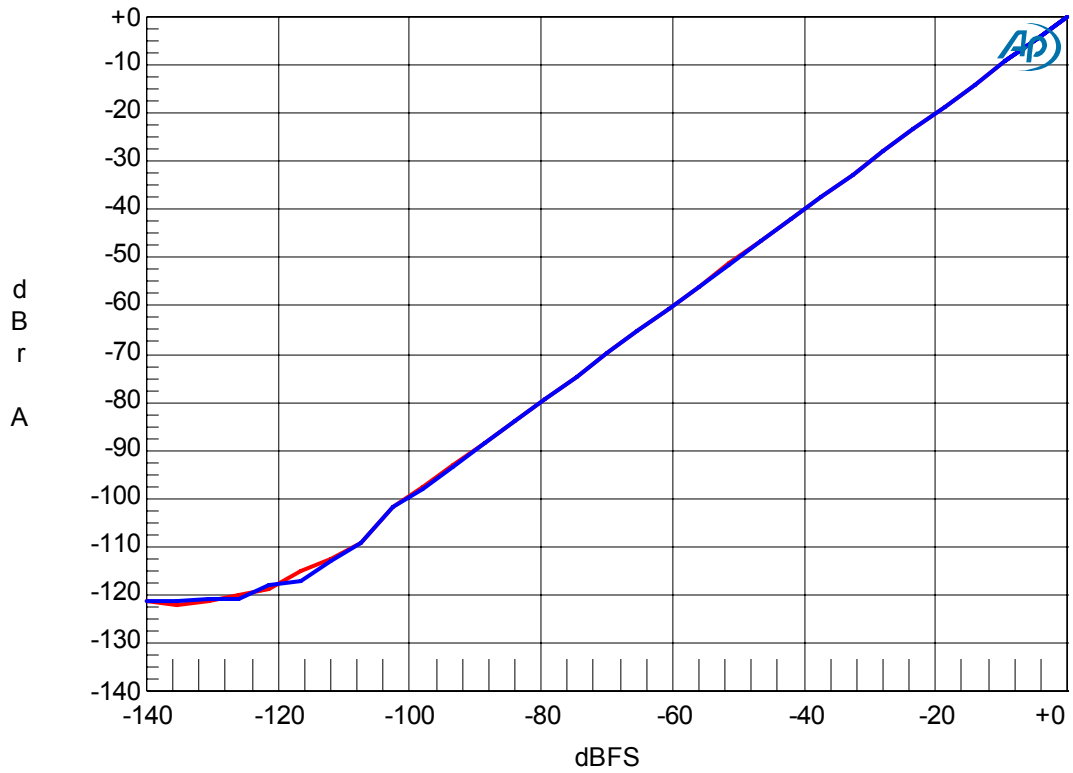


Figure 20. Linearity (Input Frequency =1kHz)

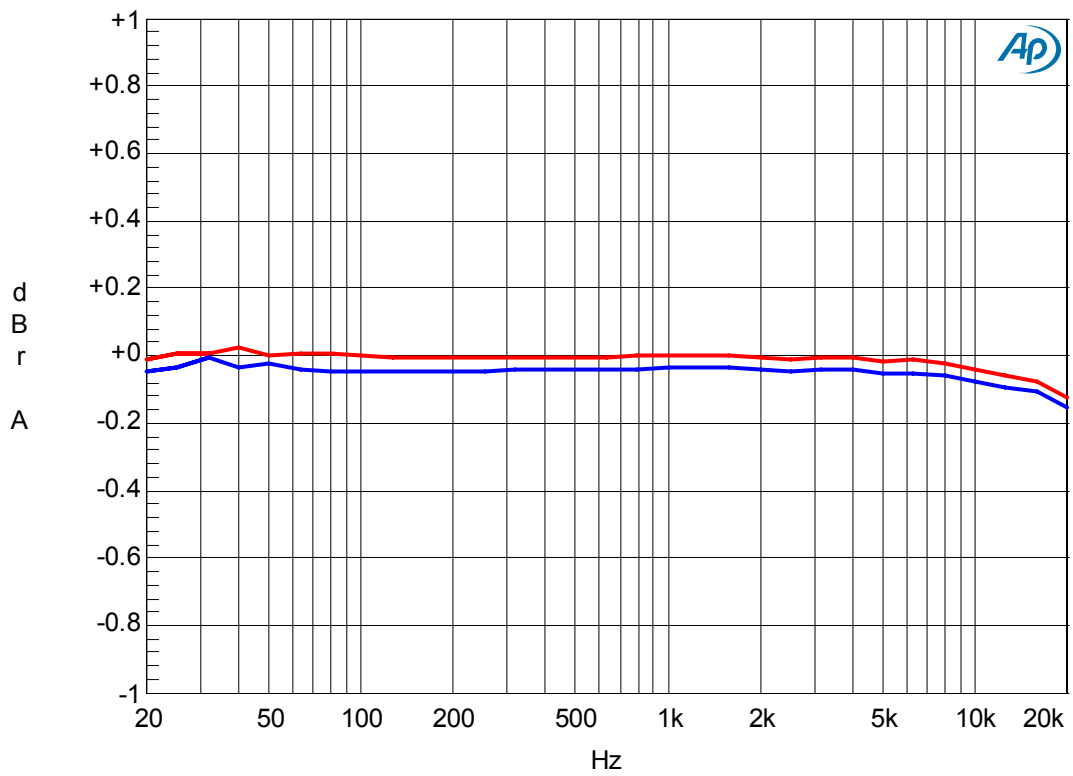


Figure 21. Frequency Response (Input Level=0dBFS, including external RC Filter)

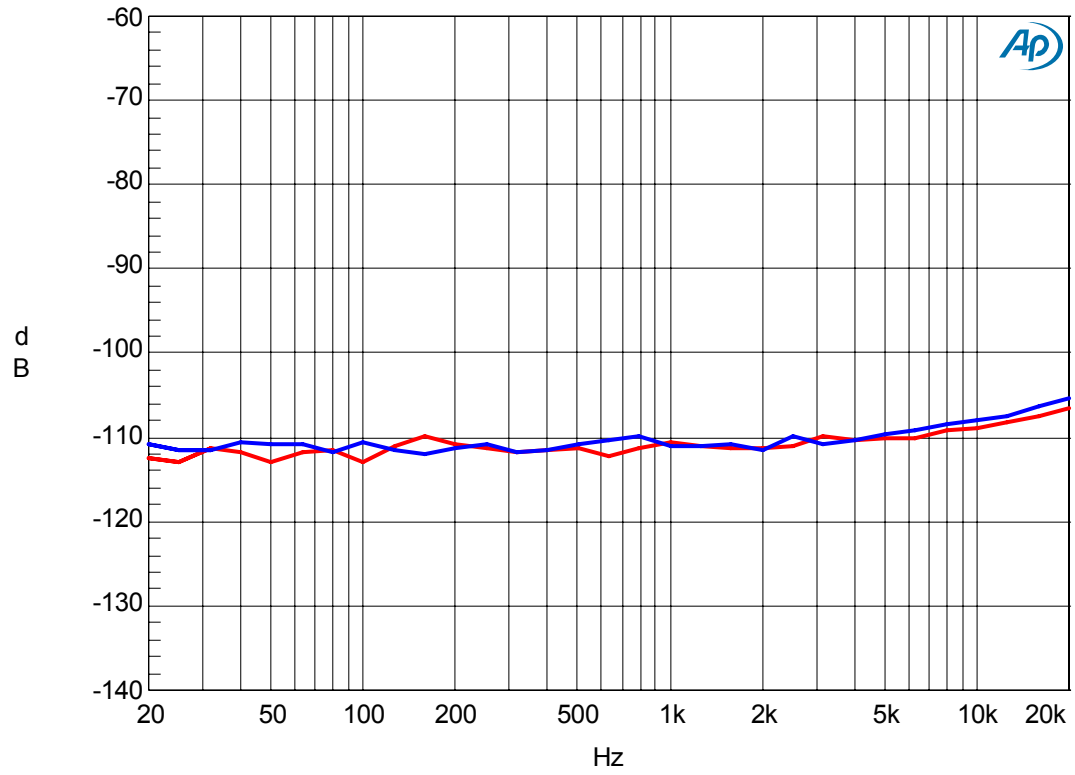


Figure 22. Cross-talk (Input Level=0dBFS)

2-2. DAC part (fs=96kHz)

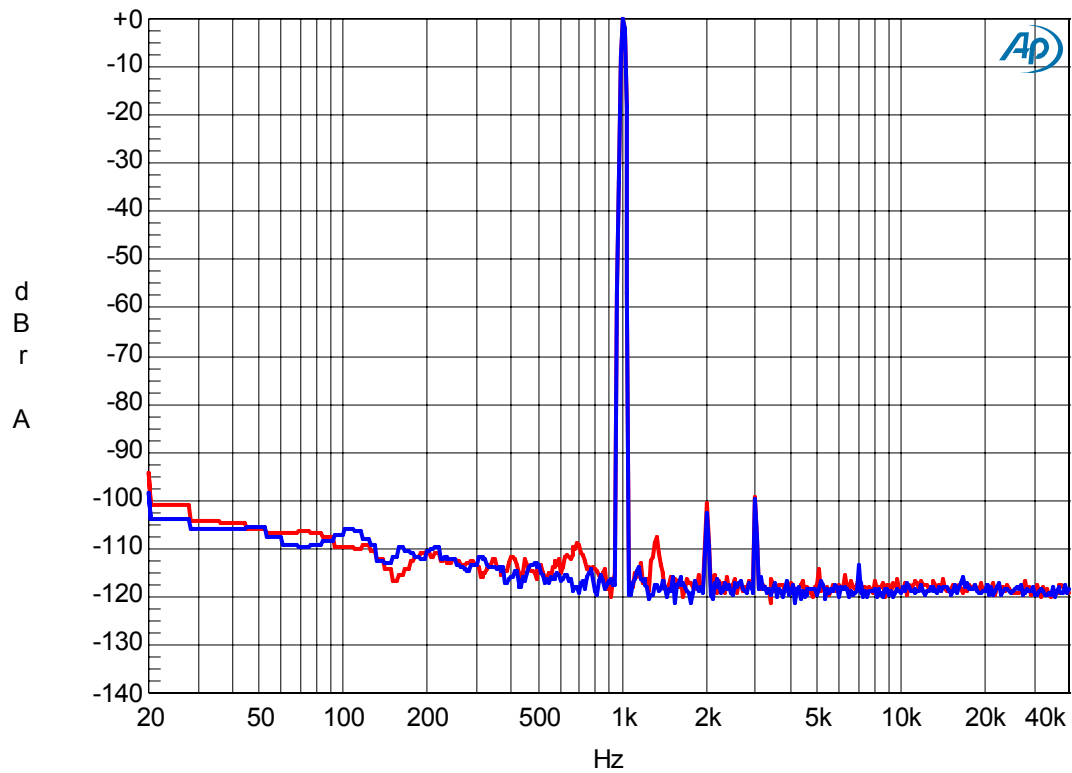


Figure 23. FFT(Input Frequency =1kHz, Input Level=0dBFS)

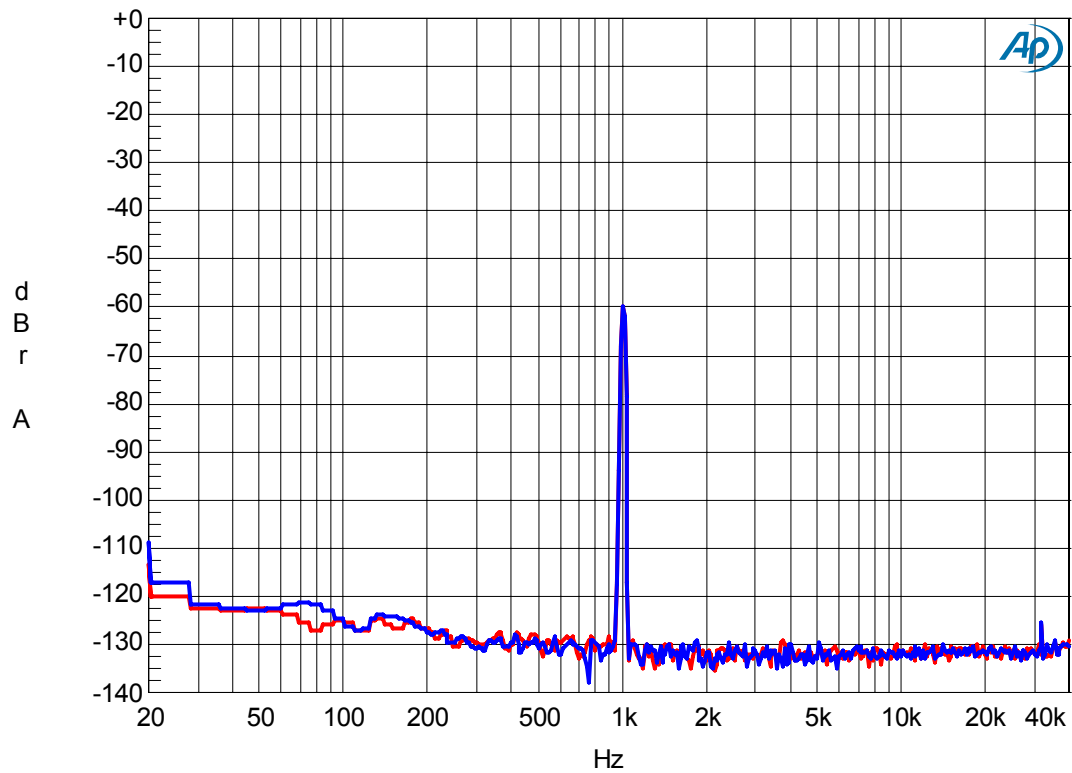


Figure 24. FFT(Input Frequency =1kHz, Input Level=-60dBFS)

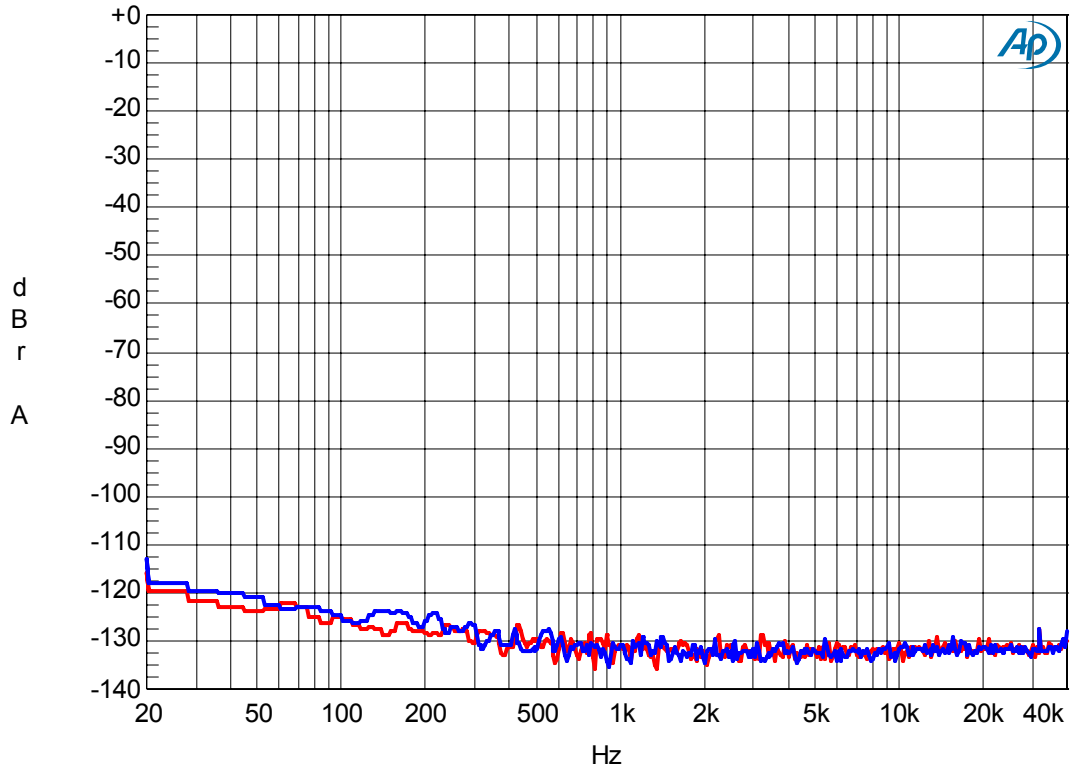


Figure 25. FFT(noise floor)

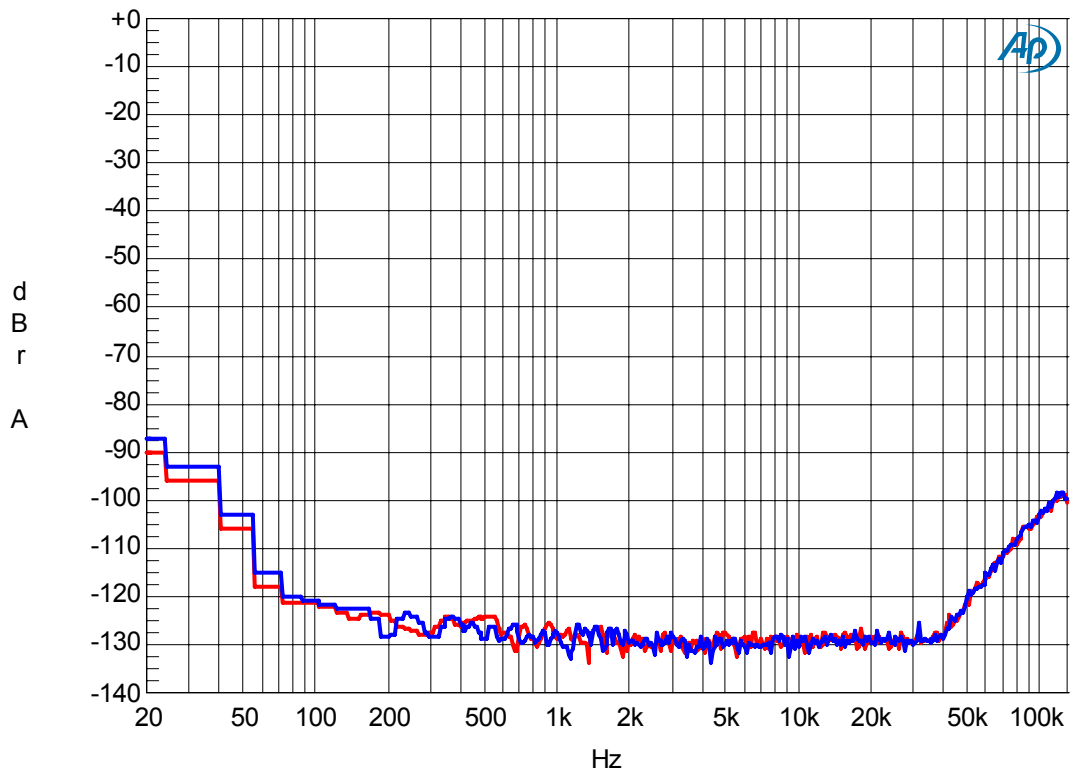


Figure 26. FFT (Out of band Noise)

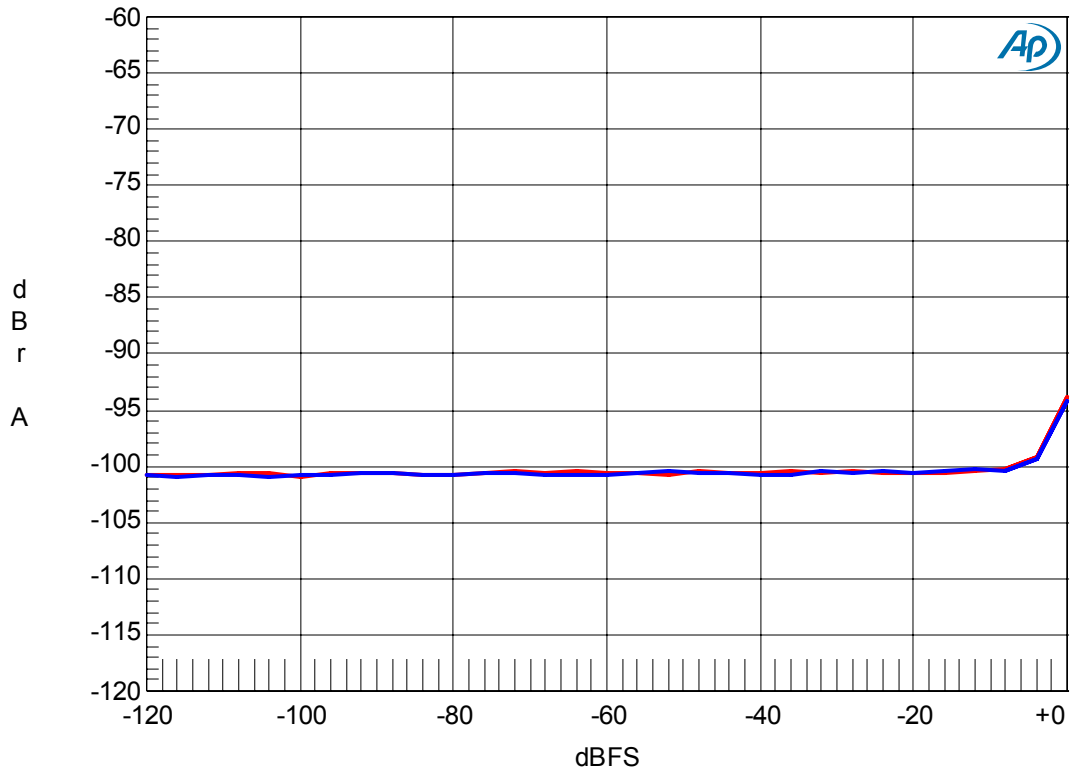


Figure 27. THD+N vs Input Level (Input Frequency =1kHz)

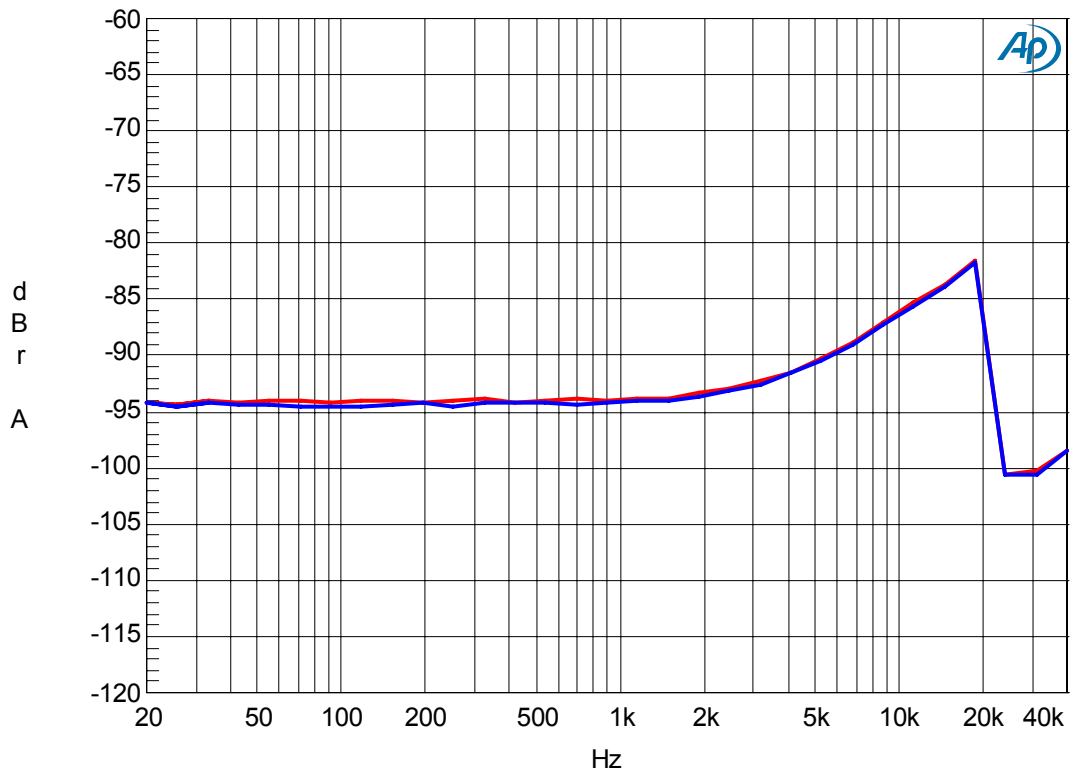


Figure 28. THD+N vs fin (Input Level=0dBFS)

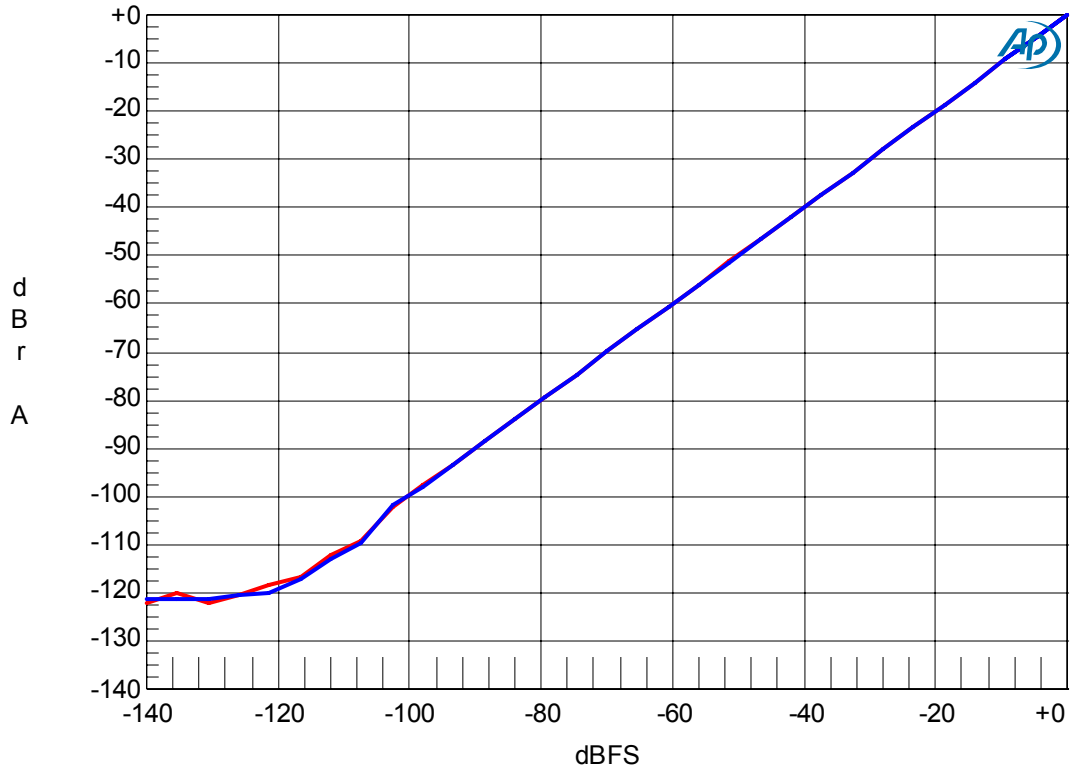


Figure 29. Linearity (Input Frequency =1kHz)

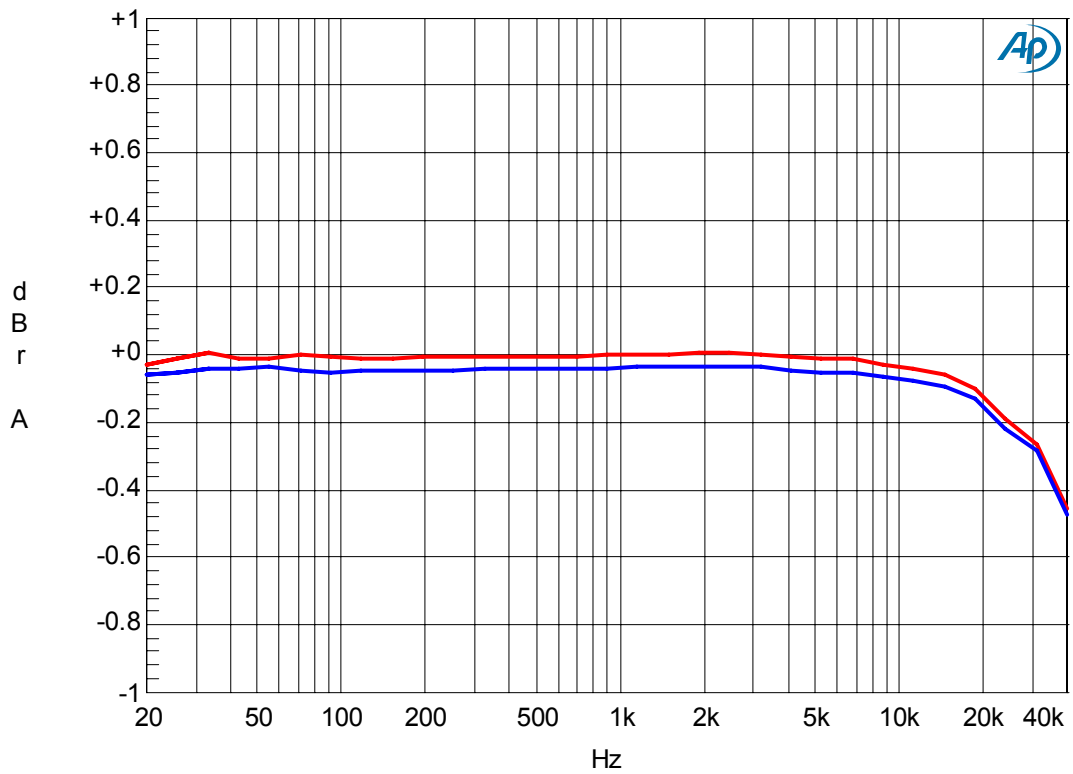


Figure 30. Frequency Response (Input Level=0dBFS, including external RC Filter)

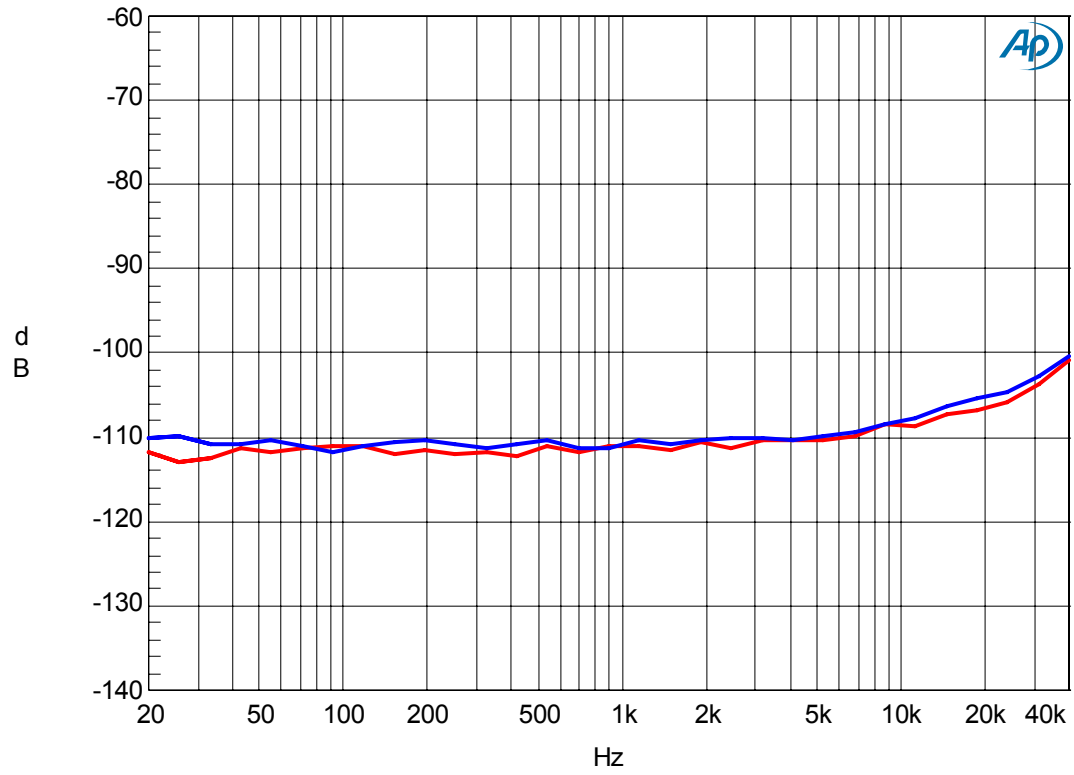


Figure 31. Cross-talk (Input Level=0dBFS)

2-3. DAC part (fs=192kHz)

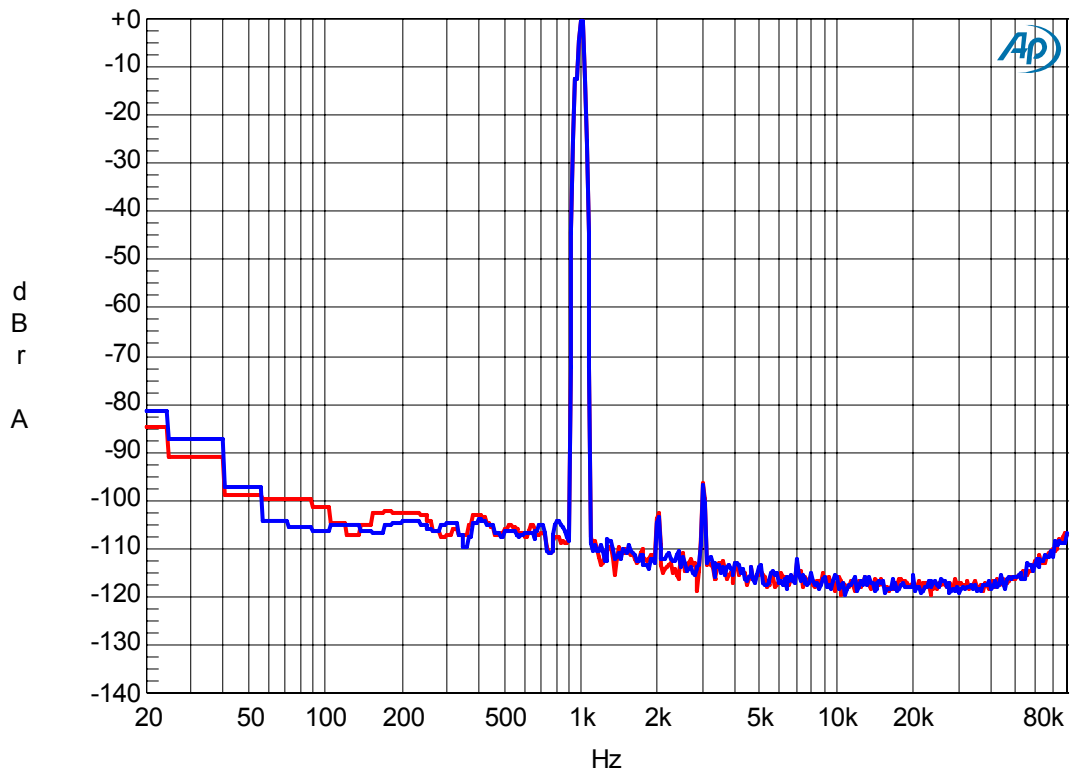


Figure 32. FFT(Input Frequency =1kHz, Input Level=0dBFS)

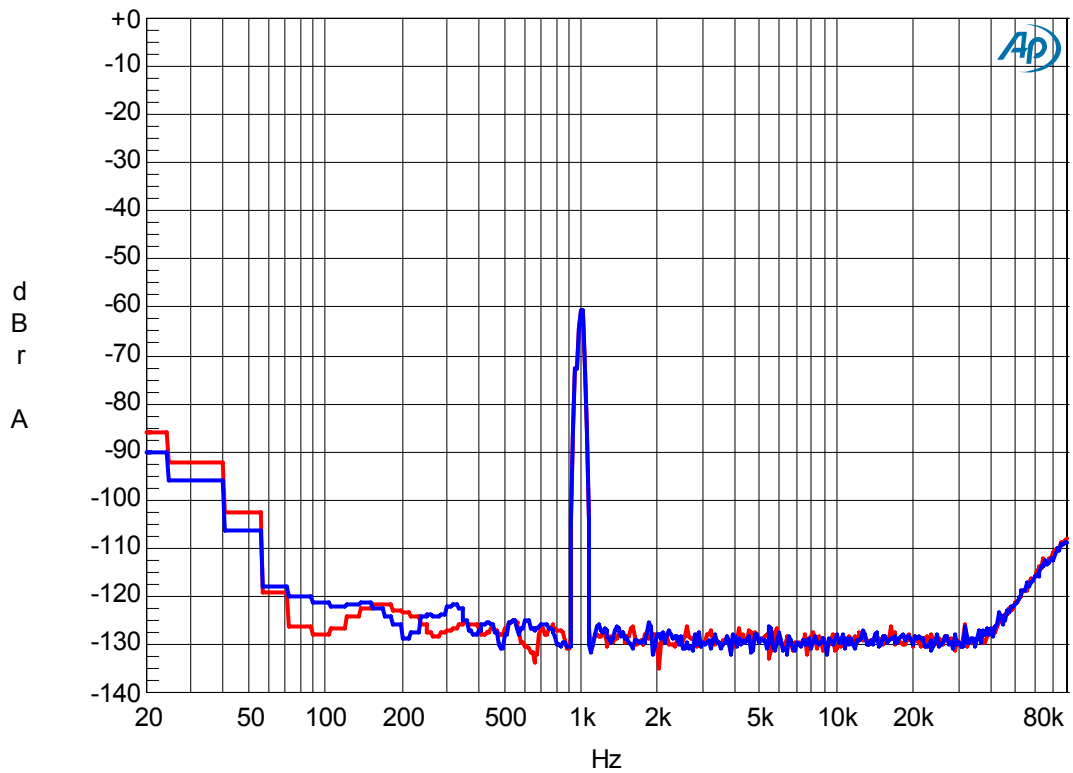


Figure 33. FFT(Input Frequency =1kHz, Input Level=-60dBFS)

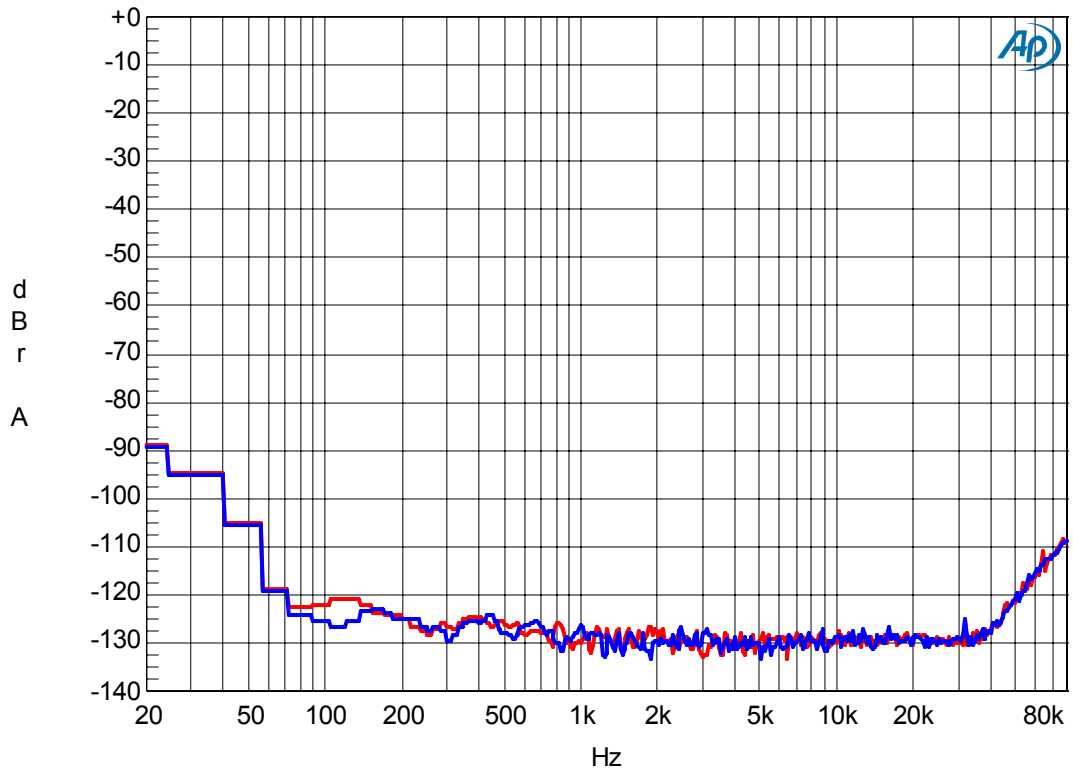


Figure 34. FFT(noise floor)

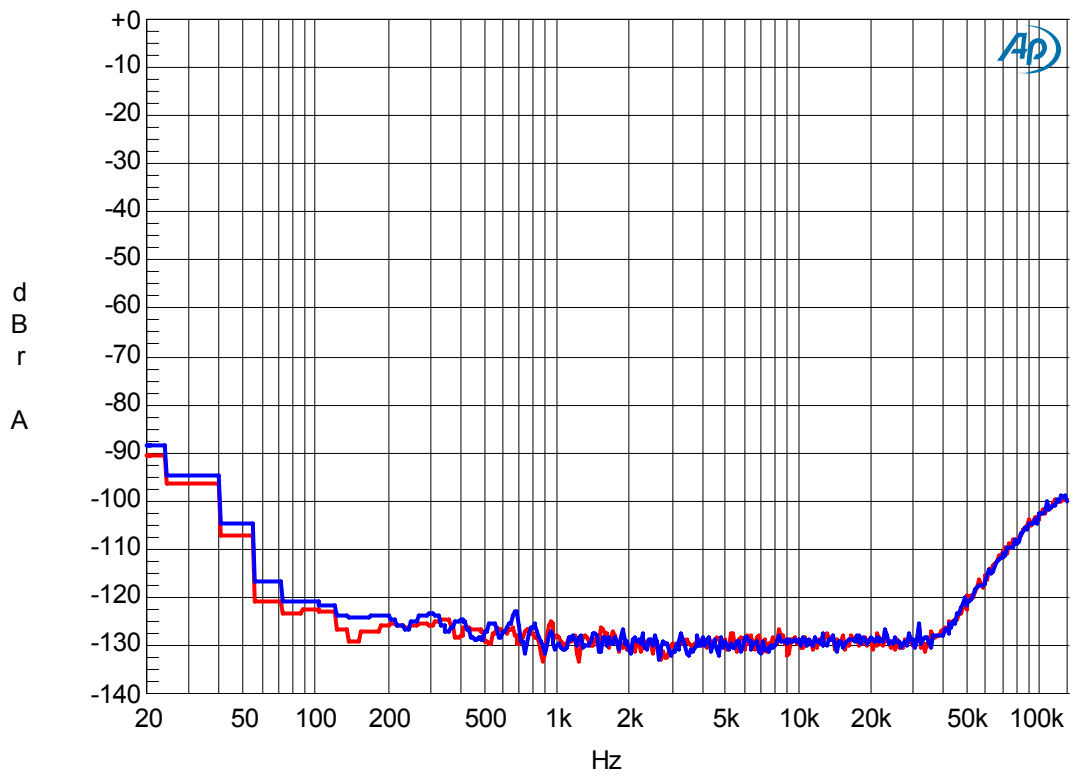


Figure 35. FFT (Out of band Noise)

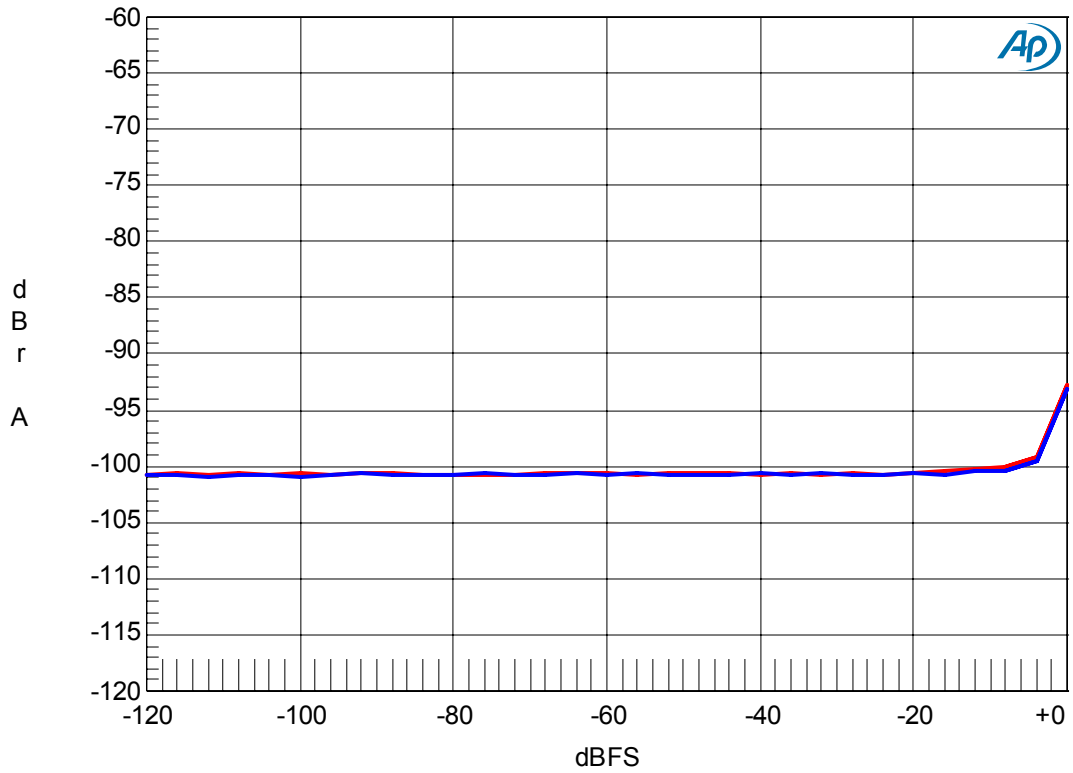


Figure 36. THD+N vs Input Level (Input Frequency =1kHz)

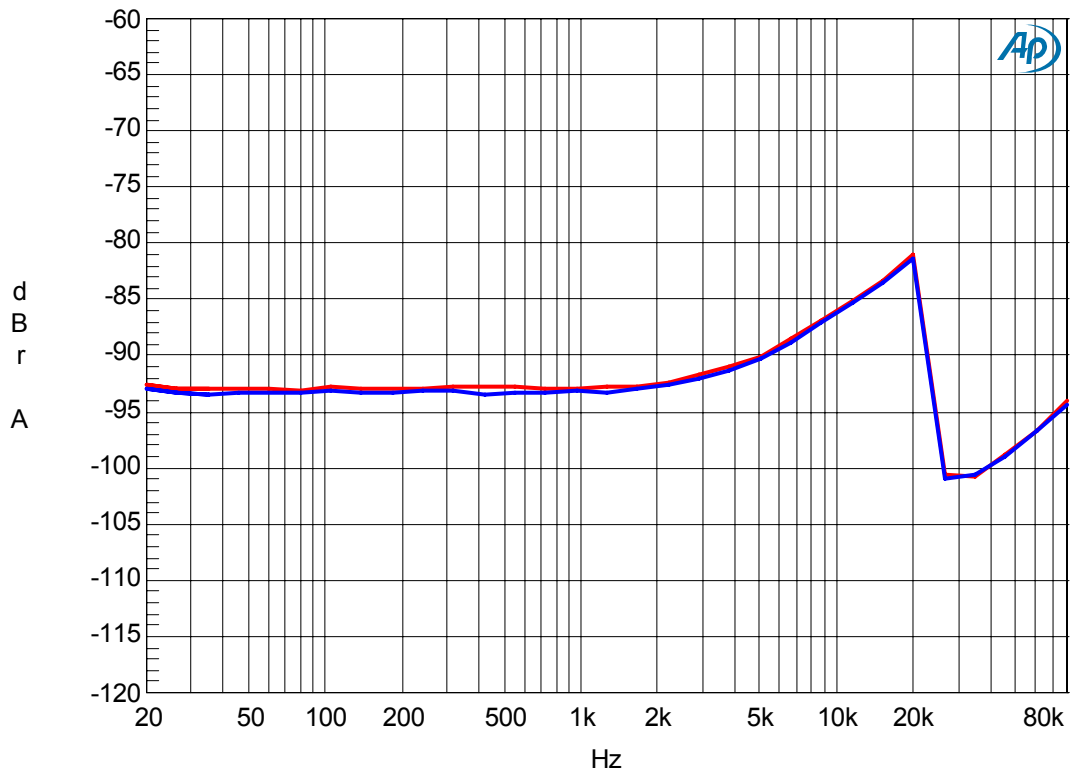


Figure 37. THD+N vs Input Frequency (Input Level=0dBFS)

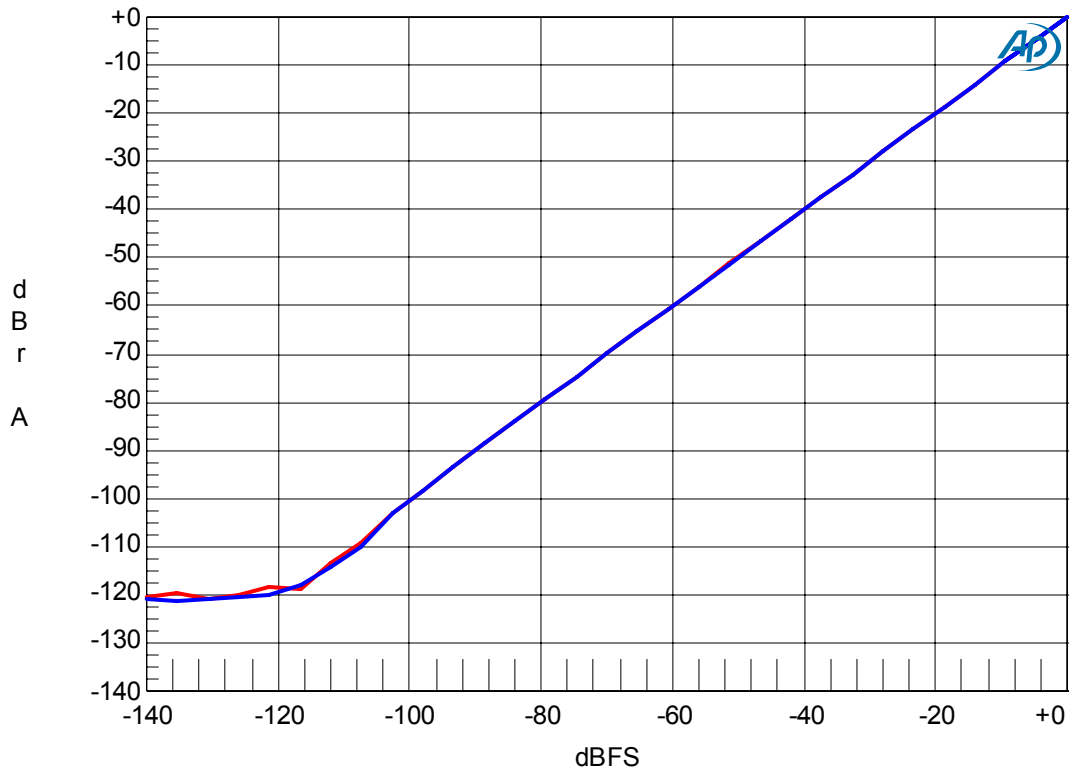


Figure 38. Linearity (Input Frequency =1kHz)

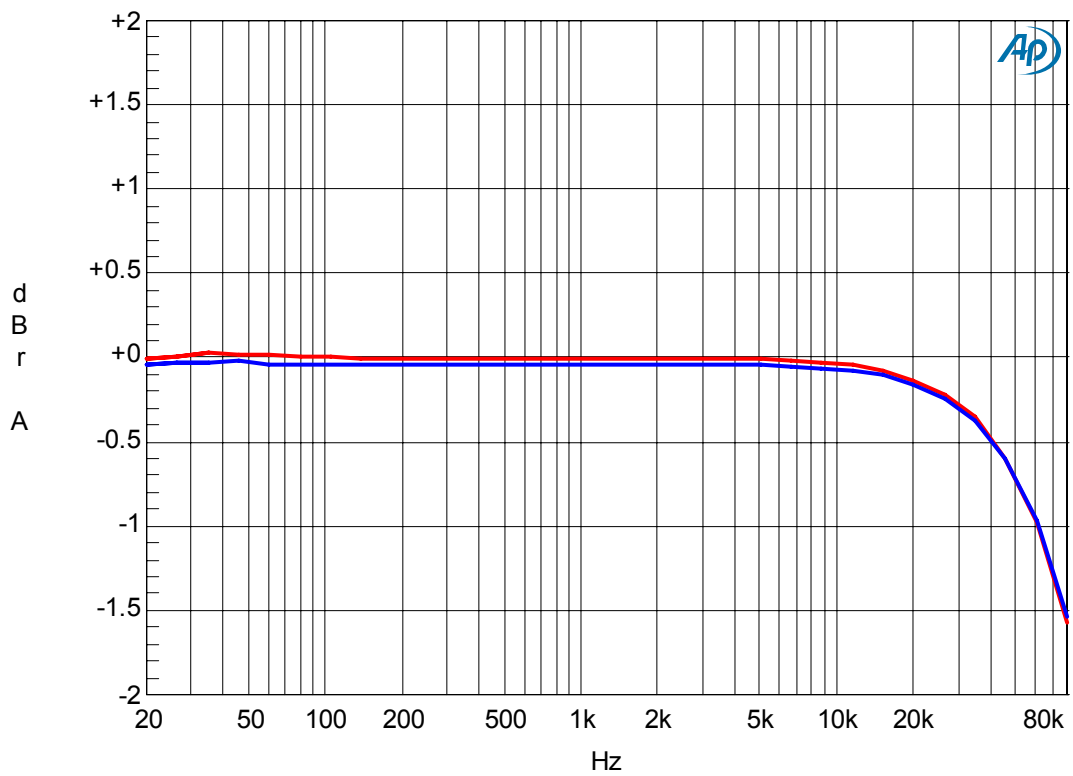


Figure 39. Frequency Response (Input Level=0dBFS, including external RC Filter)

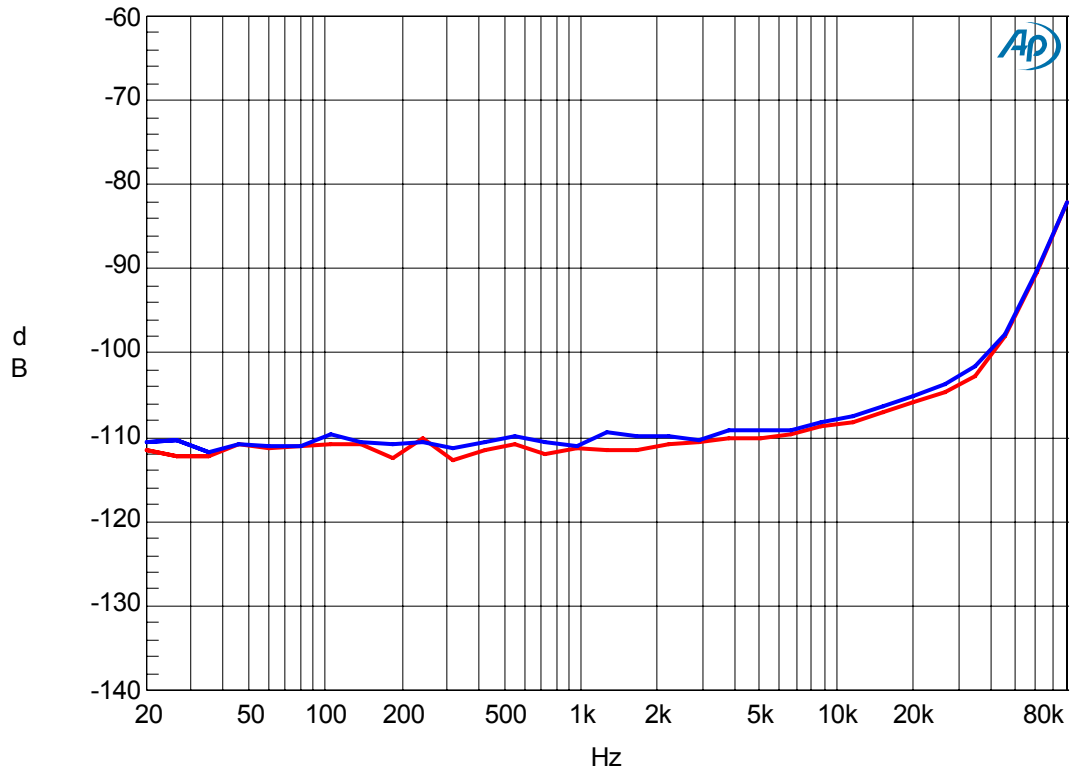


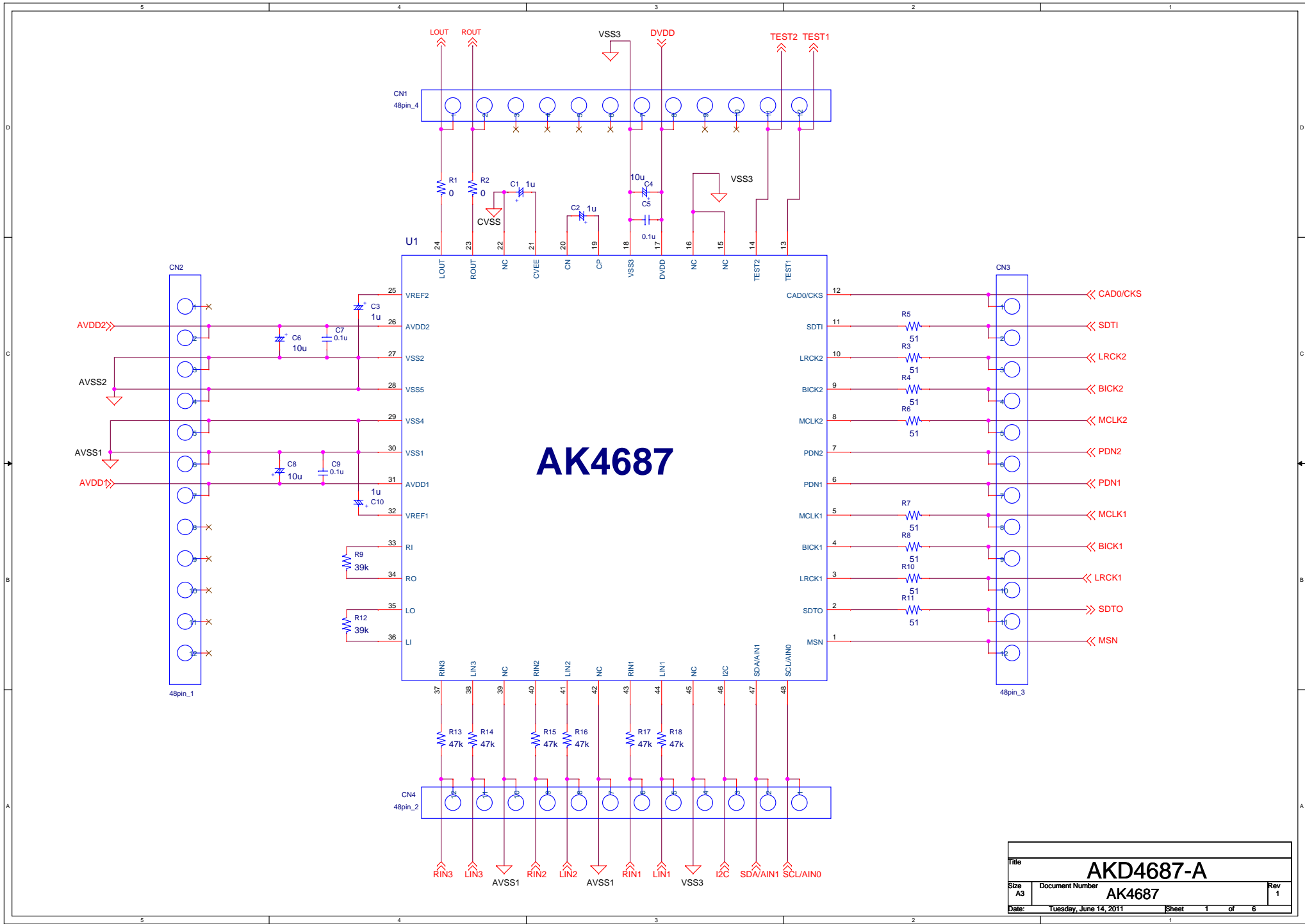
Figure 40. Cross-talk (Input Level=0dBFS)

REVISION HISTORY

Date (yy/mm/dd)	Manual Revision	Board Revision	Reason	Page	Contents
2010/10/27	KM104600	0	First Edition		
2010/11/09	KM104601		Device changed		AK4687 Rev.A Ceramic → Rev.A Plastic
2011/01/05	KM104602	1	Device Rev. changed Control Soft base changed: 1.11 → 1.13	10,14	AK4687 Rev.A Plastic → Rev.B Ceramic Control soft's plots were updated; The sentence "or via an AKDUSBIF-B interface board" was added.
2011/06/17	KM104603	2	Change		Device revision was changed. → AK4687Rev. F
			Change	43	Circuit diagram was changed. R9,R12 33kΩ → 39Ω
			Addition	21-41	Measurement Results was added.

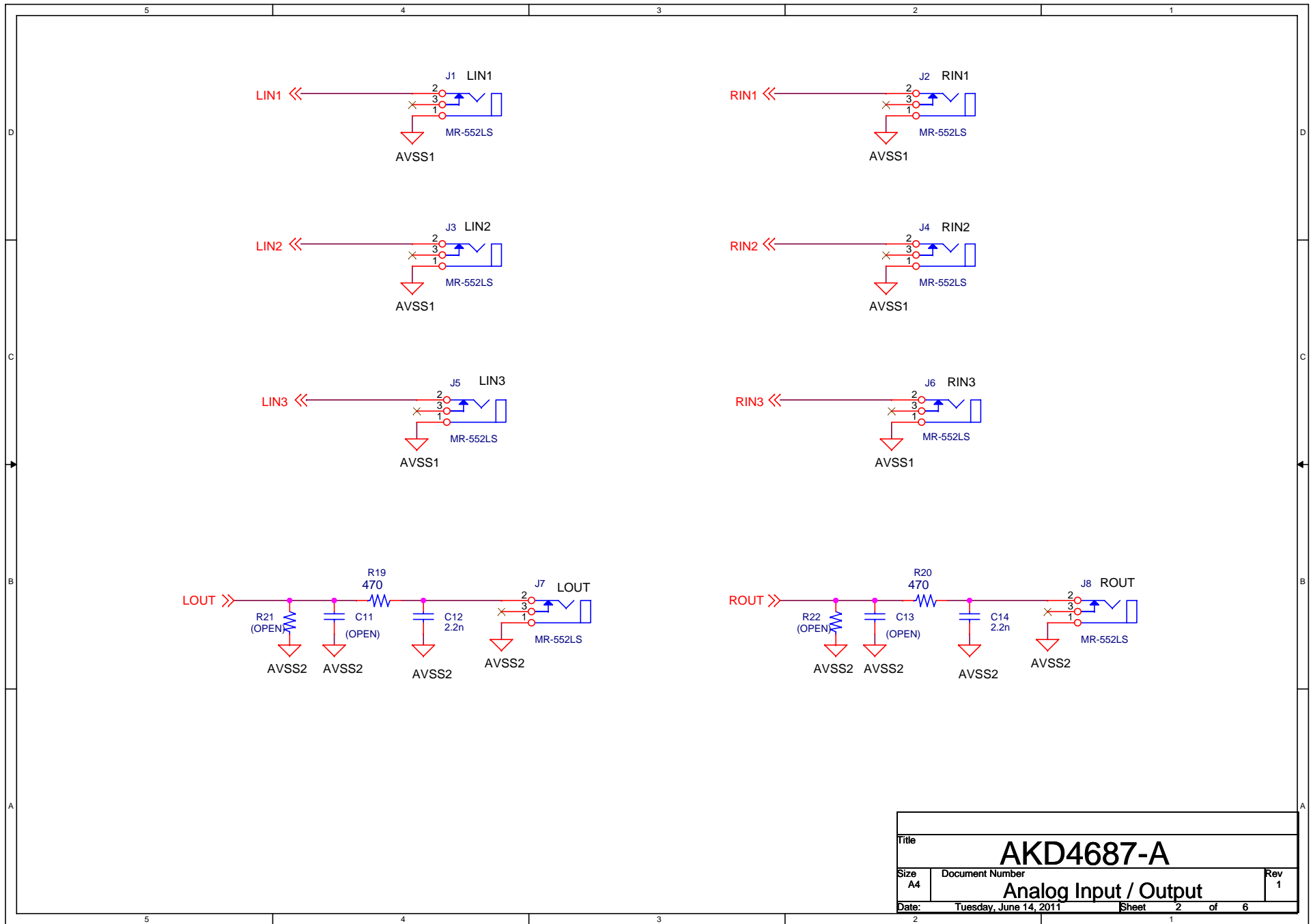
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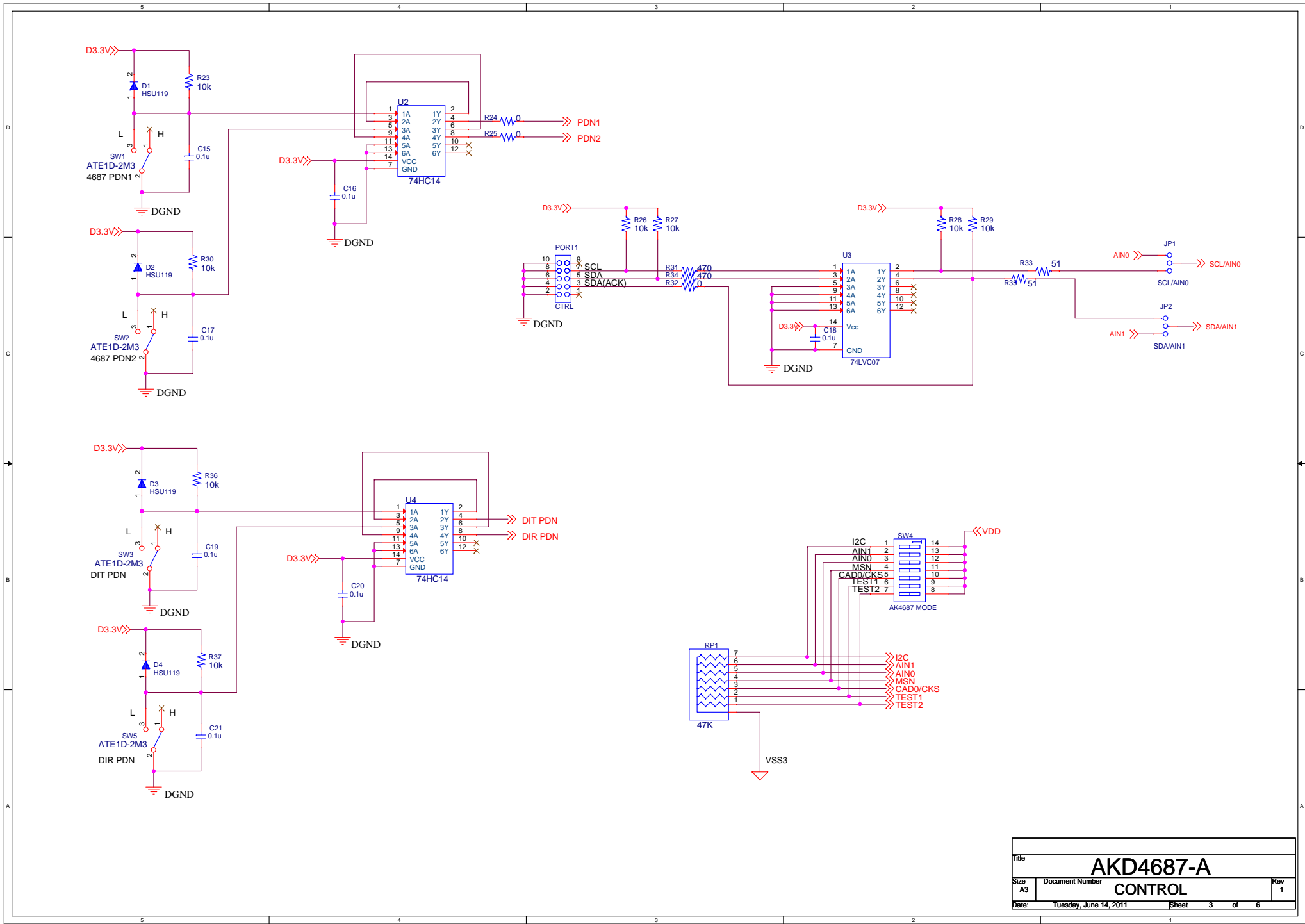


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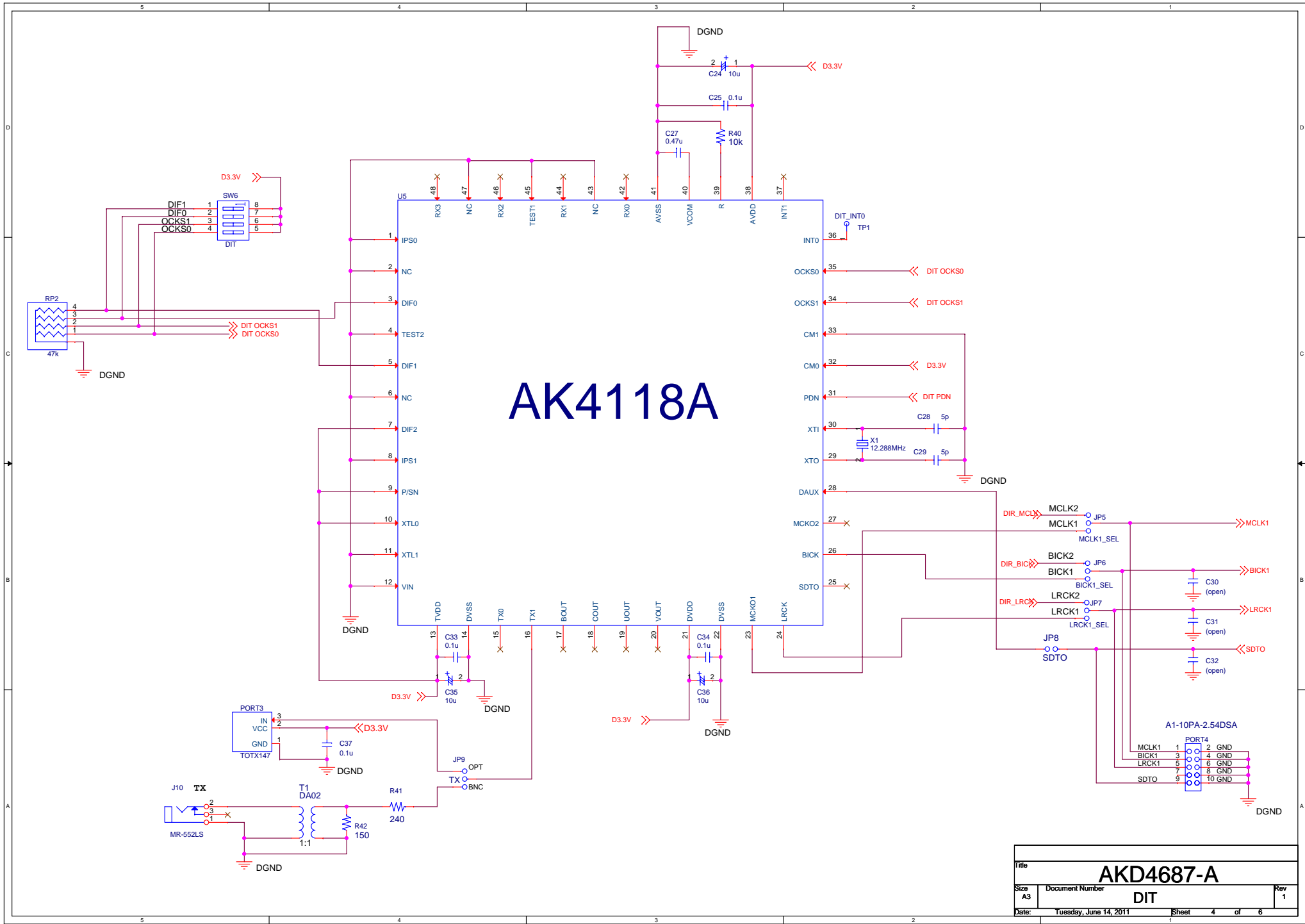
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Size	Document Number				Rev
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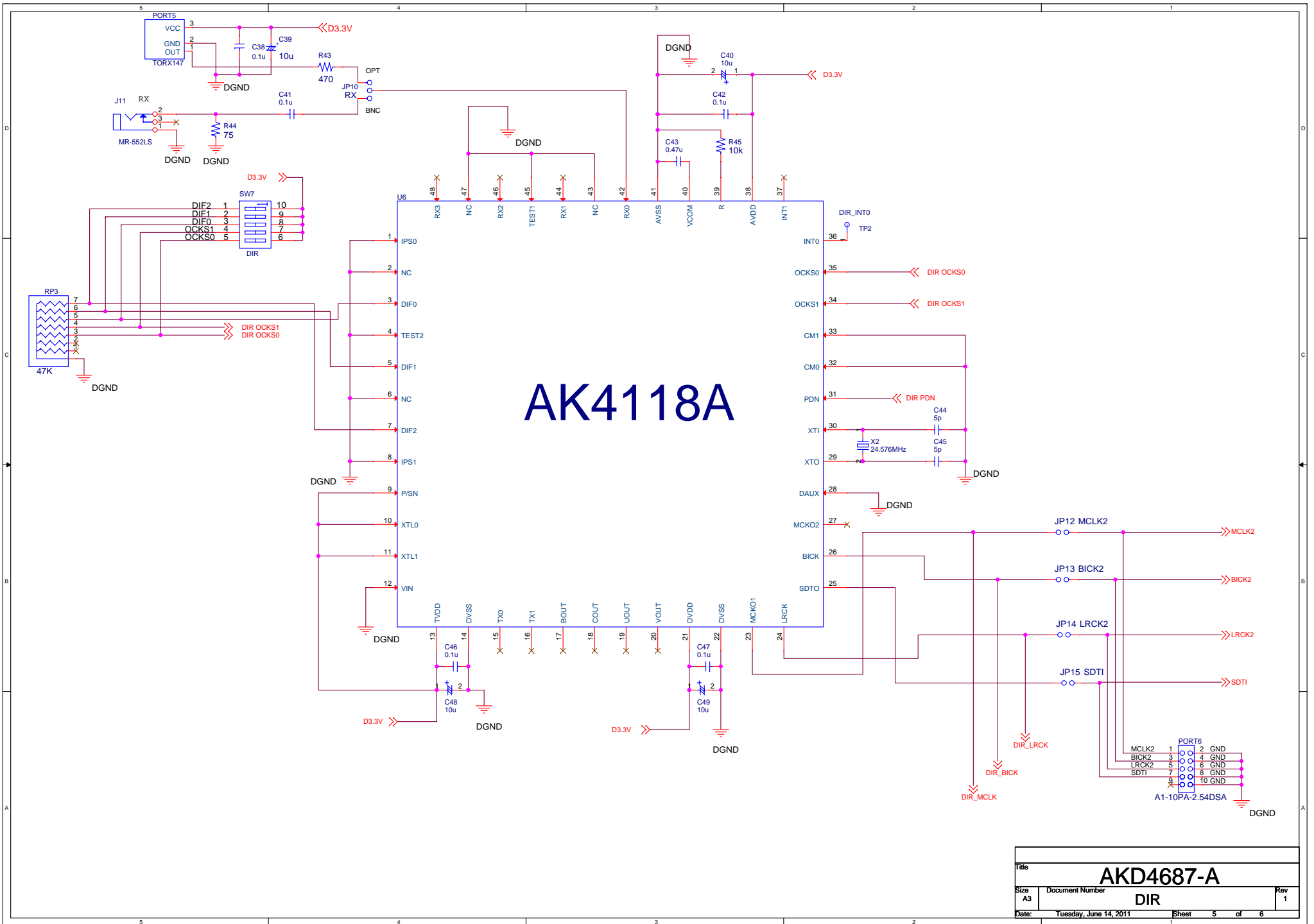


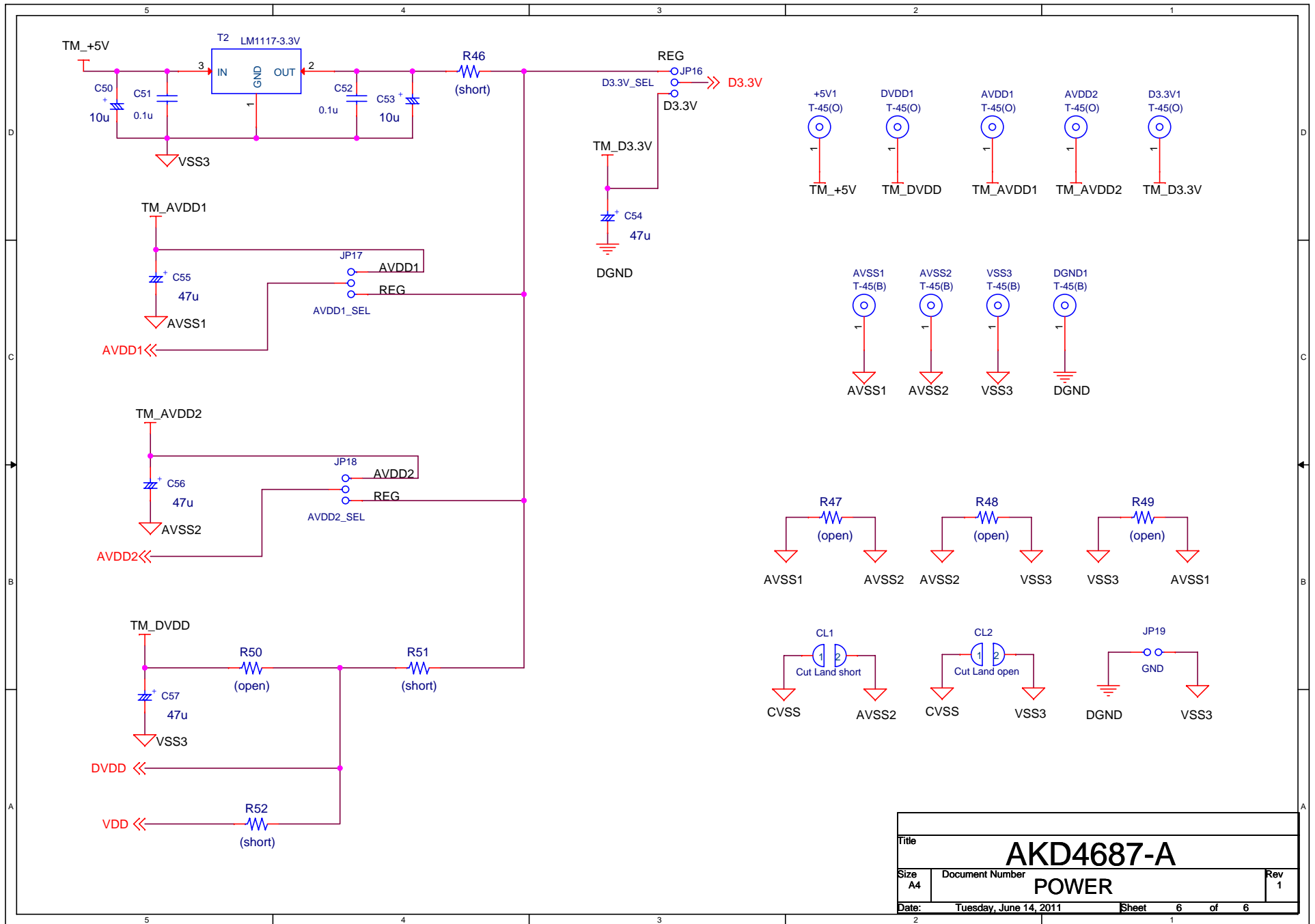
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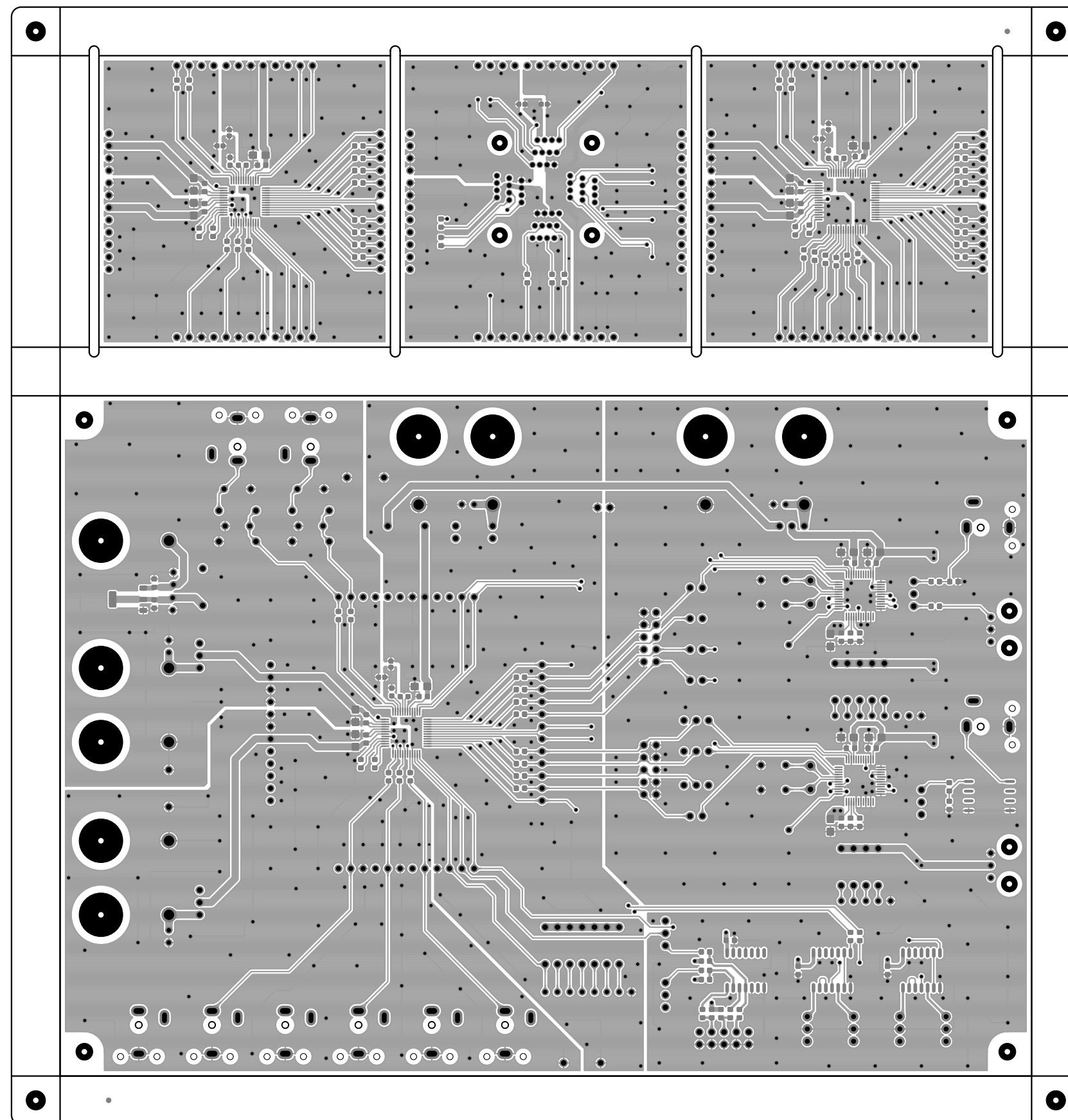




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部品面パターン図 (部品面透視図)



AKD4687-A Rev.0

半田面パターン図 (部品面透視図)

