AKD5394A
AK5394A Evaluation Board Rev.B

GENERAL DESCRIPTION

AKD5394A is an evaluation board for AK5394A, the 24bit A/D converter for professional audio. It has analog input buffer circuits, clock generator circuits, and digital audio interfaces, therefore it can achieve the interface with digital audio systems via optical connector or BNC connector. And it can achieve the direct interface with AKM's D/A converter evaluation boards via 10-line flat cable.

■ **Ordering guide**

AKD5394A --- AK5394A Evaluation Board

FUNCTION

- **Analog input buffer circuits**
- **Clock generator circuits**
- **2 type digital audio interfaces**
  - **Optical output or COAX output by DIT(AK4103A)**
  - **Direct interface with AKM's D/A converter evaluation boards via 10-line flat cable**
- **BNC connector for external clock input**

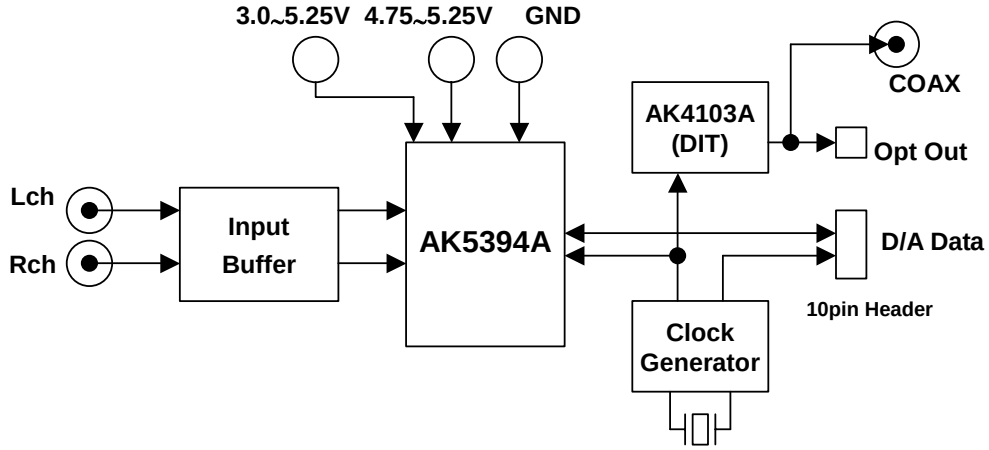

Figure 1. AKD5394A Block Diagram

* Circuit diagram and PCB layout are attached at the end of this manual.

EVALUATION BOARD MANUAL

■ Operation sequence

1) Set up the power supply lines.

[+15V]	(Green)	= +15V	
[-15V]	(Blue)	= -15V	
[5394_VA]	(Red)	= 4.75~5.25V	: VA of AK5394A
[5394_VD]	(Orange)	= 3.0~5.25V	: VD of AK5394A
[4103_VD]	(Red)	= 4.75~5.25V	: VDD of AK4103A
[AGND]	(Black)	= 0V	: Analog Ground(Include AGND and DGND of AK5394A)
[DGND]	(Black)	= 0V	: Digital Ground(Logic part)

When "5394_VD" is operated on 3.0~4.75V, JP15(IF/5V) should be connected to "5394_VD".
Each supply line should be distributed from the power supply unit.

2) Set-up the evaluation modes, jumper pins and DIP switches. (See the followings.)

3) Power on.
The AK5394A and AK4103A should be reset once by bringing SW1 (PDN) to "L" after power-on.
After that, release the reset by bringing SW1 (PDN) to "H".
Keep SW1(PDN) "H" during normal operation.

■ Evaluation mode

1) Use DIT (Optical connector or BNC connector) <default>
2) Use AKM's D/A evaluation board
3) Receive interface signal : MCLK, SCLK(BICK), LRCK from external source

1) Use DIT (Optical connector or BNC connector) <default>

PORT2(TOTX176) or J5(TX) are used. It is able to send A/D converted data through optical connector or BNC connector. And it is able to connect to AKM's D/A evaluation board and digital amp. When MCLK is received from external source through BNC connector (J6), JP2(CLK) should be connected to "BNC" side, and JP16(XTE) should be short. The setting of JP7, JP9, JP11, JP12 and JP13 should be adjusted to the AK5394A's conditions(clock ratio, data format, etc).(Refer to setting of jumper pin.)

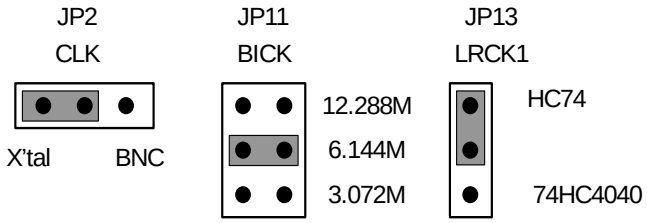

Figure2. Setting of jumper pin (Use DIT) <default>

2) Use AKM's D/A evaluation board

It is able to evaluate AKM's D/A evaluation board connecting to PORT3(EXT) via 10pin flat cable. When MCLK, SCLK(BICK) and LRCK are sent to a D/A board, setting of jumper pin is the same as "1)". When MCLK, SCLK(BICK) and LRCK are received from a D/A board, setting of jumper pin is the same as "3)".

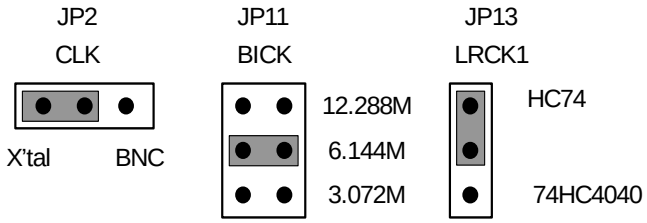

Figure3. Setting of jumper pin (Use AKM's D/A evaluation board)

3) Receive interface signal : MCLK, SCLK(BICK), LRCK from external source

PORT3(EXT) is used. JP11 and 12 should be open. The setting of JP7 and JP9 should be adjusted to the AK5394A's conditions(clock ratio, data format, etc).(Refer to setting of jumper pin.)

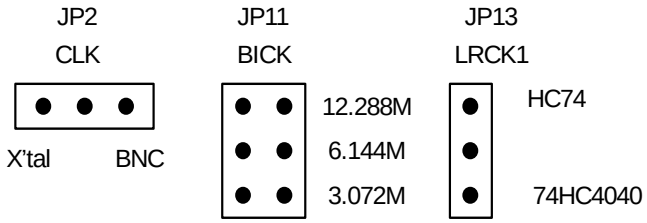

Figure4. Setting of jumper pin (Receive interface signal)

■ Setting of DIP switch

1. Polarity of DIP switch

Refer to table below, before setting of DIP switch.
(Normally, "ON" is "H", "OFF" is "L".)

Polarity of DIP switch : SW2(AK5394A), SW3(AK4103A)

	DFS1	DFS0	HPFE	SMODE2	SMODE 1	ZCAL
ON	H	H	H	H	H	H
OFF	L	L	L	L	L	L

Table1. Polarity of DIP switch: SW2

	V1	FS0	FS1	FS2	FS3	CKS0	CKS1	DIF
ON	H	H	H	H	H	H	H	H
OFF	L	L	L	L	L	L	L	L

Table2. Polarity of DIP switch: SW3

2. Setting of DIP switch : SW2(AK5394A), SW3(AK4103A)

(1) Setting of DIP switch : SW2(AK5394A)

Sampling Speed		Normal	Double	Quad
	DFS1 (SW2-1)	OFF	OFF	ON
	DFS0 (SW2-2)	OFF	ON	OFF
LRCK (fs)		~54kHz	~108kHz	~216kHz
SCLK		~128fs	~64fs	~64fs
MCLK		256fs	128fs	64fs

(default)

Table3. Setting of DFS1, DFS0
(In the case of Quad Speed, MCLK of AK4103A is 128fs.)

SMODE2 (SW2-4)	SMODE1 (SW2-5)	Audio Format	
OFF	OFF	Slave Mode	(default)
OFF	ON	Master Mode	
ON	OFF	I^2S Slave Mode	
ON	ON	I^2S Master Mode	

Table4. Setting of SMODE2, SMODE1

[SW2-6]: Calibration pin
"OFF": VCOML, VCOMR (default)
"ON": Analog input pin (AINL±, AINR±)

[SW2-3]: HPFE
"ON": Enable
"OFF": Disable (default)

(2) Setting of DIP switch : SW3(AK4103A)

CKS1 (SW3-6)	CKS0 (SW3-7)	MCLK	LRCK	
OFF	ON	128fs	28~216kHz	
OFF	OFF	256fs	28~108kHz	(default)

Table5.Setting of system clock

DIF0 (SW3-8)	Audio Format	BICK	
OFF	24bit, Left Justified	48~128fs	(default)
ON	24bit, I2S	50~128fs	

Table6. Audio format of AK4103A

[SW3-2,3,4,5] : Set sampling frequency of channel status. (default is all “OFF”.)

[SW3-1] : Set validity of channel status. (default is “OFF”.)

3. Setting of clock

Setting of clock of AK5394A and AK4103A

LRCK(fs)	MCLK	BICK	JP9	JP11	JP12	JP13	
48kHz	256fs	128fs 64fs	12.288M	6.144M 3.072M	48k	HC74	(default)
96kHz	128fs	64fs	12.288M	6.144M	96k	HC74	
192kHz	64fs	64fs	12.288M	12.288M	192k	HC74	

Table7. System clock example

■ Setting of jumper pin

[JP1] (5394_VA) : select the source of power supply for VA pin of AK5394A.
Short : supply from the regulator(T1) on board (default)
(In this case, the jack of "5394_VA" should be open.)
Open : supply from the jack of "5394_VA"

[JP2] (CLK) : select the source of MCLK for AK5394A and AK4103A.
(Excepting the case of receiving from external source, SCLK(BICK) and LRCK for AK5394A and AK4103A are generated by dividing MCLK which is selected on JP2.)
X'tal : supply from X'tal oscillator(X1) on board. (default)
(Use 24.5760MHz as frequency of X'tal Oscillator.)
BNC : supply from external source through BNC connector(J6)

[JP3, JP4, JP5, JP6] (BNC) : select the connector for analog input.
Short : use BNC connectors(J2, J4).
Open : use XLR(Cannon) connectors(J1, J3). (default)

[JP7] (4103_MCLK) : select the frequency of MCLK for AK4103A. (Note1)
CLK : x 1
HC4040 : x 1/2 (default)

[JP9] (5394_MCLK) : select the frequency of MCLK for AK5394A. (Note1)
24.576M (Note2) : x 1
12.288M (Note2) : x 1/2 (default)

[JP11] (BICK) : select the frequency of SCLK(BICK) for AK5394A and AK4103A. (Note1)
12.288M (Note2) : x 1/2
6.144M (Note2) : x 1/4 (default)
3.072M (Note2) : x 1/8

[JP12] (LRCK) : select the frequency of LRCK for AK5394A and AK4103A. (Note1)
192k (Note2) : x 1/128
96k (Note2) : x 1/256
48k (Note2) : x 1/512 (default)

[JP13] (LRCK1): select the adjust of the phase of LRCK and SCLK(BICK) for AK5394A and AK4103A.
74HC4040 : supply LRCK without the adjust of the phase of LRCK and SCLK(BICK).
74HC74 : supply LRCK after the adjust of the phase of LRCK and SCLK(BICK) by 74HC74. (default)

[JP15] (IF/5V) : select the source of power supply for digital logic part.
5394_VD :supply from the jack of "5394_VD" (default)
(Use this jack when VD of AK5394A is operated in 3.3V.)
4103_VD :supply from the jack of "4103_VD".

[JP16] (XTE) : select X'tal oscillator(X1) on board.

Short : not use X'tal oscillator(X1) on board.
Open : use X'tal oscillator(X1) on board. (default)

(Note1) Select the ratio to the frequency of (PORT3, J6 or X1).
(Note2) The value assumed that the frequency of (PORT3, J6 or X1) is 24.576MHz.

■ Function of the toggle SW

[SW1](PDN) : Reset AK5394A and AK4103A, bringing it to "L" once, after power-on.
And then, release the reset, bringing it to "H".
Keep it "H" during normal operation.
(Upper side is "H", and lower side is "L".)

■ Analog input buffer circuit

An analog input buffer circuit example (1st order HPF; fc=0.70Hz, 2nd order LPF; fc=320kHz, gain=-14.5dB) is shown in Figure 5. The analog signal is able to input through XLR or BNC connectors. (For BNC input, jumper should be short. For XLR input, jumper should be open.) The input level of this circuit is +/-12.7Vpp (AK5394A: +/-2.4Vpp Typ.). When using this circuit, analog characteristics at fs=48kHz is DR=120dB, S/(N+D)=105dB.

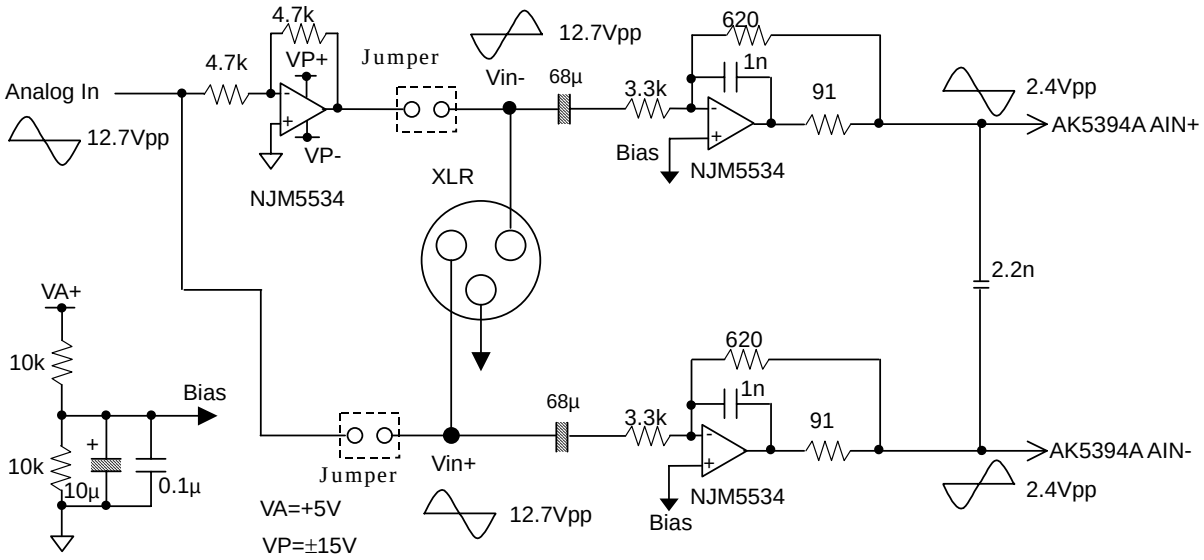

Figure 5. Analog input buffer circuit example

Fin	1Hz	10Hz
Frequency Response	-1.77dB	-0.02dB

Table 8. Frequency Response of HPF

Fin	20kHz	40kHz	80kHz	6.144MHz
Frequency Response	0.00dB	0.00dB	0.00dB	-51.36dB

Table 9. Frequency Response of LPF

■ When capacitors more than 10μF are connected between VREF pin and GND

The distortion at low frequency can be improved by connecting large capacitors C(Figure 6) to VREF pins. (Refer to Figure 7) C is C10, C13, C56 and C58 in circuit diagram. However, when the capacitors of VREF pins are larger than 10μF, it is possibility that the offset calibration does not performed correctly if the offset calibration cycle is started right after power-up. Because the internal VREF cannot settle to the appropriate voltage when the calibration cycle is completed. In this case, the offset calibration cycle should be started again after the VREF voltage settled. (Figure 8) The relationship between the capacitance and the VREF settling time is shown in Table 10.

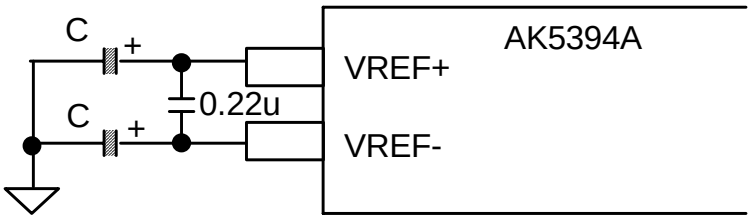

Figure 6. VREF circuit example(C is C10, C13, C56 and C58 in circuit diagram)

[Measurement Example]

Ta=25°C; VA=5.0V; VD=3.3V; AGND, BGND, DGND=0V; fs=48kHz;
24 bit Output; BW=10Hz~20kHz; DFS0= “L”, DFS1= “L”, Using Audio Precision System Two.

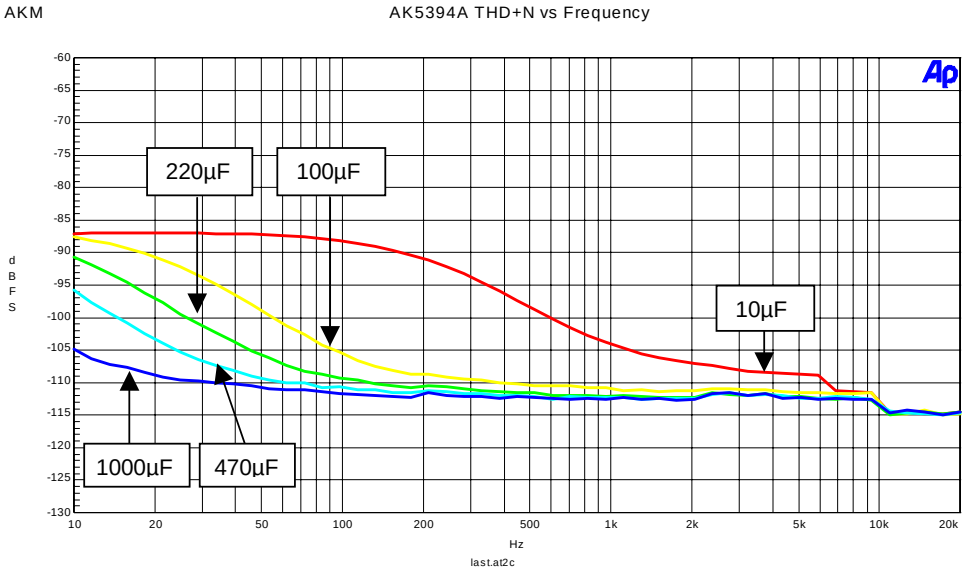

Figure 7. THD+N vs. Frequency

Capacitor C [µF]	Settling Time T[s]=0.005 x C
1000	5
470	2.4
220	1.1
100	0.5

Table 10. Capacitors connected between VREF and GND, and Settling Time

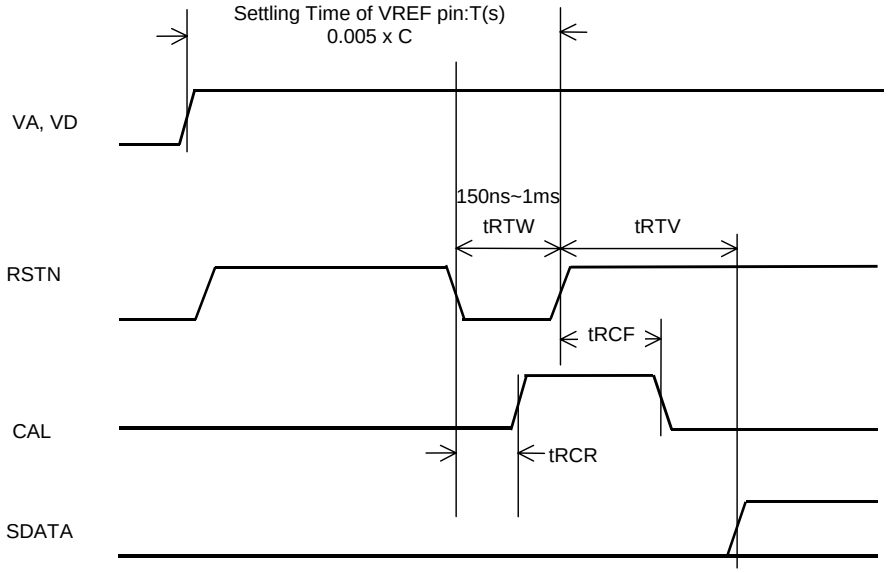

Figure 8. Reset & Calibration Timing

MEASUREMENT RESULTS

[Measurement condition]

- Measurement unit : Audio Precision System Two Cascade(AP2C) / ROHDE & SCHWARZ, UPD04 (R&S)
- MCLK : 12.288MHz
- BICK : 128fs for 48kHz, 64fs for 96kHz and 192kHz
- fs : 48kHz, 96kHz, 192kHz
- BW : 10Hz~20kHz (fs=48kHz)
- Resolution : 24bit
- Power Supply : VA=5V, VD=3.3V
- Interface : DIT / Serial MUX
- Temperature : Room

1. VREF cap = 10µF, Measurement Unit = AP2C ; I/F = Optical

Parameter	Input signal	Measurement filter	Results	
fs			48kHz	96kHz
BW			20kHz	Fs/2 (=48kHz)
S/(N+D)	1kHz, -1dB	-	106.0	105.6
	1kHz, -20dB	-	98.1	94.1
	1kHz, -60dB	-	57.3	54.1
DR	1kHz, -60dB	A-weighted	121.0	121.0
S/N	no signal	-	118.7	115.1
		A-weighted	121.1	121.2

[dB]

2. VREF cap = 10µF, Meas. Unit = R&S ; I/F = Serial MUX

Parameter	Input signal	Measurement filter	Results
fs			192kHz
BW			80kHz
S/(N+D)	1kHz, -1dB	-	105.1
	1kHz, -20dB	-	91.0
	1kHz, -60dB	-	54.1
DR	1kHz, -60dB	A-weighted	119.0
S/N	no signal	-	111.5
		A-weighted	120.3

[dB]

3. Example measurement, VREF cap=1000µF, Meas. Unit = AP2C; I/F = Optical,

Parameter	Input signal	Measurement filter	Results
fs			48kHz
BW			20kHz
S/(N+D)	1kHz, -1dB	-	111.1
DR	1kHz, -60dB	A-weighted	121.6
S/N	No signal	A-weighted	121.4

[dB]

■ Plots

Measurement unit : Audio Precision, System two, Cascade (fs=48kHz,96kHz),
ROHDE & SCHWARZ, UPD04 (fs=192kHz), VREF cap = 10μF

1. AP2C
(FFT : BW=fs/2, point=16384)
1-1. fs=48kHz
Figure 1-1-1. FFT (1kHz, –1dB input)
Figure 1-1-2. FFT (1kHz, –60dB input)
Figure 1-1-3. FFT (off the input)
Figure 1-1-4. THD+N vs Input Frequency (-1dB input)
Figure 1-1-5. THD+N vs Input Level (1kHz input)
Figure 1-1-6. Linearity (fin=1kHz)
Figure 1-1-7. Frequency Response (-1dB input)
Figure 1-1-8. Cross-talk (-1dB input)
1-2. fs=96kHz
Figure 1-2-1. FFT (1kHz, –1dB input)
Figure 1-2-2. FFT (1kHz, –60dB input)
Figure 1-2-3. FFT (off the input)
Figure 1-2-4. THD+N vs Input Frequency (-1dB input)
Figure 1-2-5. THD+N vs Input Level (1kHz input)
Figure 1-2-6. Linearity (fin=1kHz)
Figure 1-2-7. Frequency Response (-1dB input)
Figure 1-2-8. Cross-talk (-1dB input)

2. R&S
(FFT : BW=fs/2, point=8192)
2-1. fs=192kHz
Figure 2-1-1. FFT (1kHz, –1dB input)
Figure 2-1-2. FFT (1kHz, –60dB input)
Figure 2-1-3. FFT (off the input)
Figure 2-1-4. THD+N vs Input Frequency (-1dB input)
Figure 2-1-5. THD+N vs Input Level (1kHz input)
Figure 2-1-6. Linearity (fin=1kHz)
Figure 2-1-7. Frequency Response (-1dB input)

1. AP2C

1-1. fs=48kHz

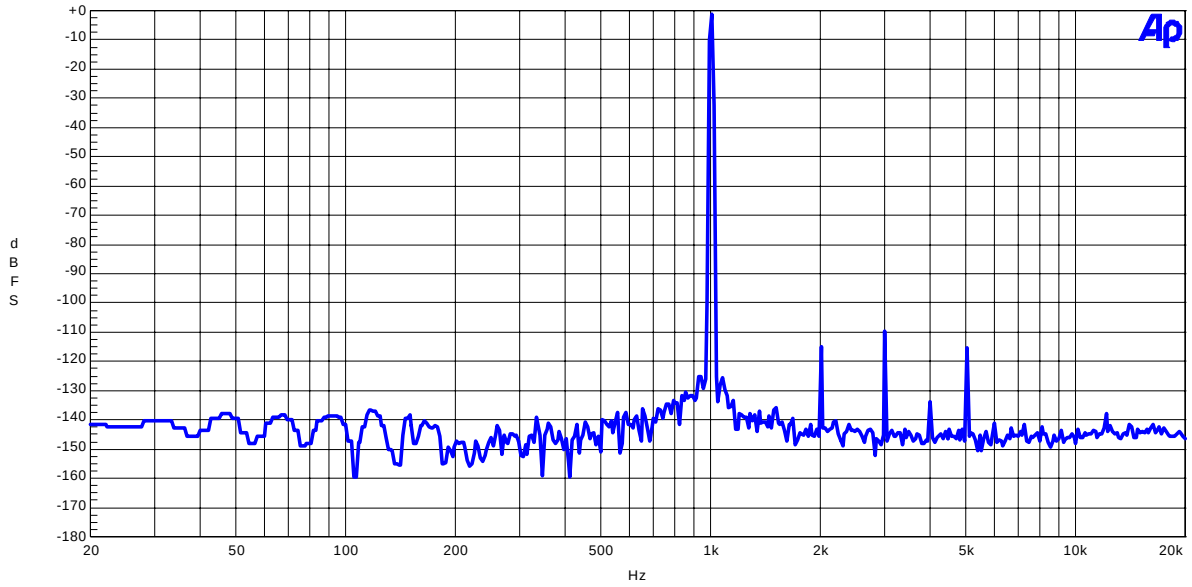

Figure 1-1-1. FFT (1kHz, –1dB input)

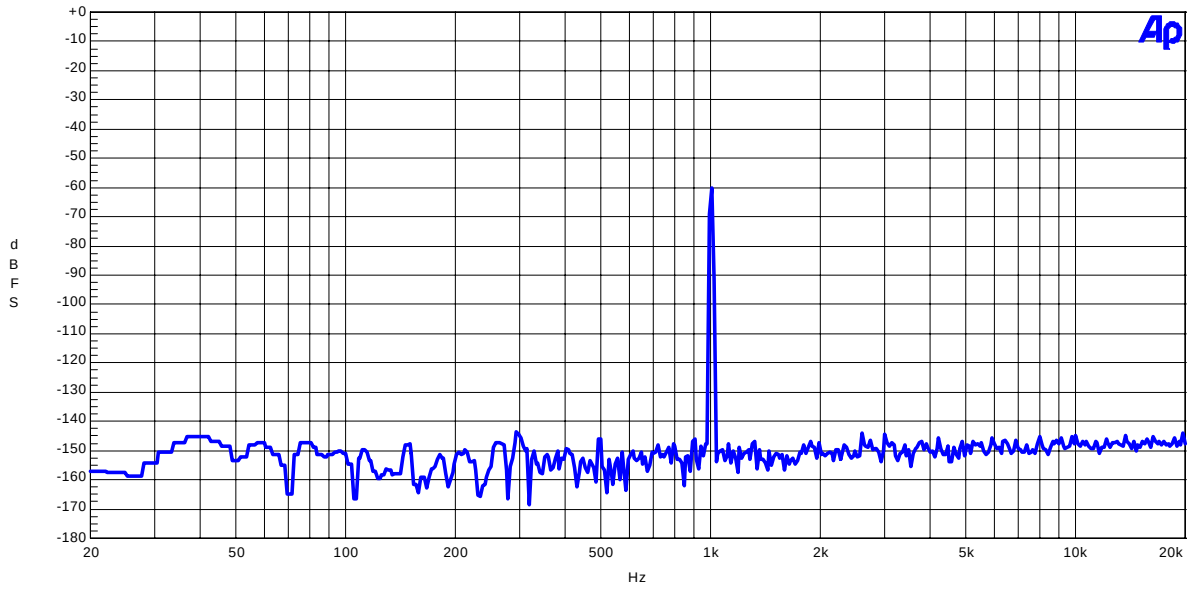

Figure 1-1-2. FFT (1kHz, –60dB input)

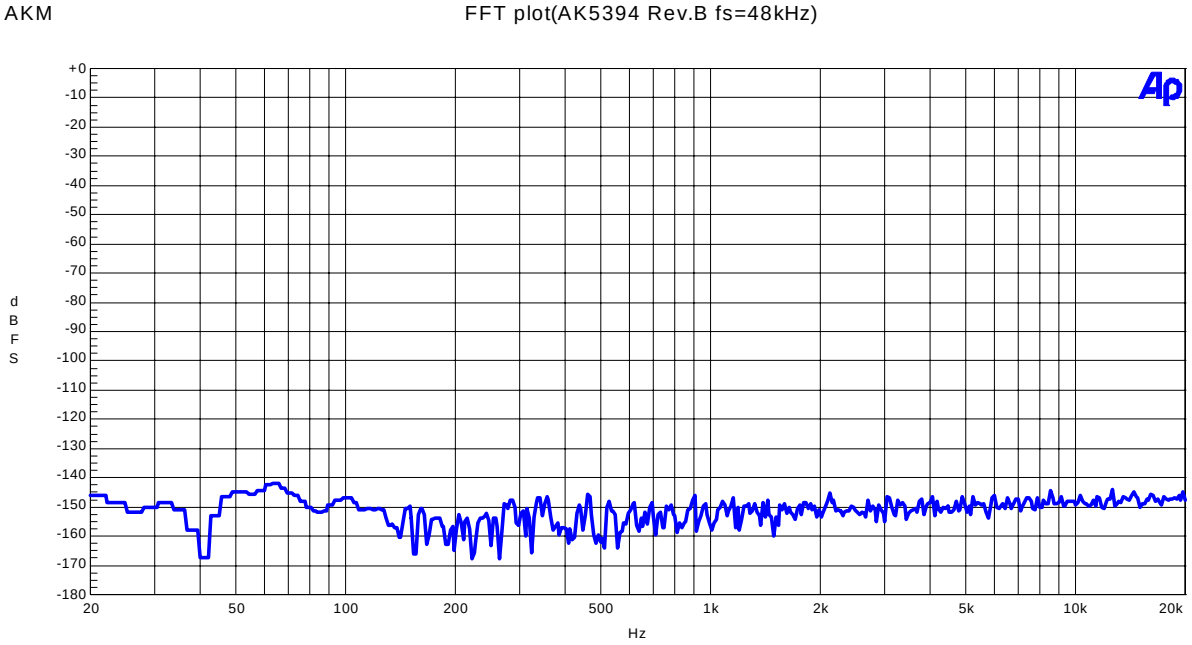

Figure 1-1-3. FFT (off the input)

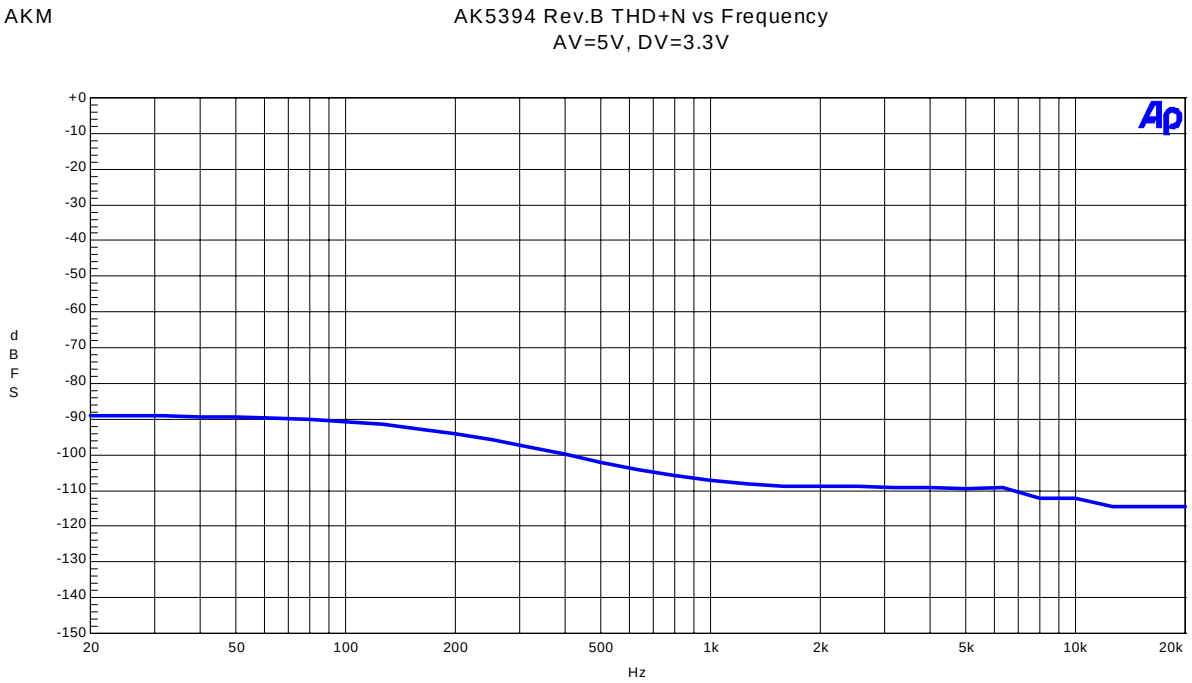

Figure 1-1-4. THD+N vs Input Frequency (-1dB input)

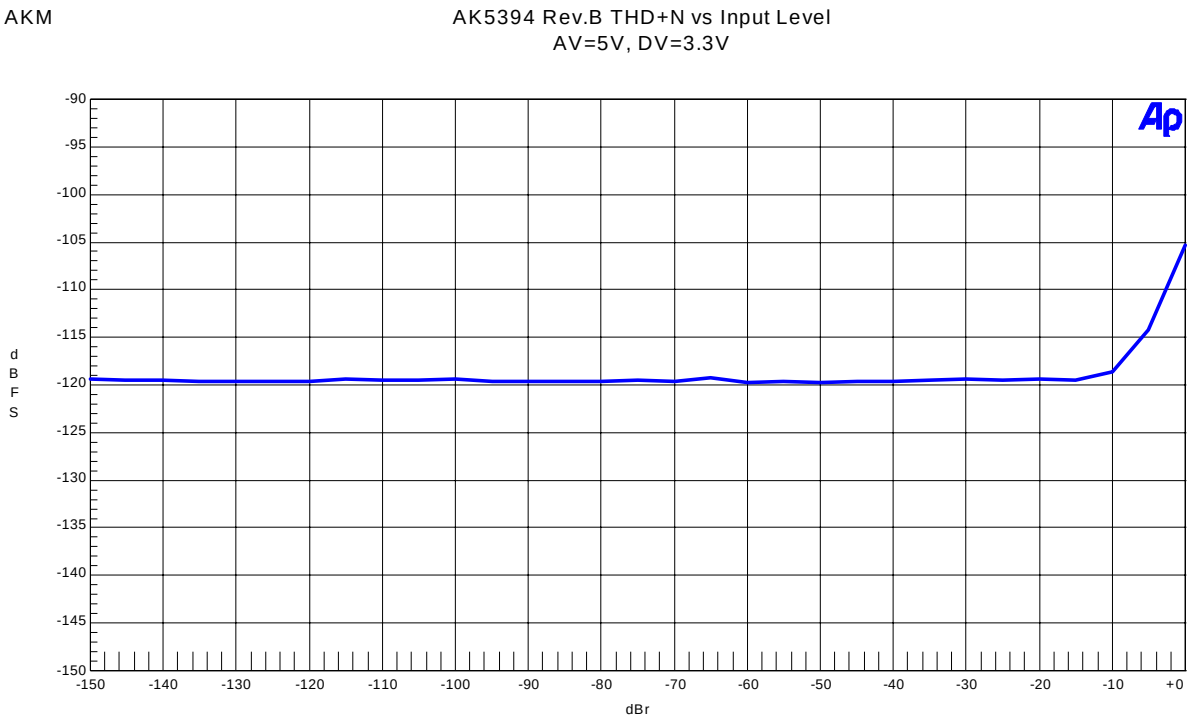

Figure 1-1-5. THD+N vs Input Level (1kHz input)

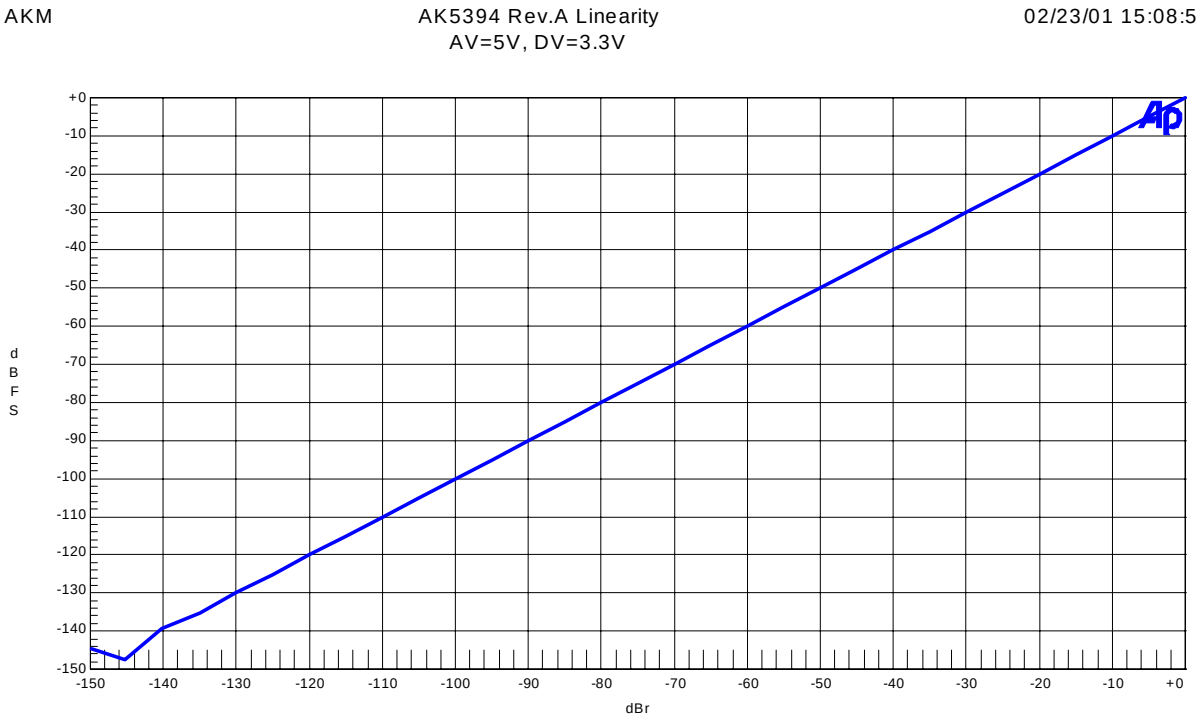

Figure 1-1-6. Linearity (fin=1kHz)

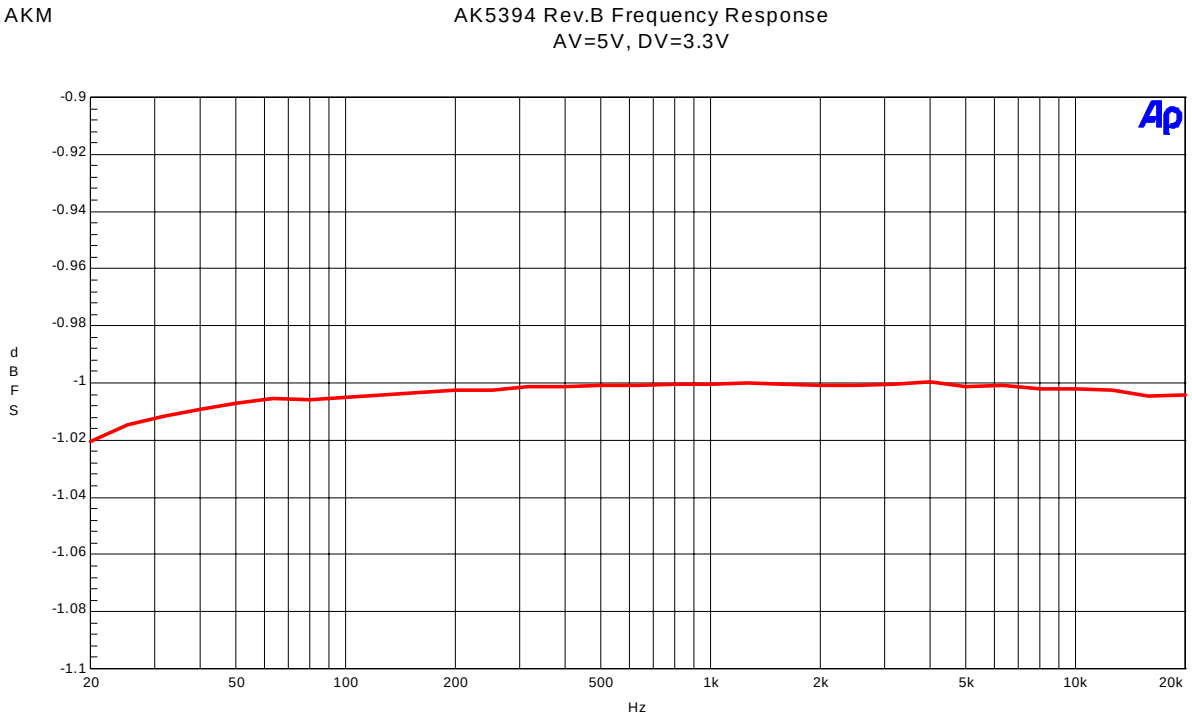

Figure 1-1-7. Frequency Response (-1dB input)

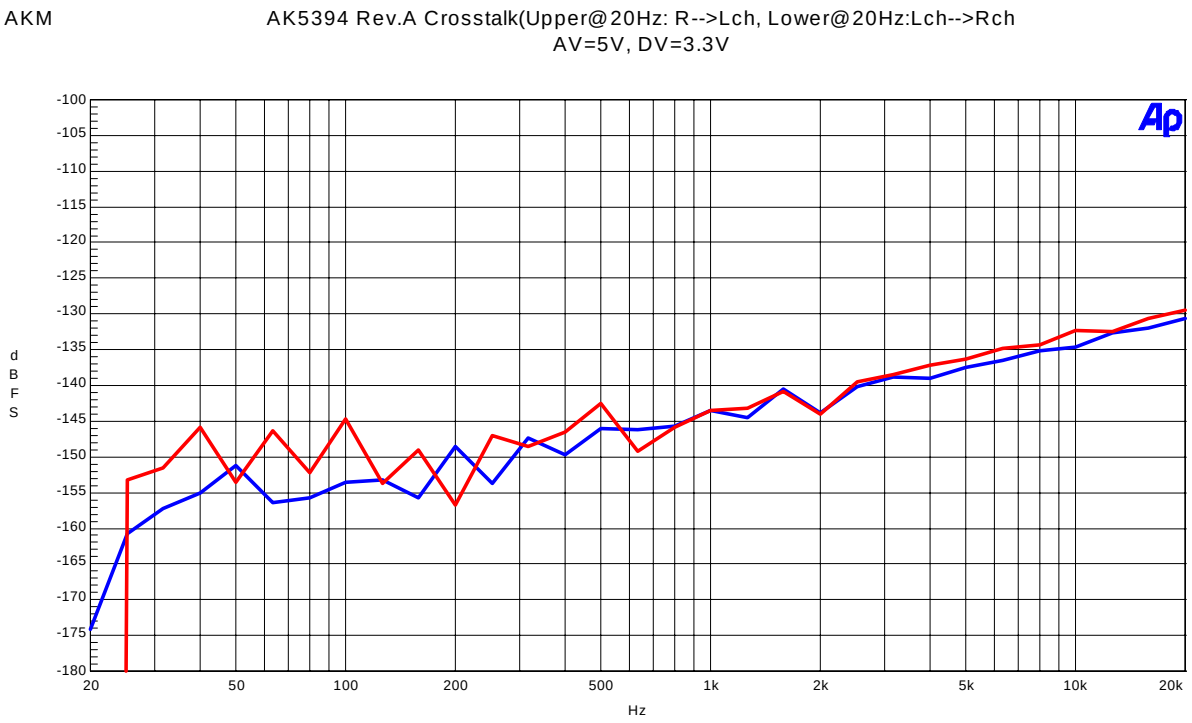

Figure 1-1-8. Cross-talk (-1dB input)

1-2. fs=96kHz

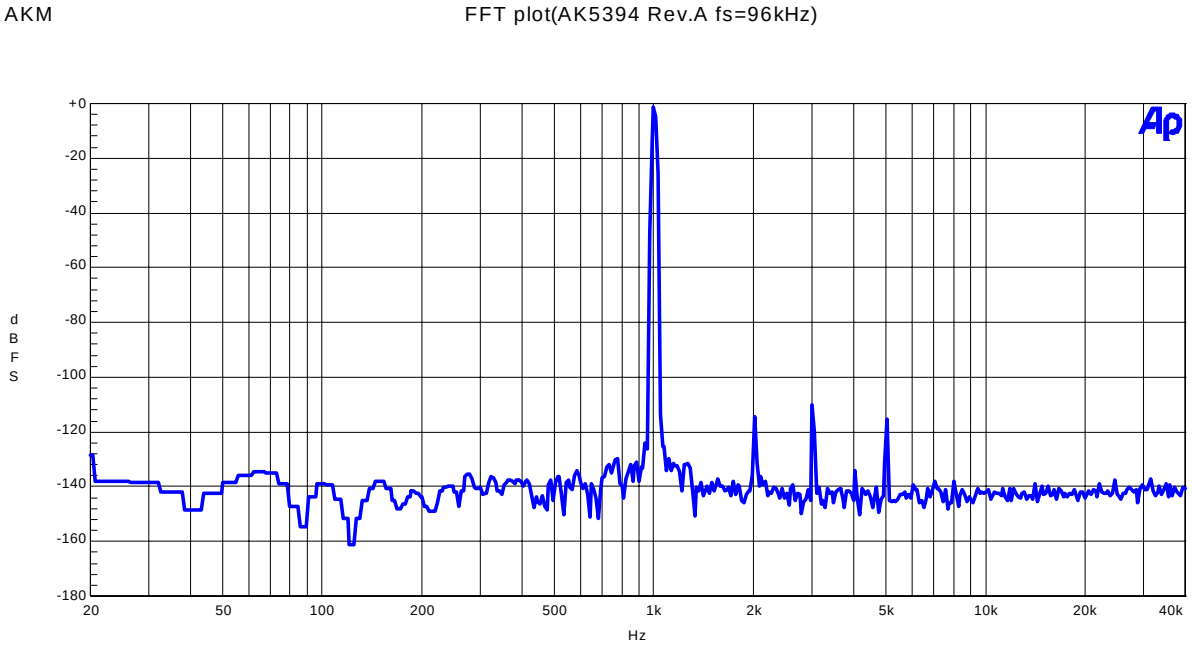

Figure 1-2-1. FFT (1kHz, –1dB input)

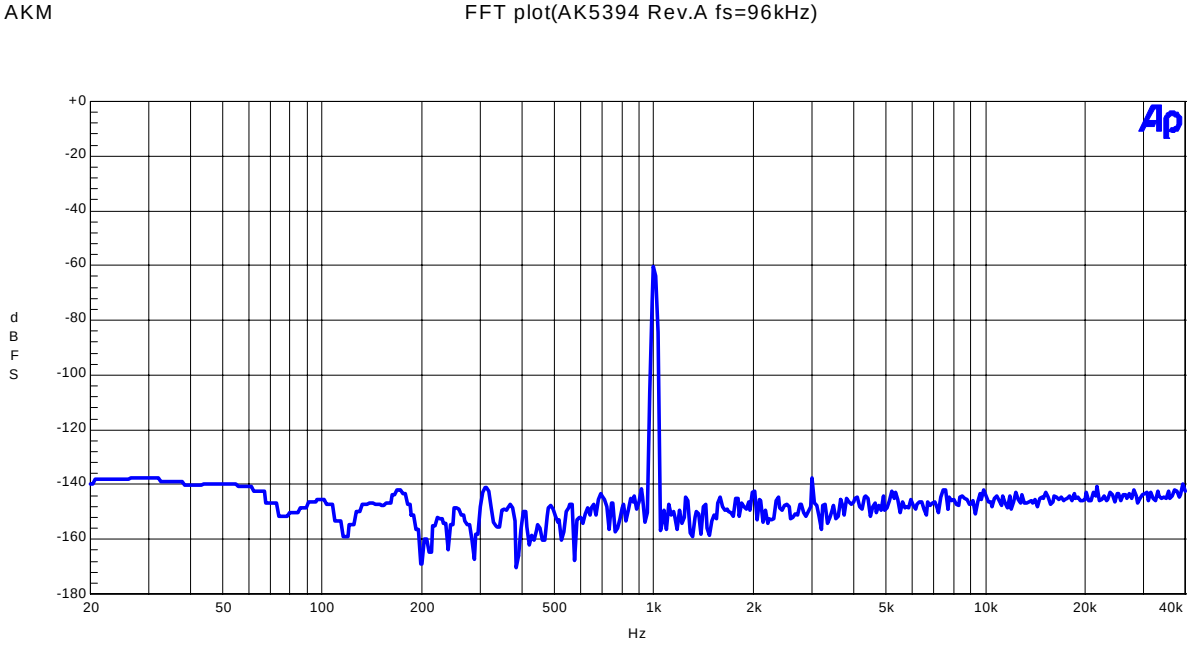

Figure 1-2-2. FFT (1kHz, –60dB input)

AKM FFT plot(AK5394 Rev.A fs=96kHz)

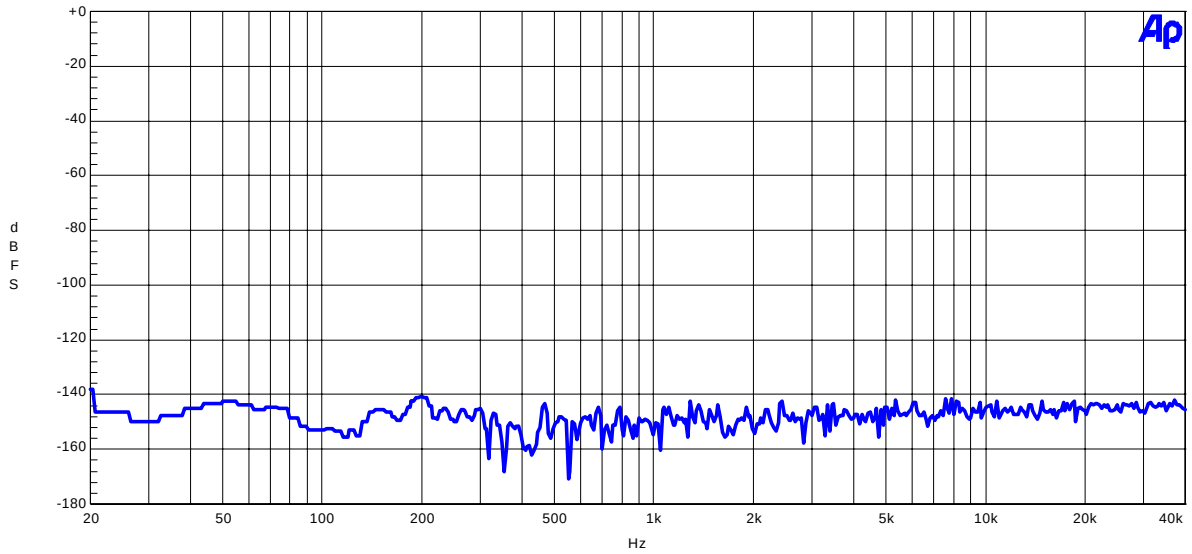

Figure 1-2-3. FFT (1kHz, –60dB input)

AKM AK5394 Rev.A THD+N vs Frequency, fs=96k
AV=5V, DV=3.3V

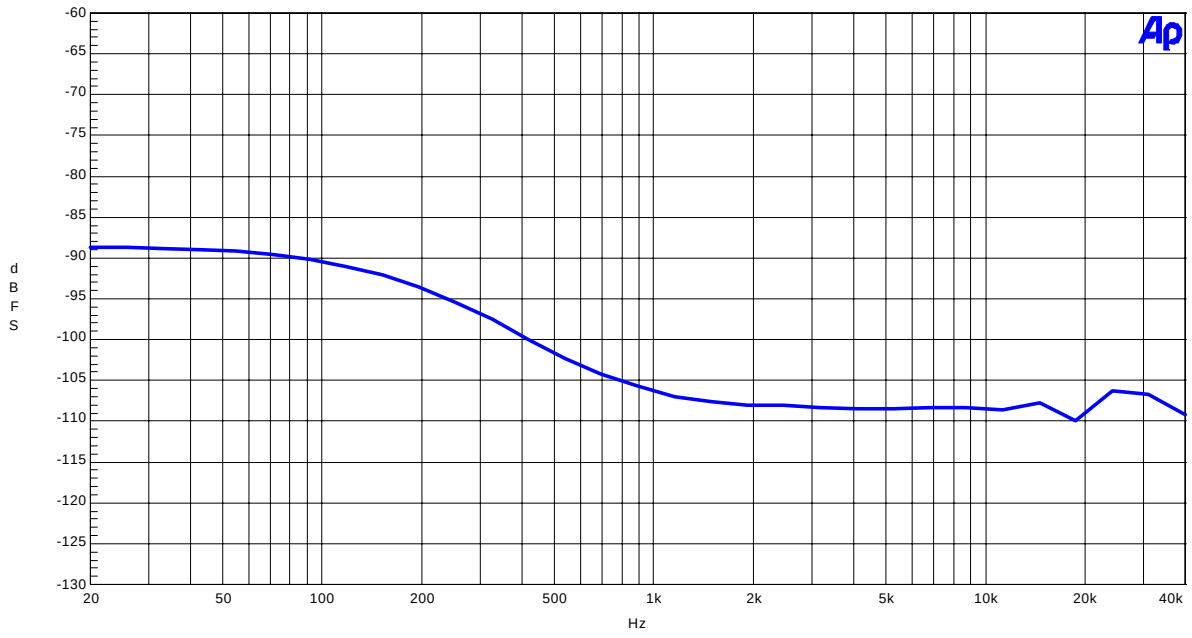

Figure 1-2-4. FFT (off the input)

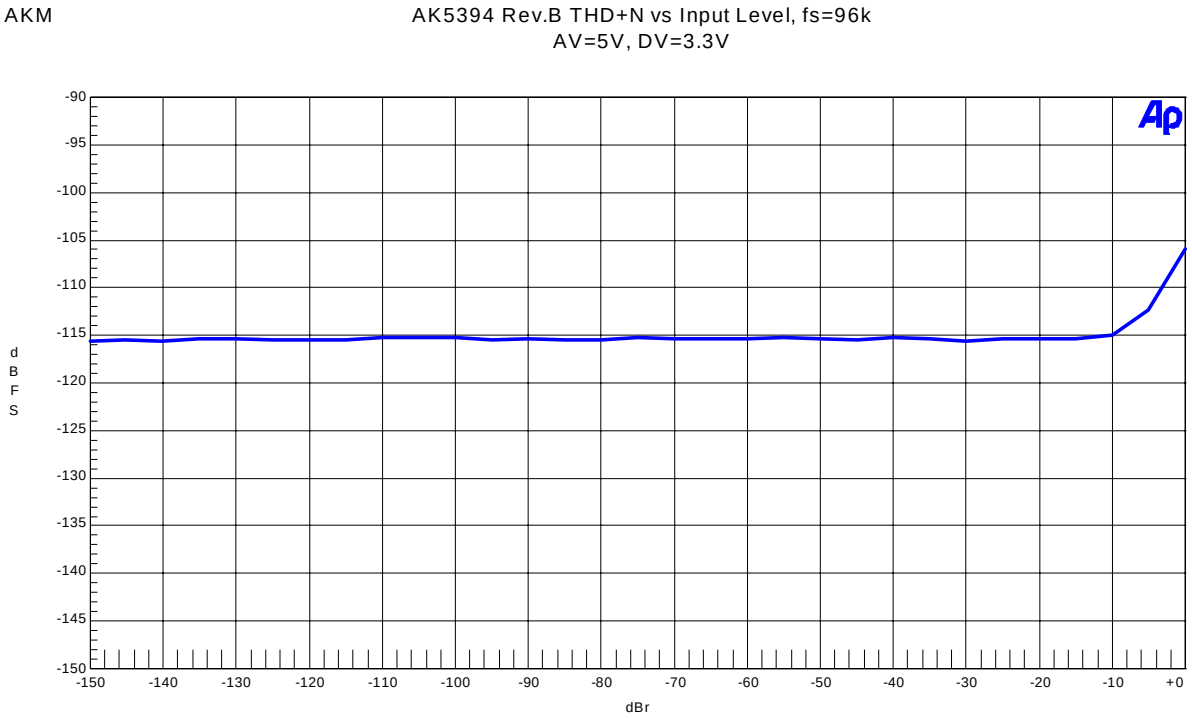

Figure 1-2-5. THD+N vs Input Level (1kHz input)

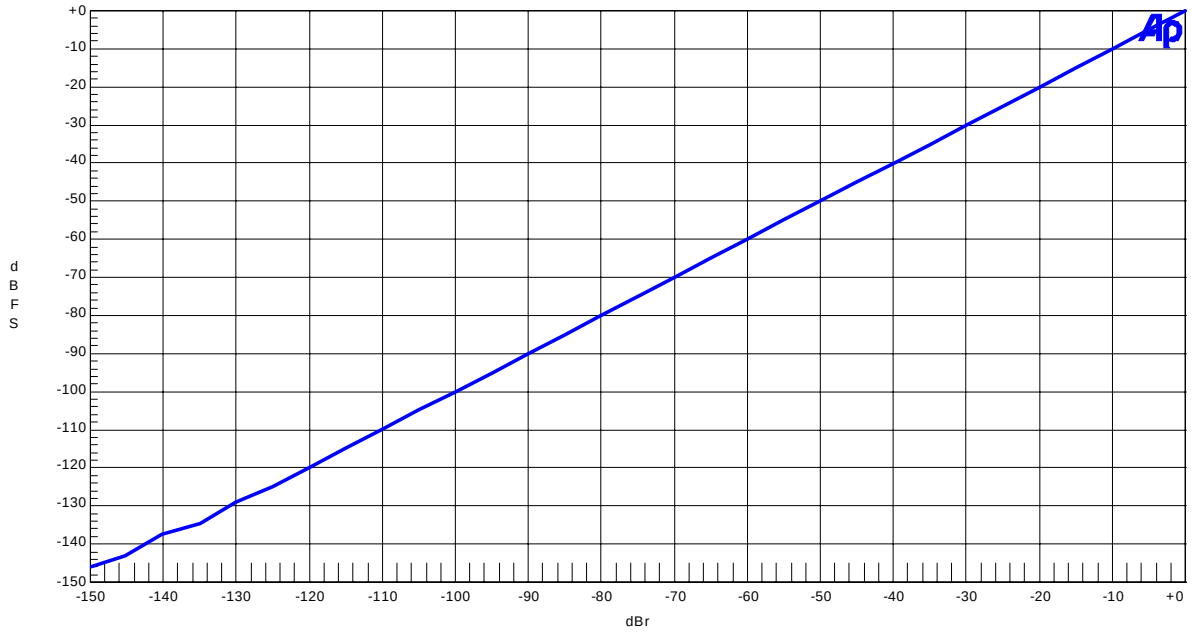

Figure 1-2-6. Linearity (fin=1kHz)

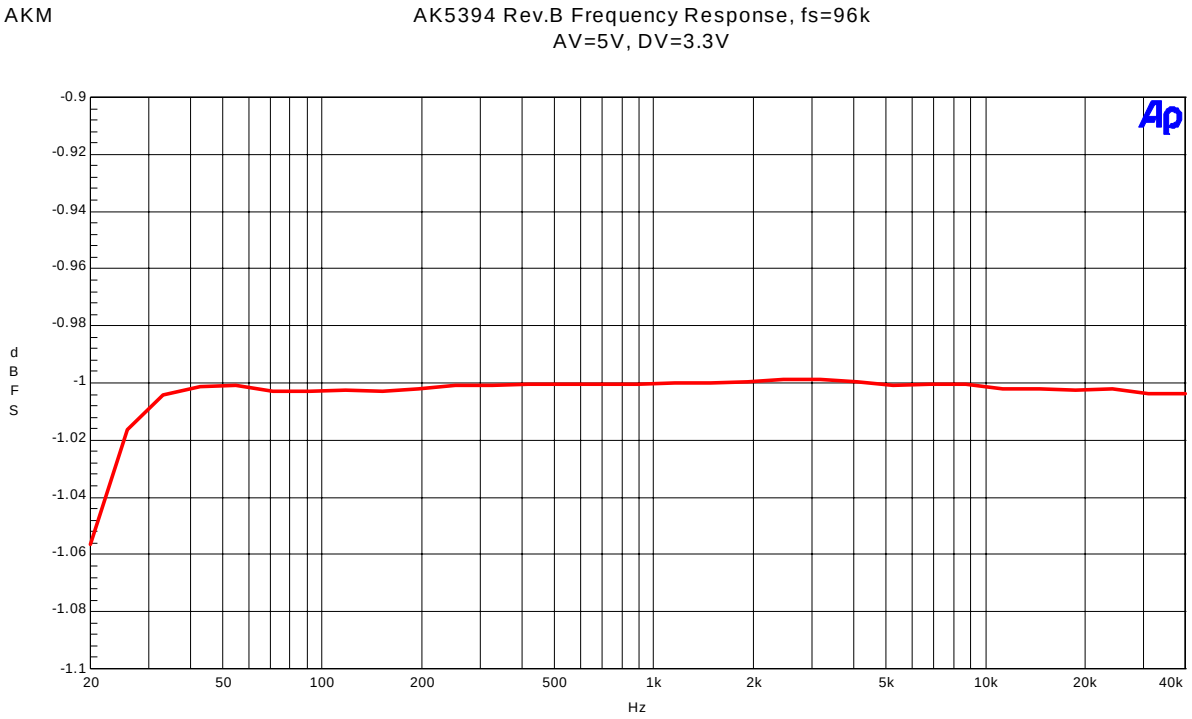

Figure 1-2-7. Frequency Response (-1dB input)

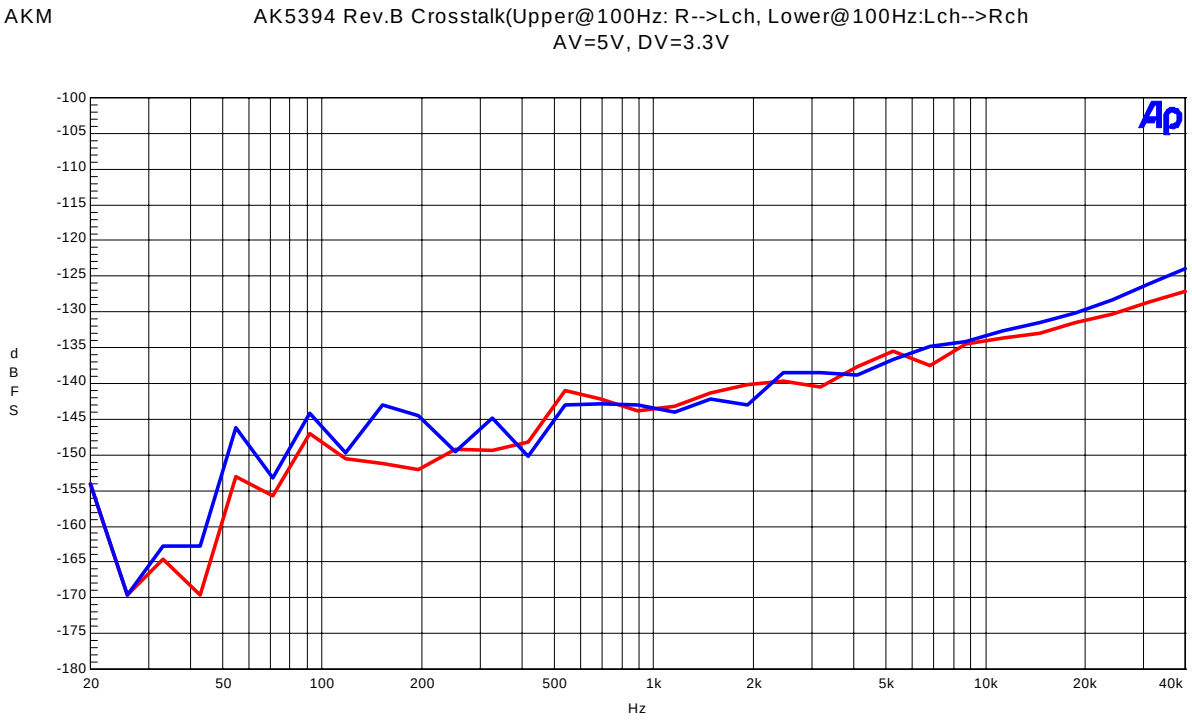

Figure 1-2-8. Cross-talk (-1dB input)

2-3. fs=192kHz

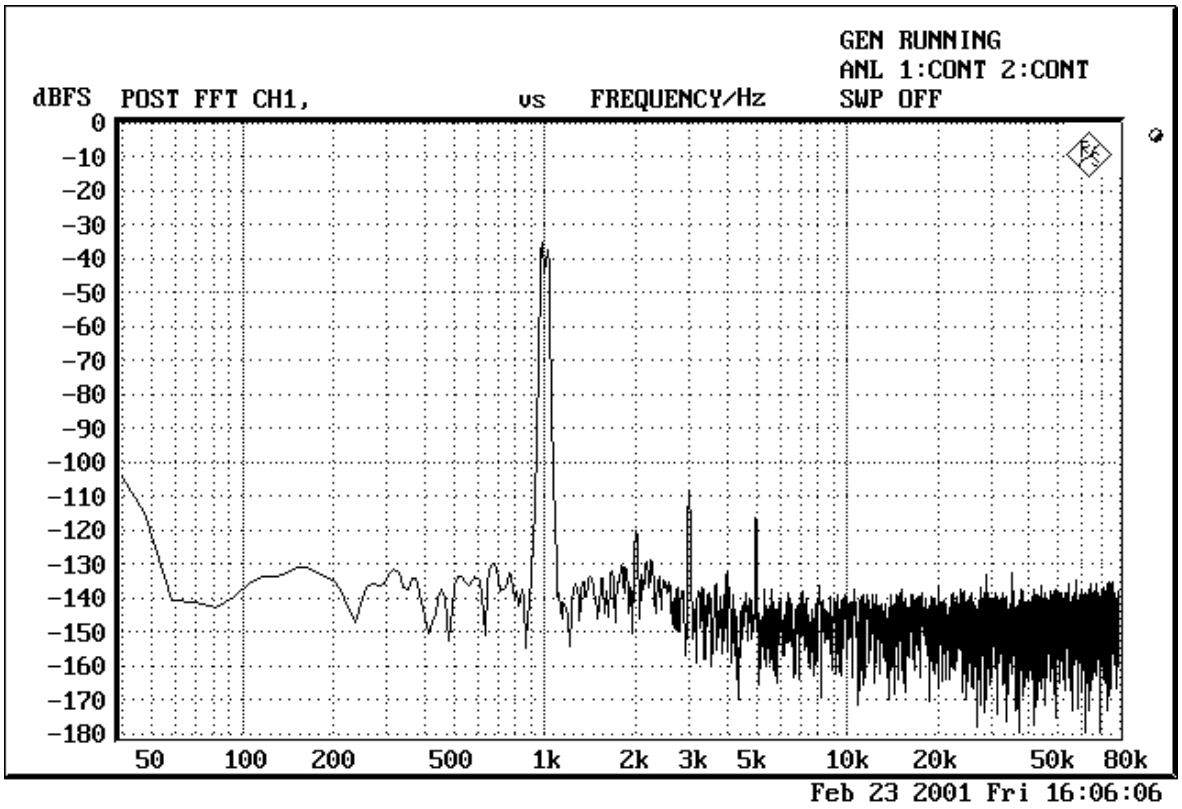

Figure 2-1-1. FFT (1kHz, –1dB input)

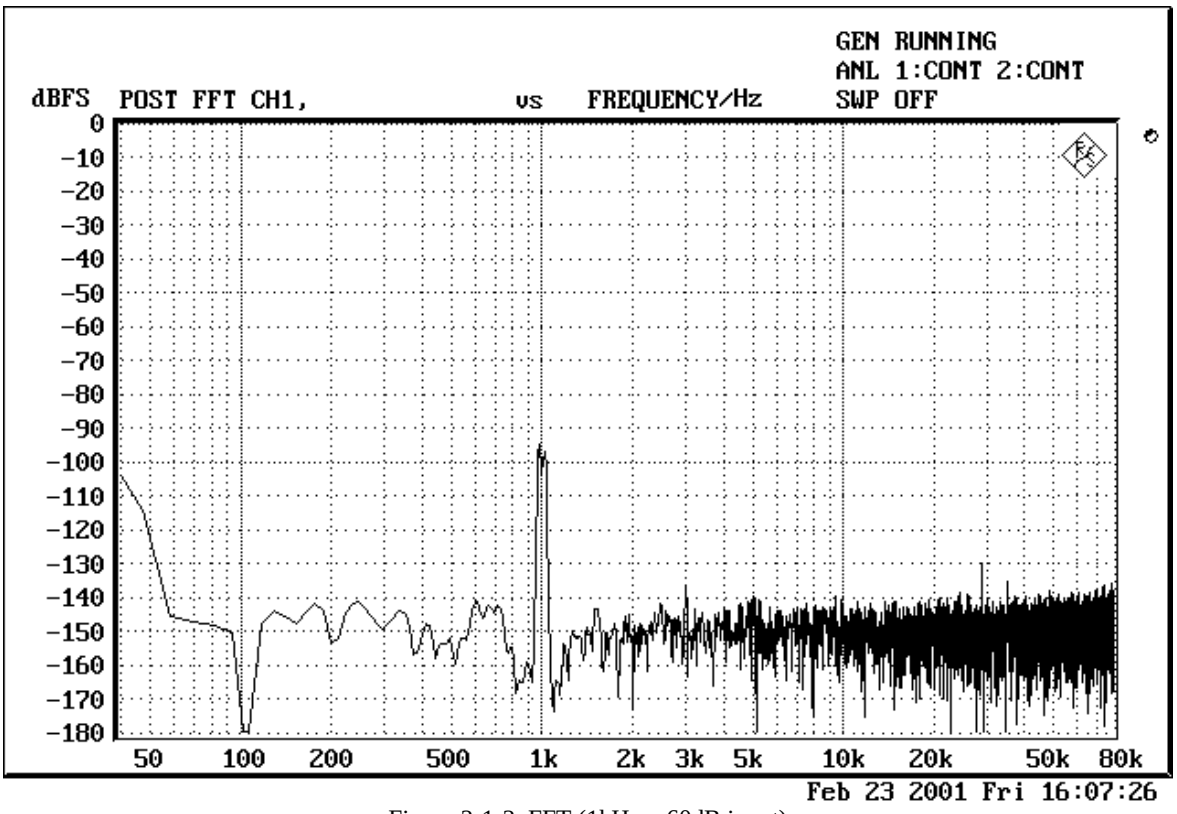

Figure 2-1-2. FFT (1kHz, –60dB input)

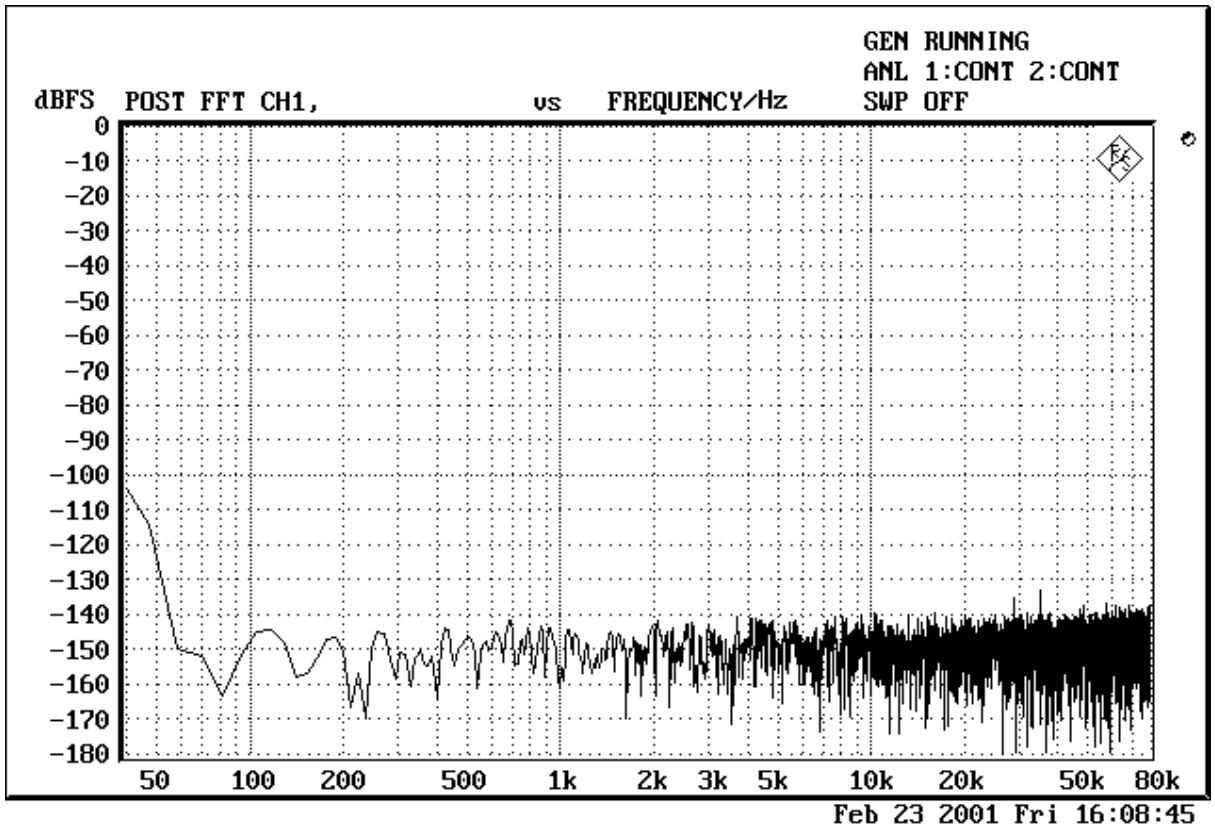

Figure 2-1-3. FFT (off the input)

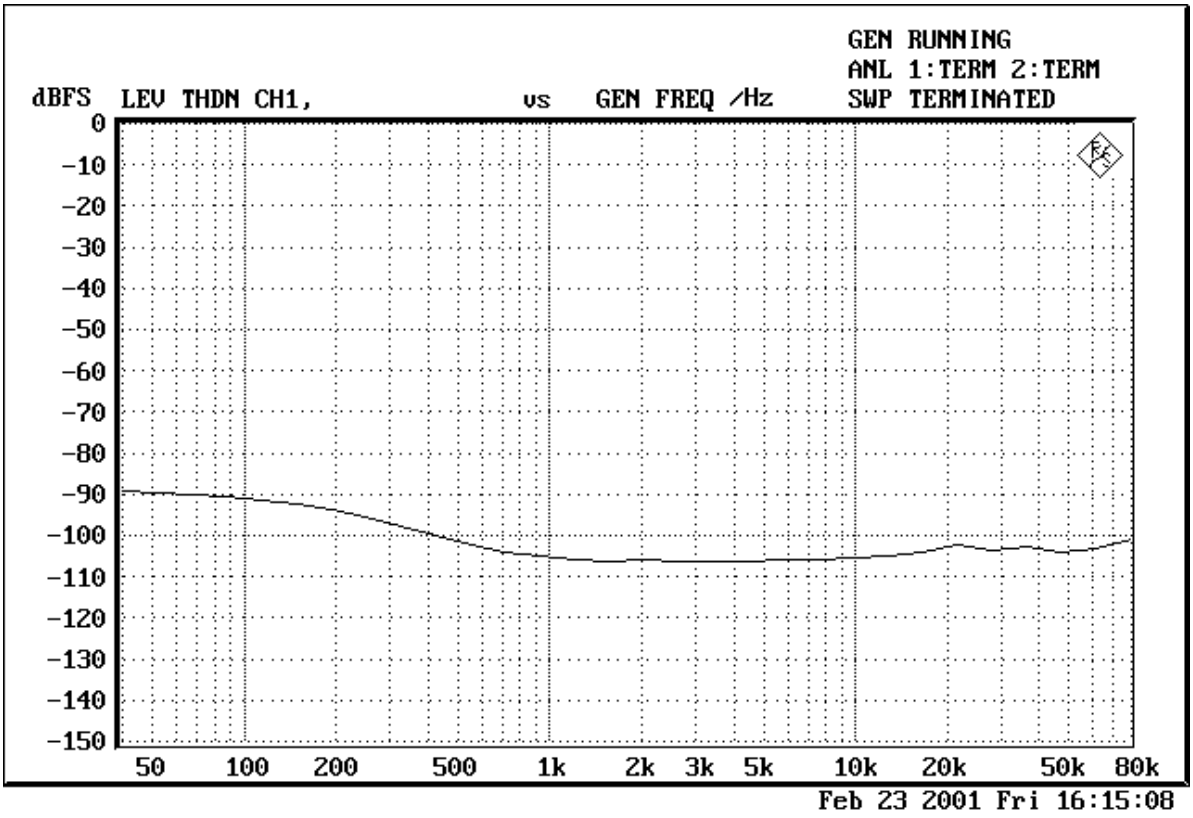

Figure 2-1-4. THD+N vs Input Frequency (-1dB input)

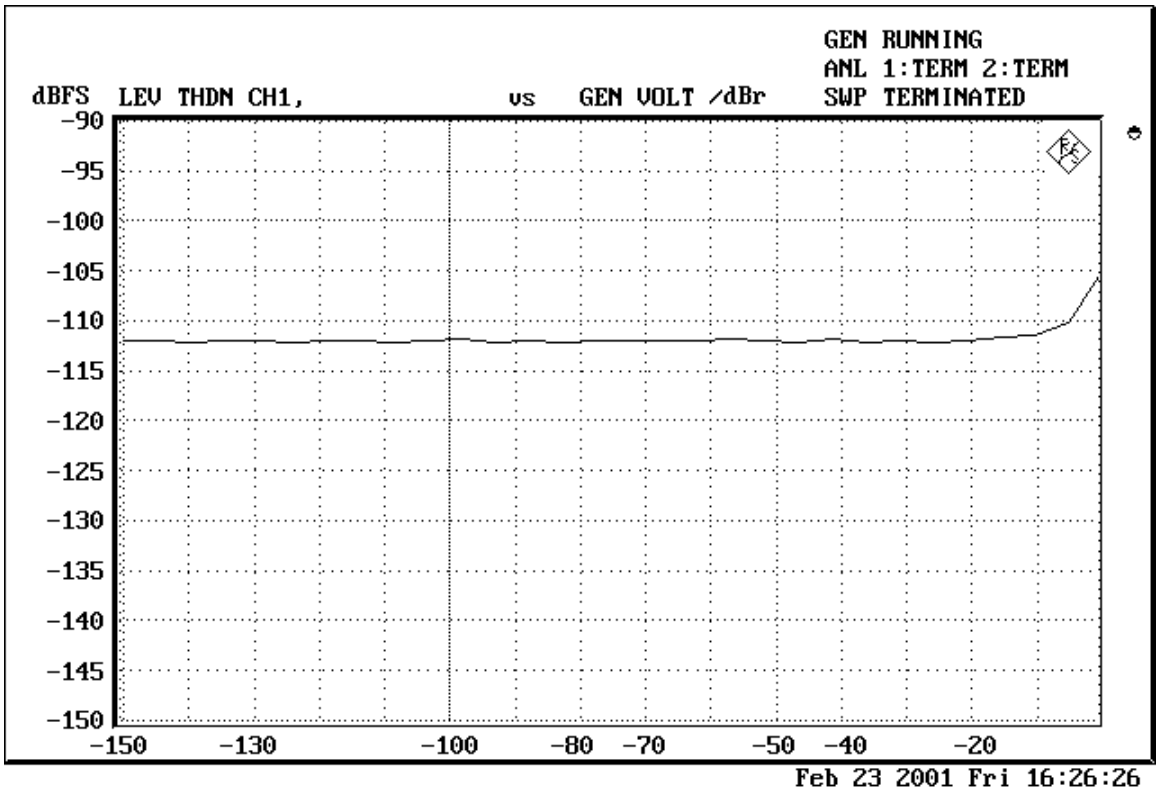

Figure 2-1-5. THD+N vs Input Level (1kHz input)

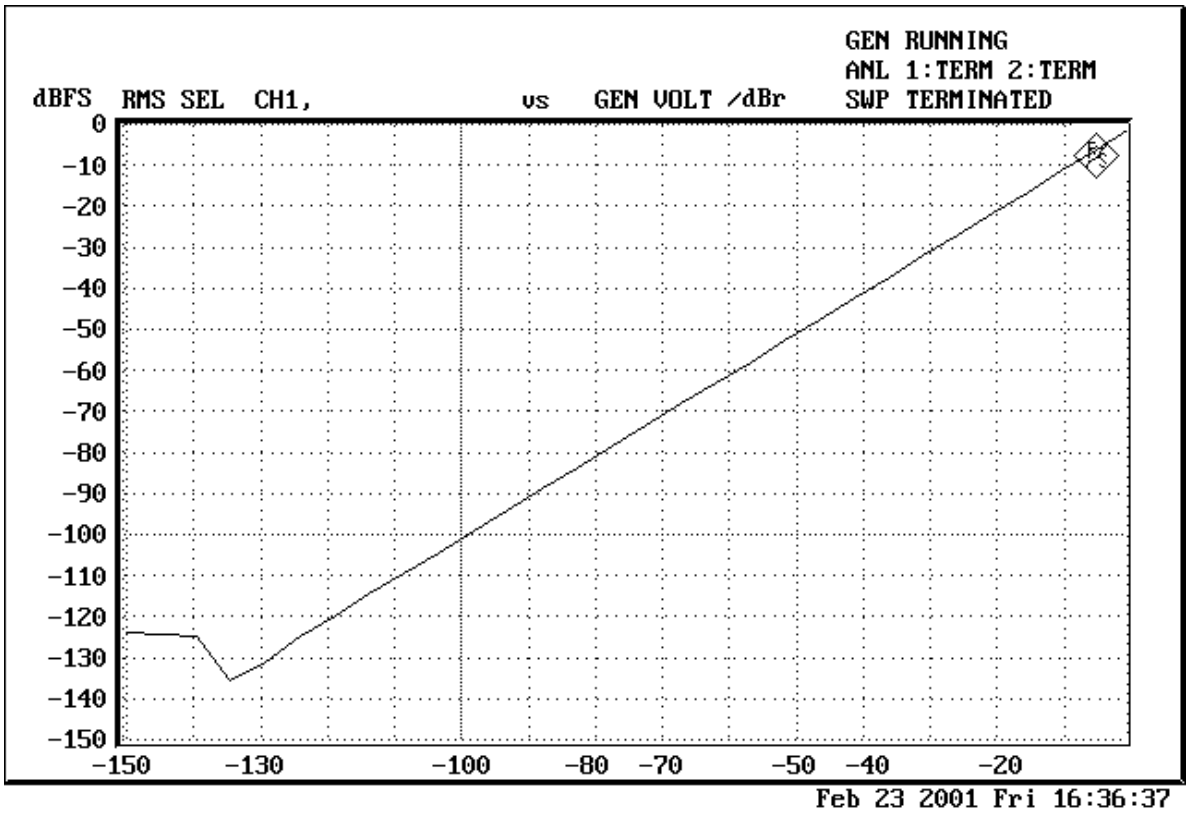

Figure 2-1-6. Linearity (fin=1kHz)

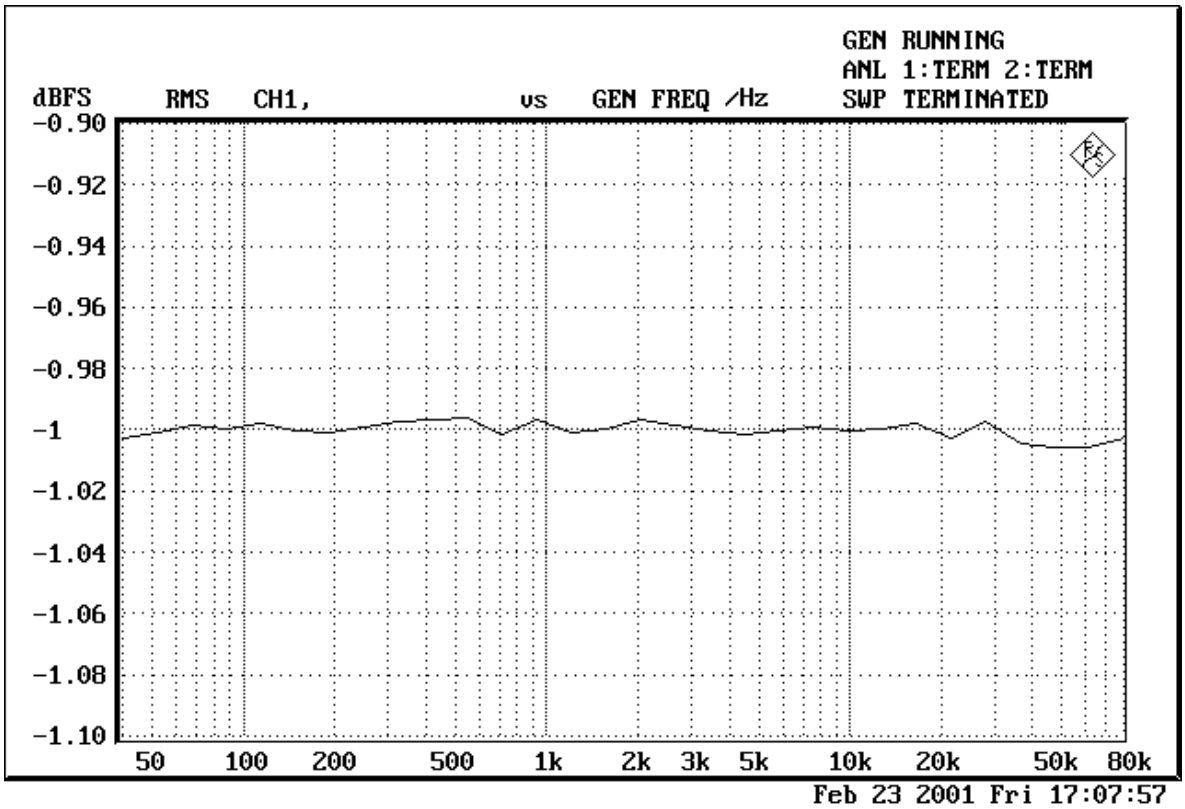

Figure 2-1-7. Frequency Response (-1dB input)

Revision History

Date (YY/MM/DD)	Manual Revision	Board Revision	Reason	Contents
01/03/06	KM064800	0	First edition	
01/12/11	KM064801	0	Device Name Change	AK5394 →AK5394A
			Board Name Change	AKD5394 →AKD5394A
04/11/16	KM064802	1	Circuit Change (Additional description)	Unused input pins of CMOS-IC→DGND U2(74HC14) : 11pin→DGND 13pin→DGND U13(74HCU04) : 11pin→DGND 13pin→DGND
05/01/18	KM064803	2	Circuit Change (Exchange signal lines)	Analog input : AINL+ ←→ AINL- AINR+ ←→ AINR-
			Error Correct	Setting of jumper pin : Default setting : [JP1](5394_VA) : open→short [JP12](LRCK) : 96K→48K [JP16](XTE) : no description→open Operation sequence : 1) Set up the power supply lines : Connector name : [4103]→[4103_VD] Jumper pin number : JP12(IF/5V)→ JP15(IF/5V) Device name for DIT : AK4103→AK4103A
			Change figures and tables	Evaluation mode : Setting of DIP switches
			Additional figure	Analog input buffer circuit example
			Additional comment	Setting of jumper pin
05/05/19	KM064804	3	Circuit Change (Resistance Value Change)	Resistance: R27, R29: 4.7K → 10K

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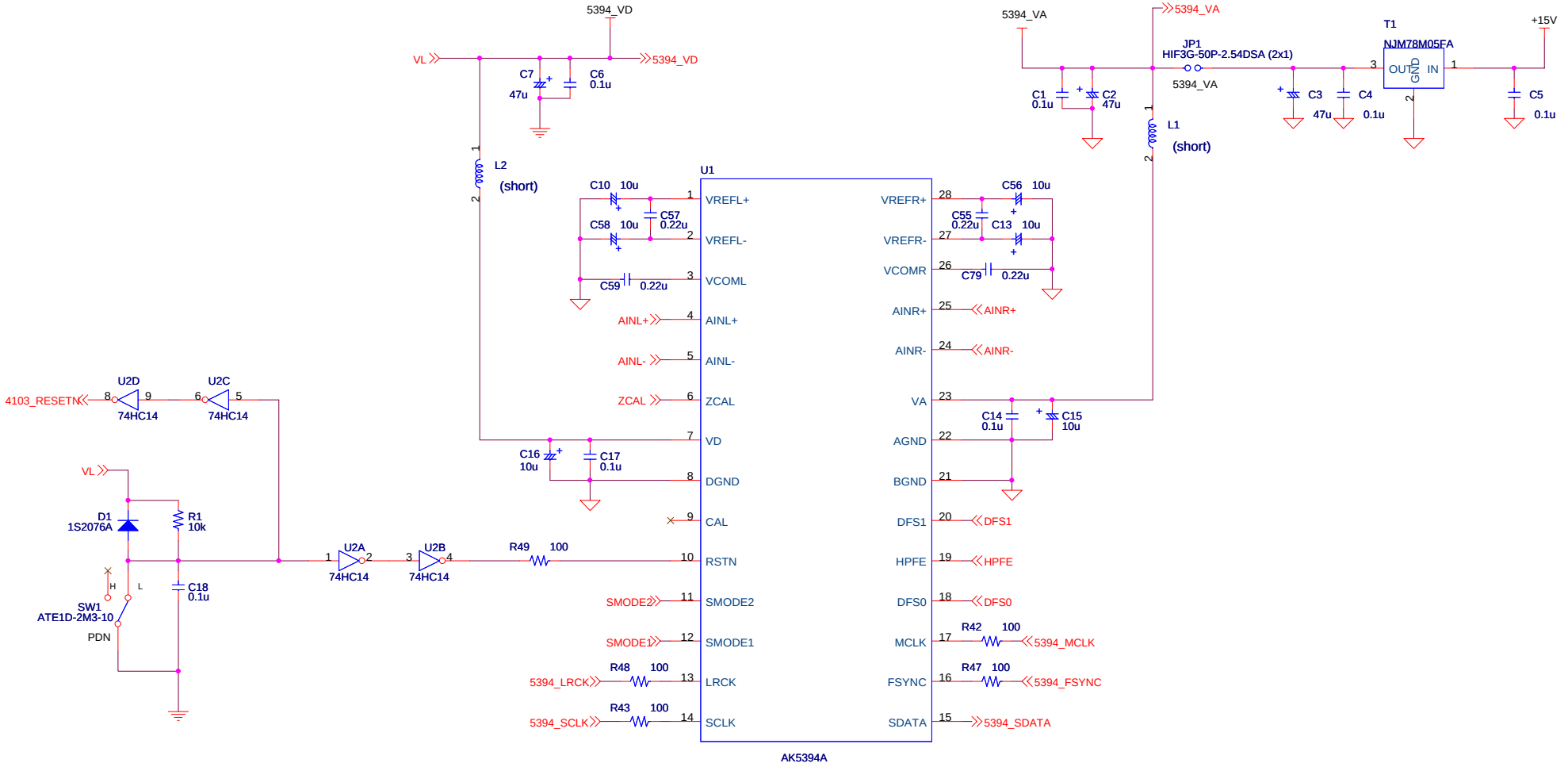

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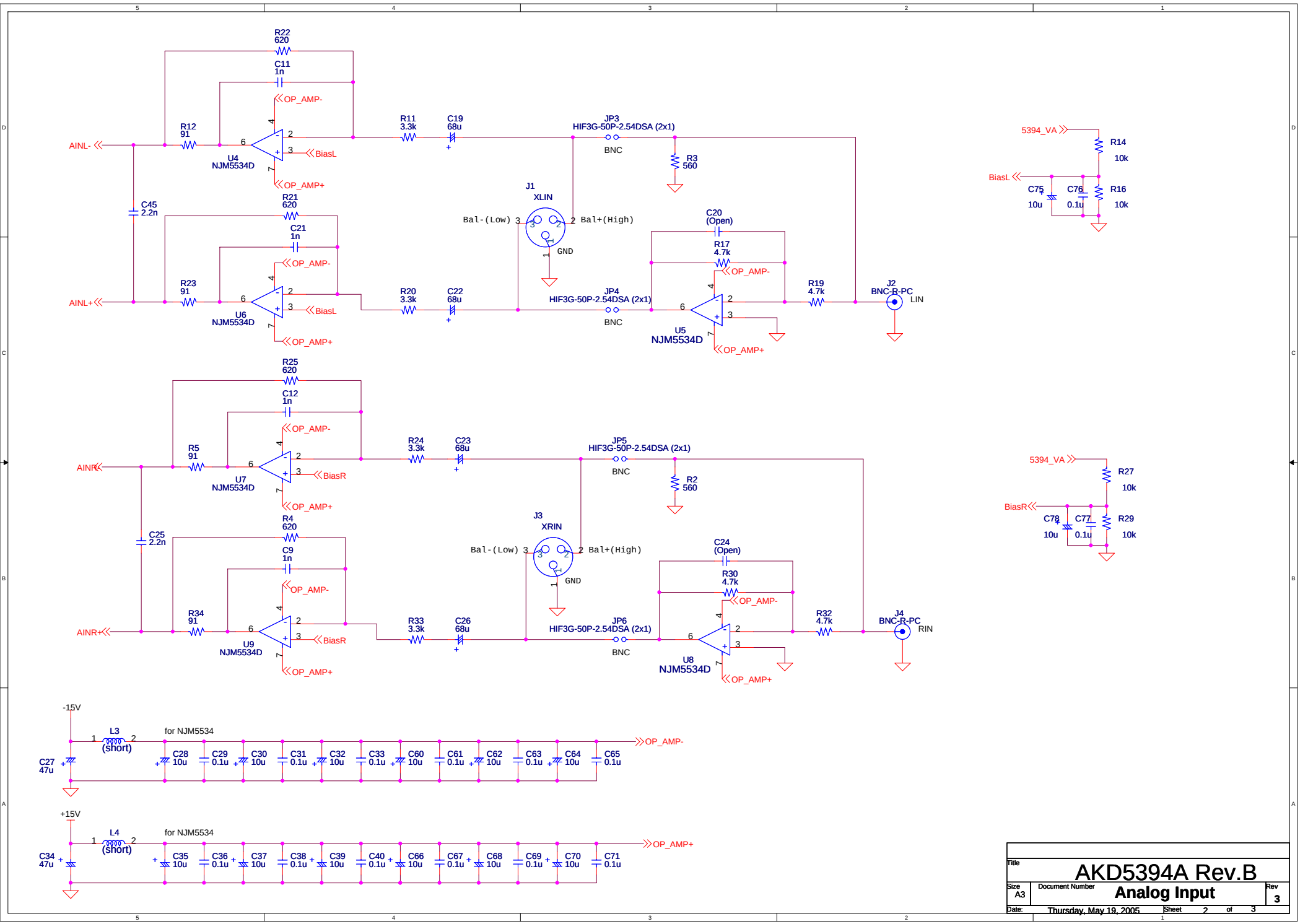
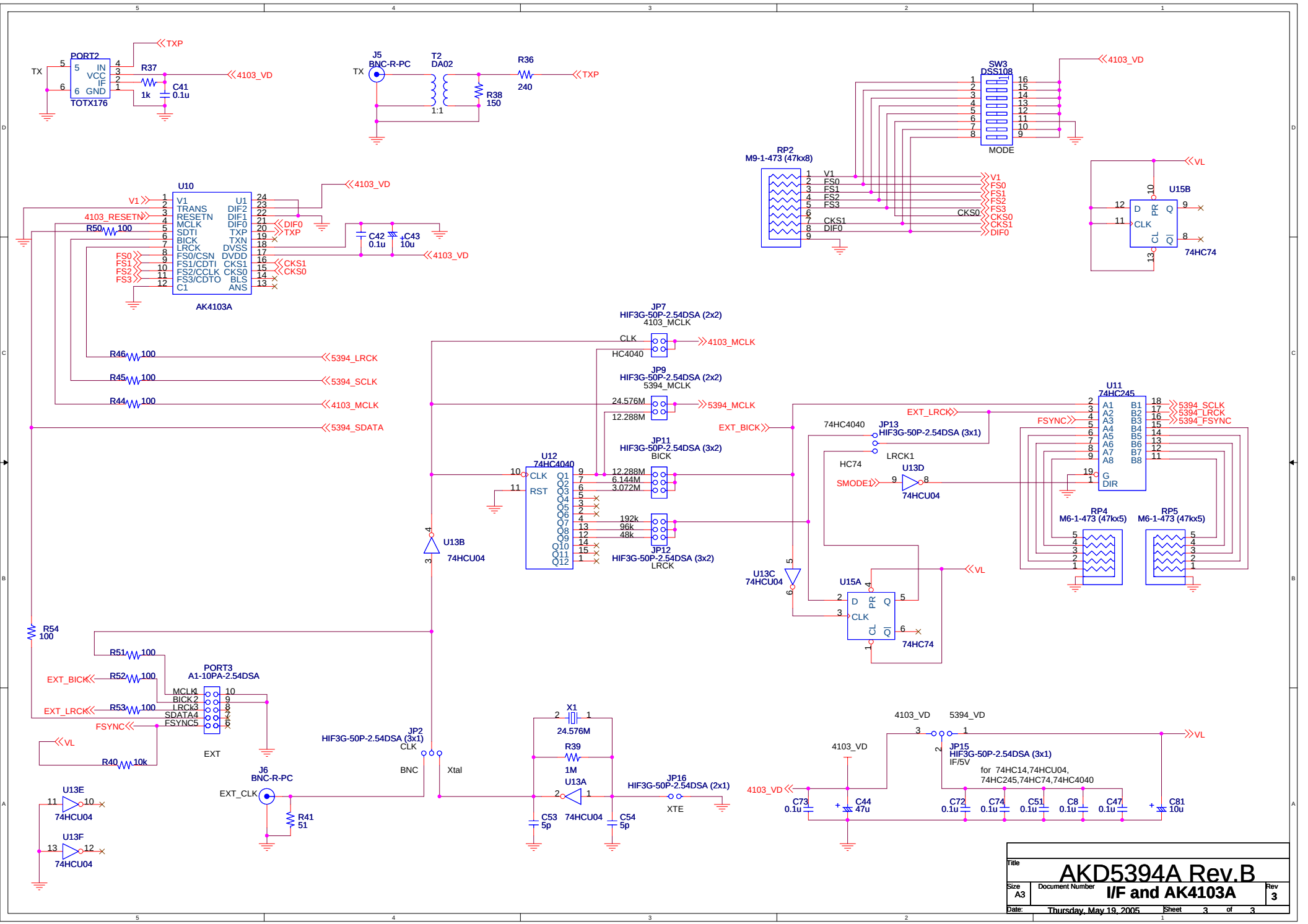
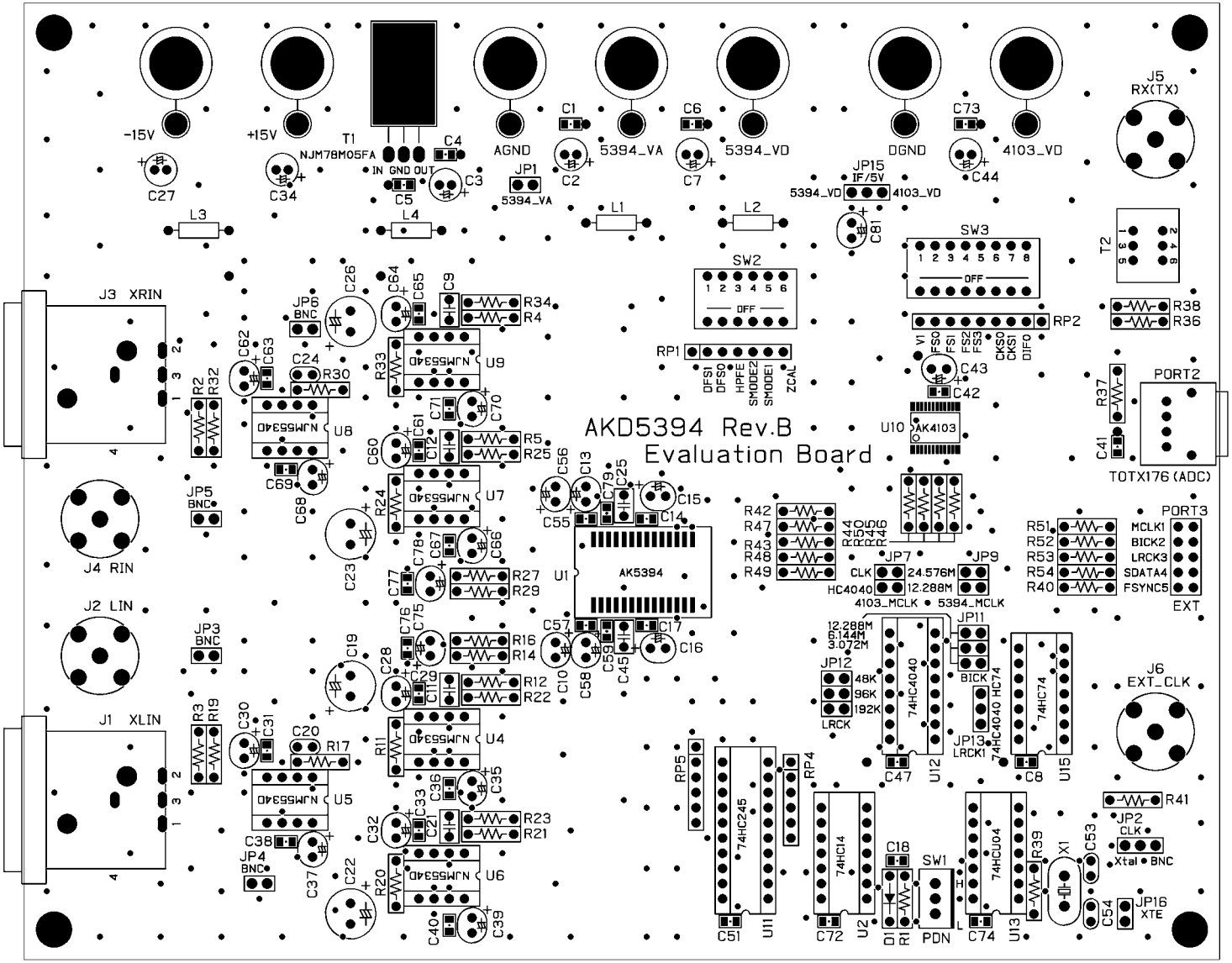
Size A3	Document Number **AK5394A**		Rev 3
Date: Thursday, May 19, 2005	Sheet 1 of 3		



Title	AKD5394A Rev.B		
Size A3	Document Number **Analog Input**		Rev 3
Date: Thursday, May 19, 2005	Sheet 2 of 3		



Title	AKD5394A Rev.B		
Size A3	Document Number I/F and AK4103A		Rev 3
Date: Thursday, May 19, 2005		Sheet 3 of 3	


AKD5394 Rev.B
Evaluation Board
AK5394
J1 XLIN
J2 LIN
J3 XRIN
J4 RIN
J5 RX(TX)
J6 EXT_CLK
PORT2
TOTX176 (ADC)
PORT3
EXT
-15V
+15V
AGND
5394_VA
5394_VD
DGND
4103_VD
NJM78M05FA
IN GND OUT
U1
U2
U4
U5
U6
U7
U8
U9
U10
U11
U12
U13
U15
SW1
SW2
SW3
RP1
RP2
RP4
RP5
X1
T1
T2
L1
L2
L3
L4
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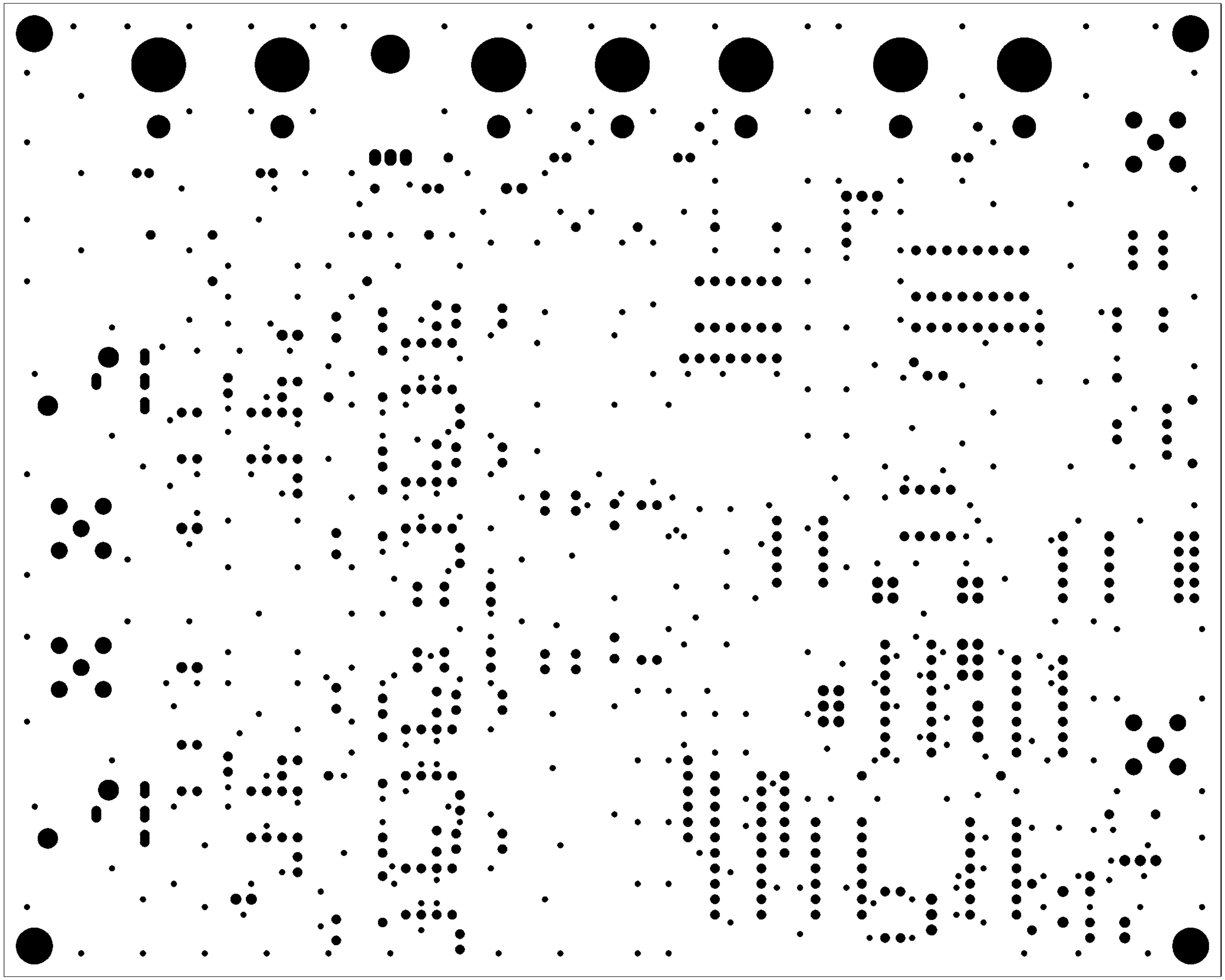
74HCU04
AK4103
PDN
Xtal • BNC
AKD5394 Rev.B L1 SR SILK



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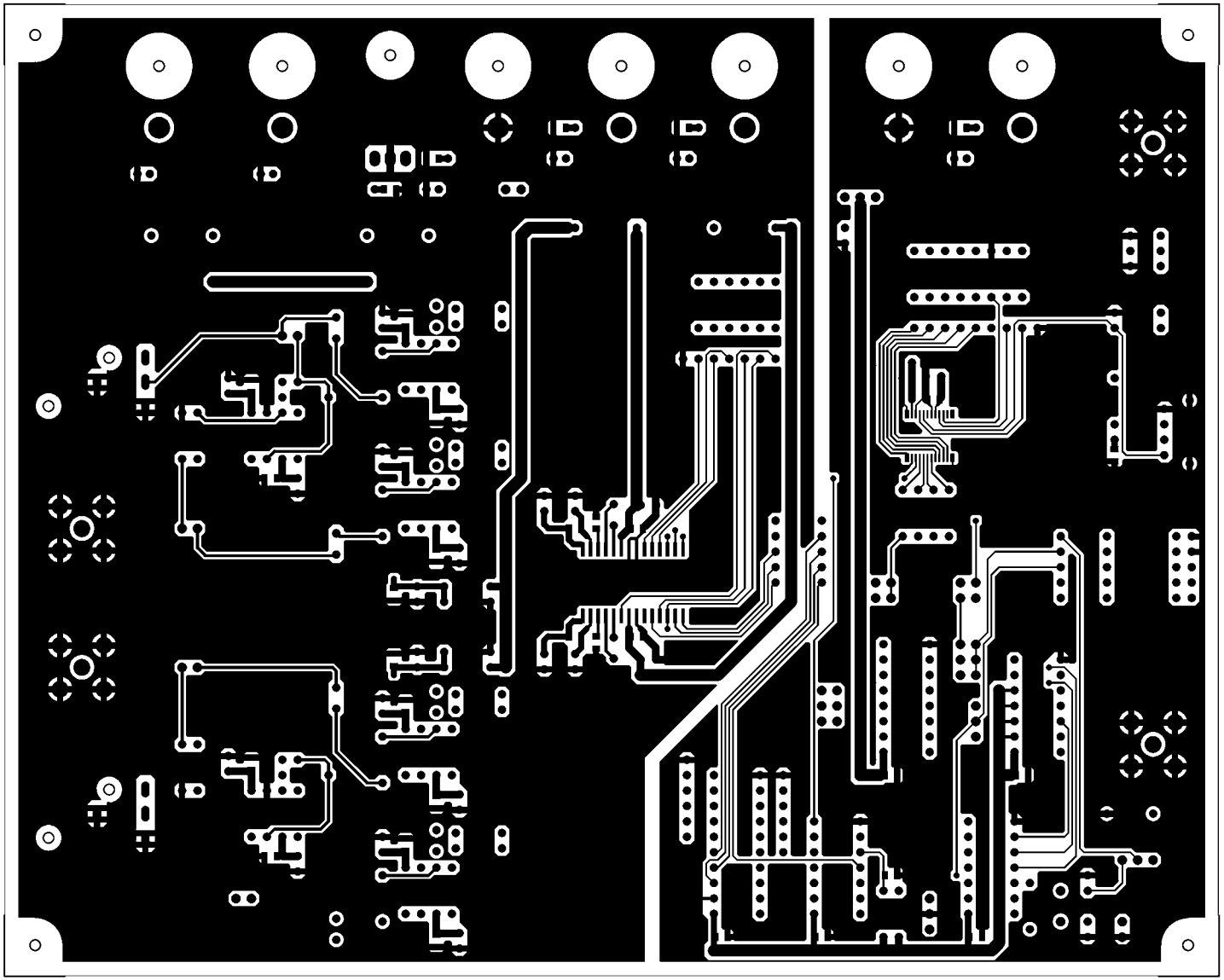

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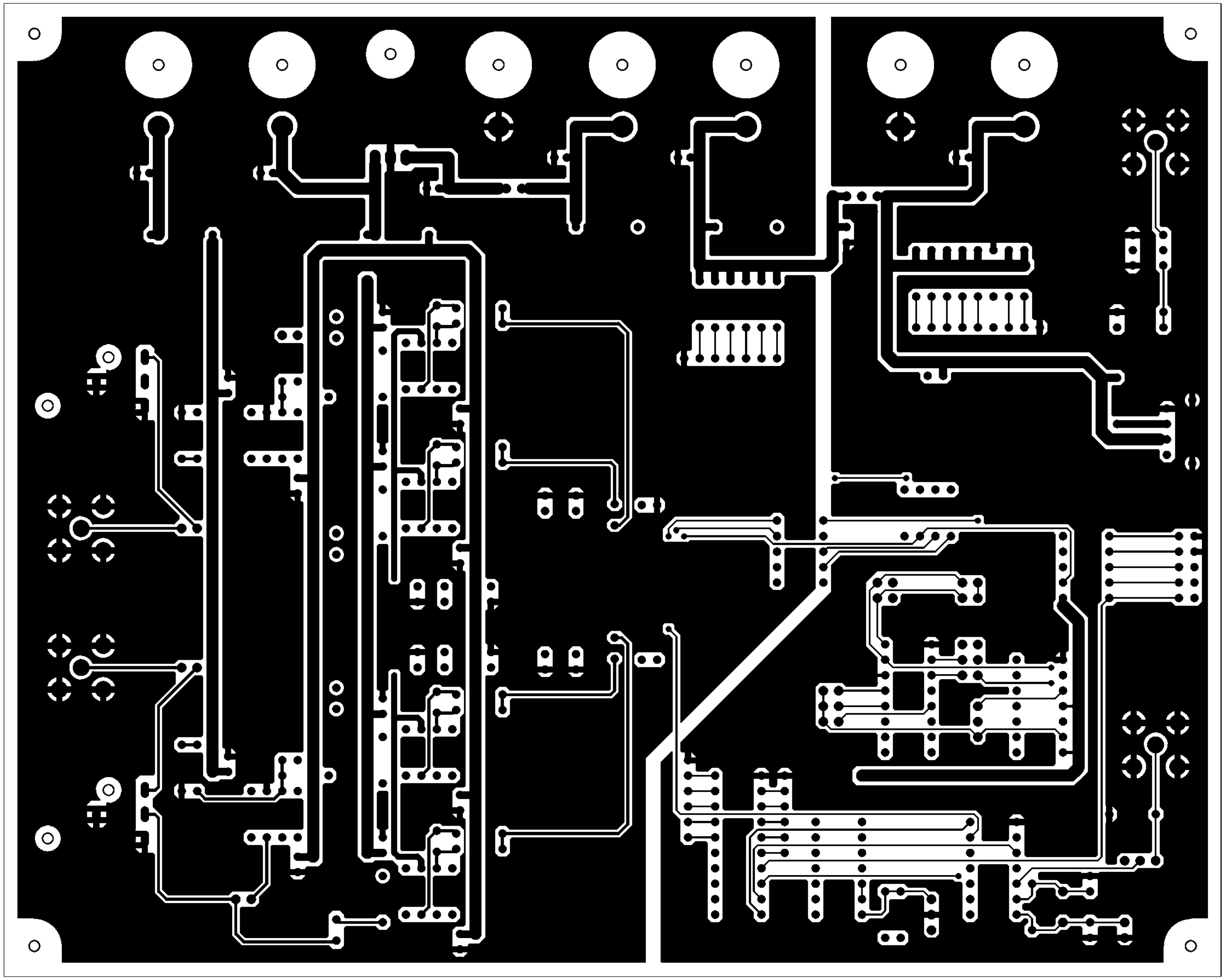

AKD5394 Rev.B L2