



AK7722

24bit 4ch ADC + 24bit 4ch DAC with Audio DSP

GENERAL DESCRIPTION

The AK7722 is a digital signal processor with an integrated 4ch 24bit DAC, a stereo ADC with input selector and a 2ch input ADC. The integrated 4ch DAC, the 2ch ADC with input selector and the other 2ch ADC feature high performance achieving 108dB, 96dB and 95dB, respectively. The integrated SRC has three input selector enabling the DSP to operate in master mode with digital inputs. The audio DSP has 1536step/fs (at 48kHz sampling) parallel arithmetic operation performance and the 5k-word delay RAM allows surround processing and time alignment adjusting. As the AK7722 is a RAM based DSP, it is programmable for various user requirements. It is housed in an 80pin LQFP package.

FEATURES

[DSP Block]

- Word length: 24bit (Coefficient RAM & Data RAM: F24 floating point)
- Processing Speed: 13.6 ns (1536step/fs; fs = 48kHz)
- Multiplication: 20 x 24 → 44-bit Double precision arithmetic available
- Divider 20 / 20 → 20bit
- ALU: 48bit arithmetic operation (overflow margin 4bit) 20bit floating point arithmetic and logic operation
- Program RAM: 3072 x 36bit
- Coefficient RAM: 2048 x 24bit (F24 floating point)
- Data RAM: 2048 x 24-bit (F24 floating point)
- Offset Register: 64 x 13bit
- Delay RAM1: 3072 x 24-bit
- Delay RAM2: 2048 x 24-bit
- Sampling rate: fs= 7.35k ~ 48kHz
- Master Clock: 1536fs
(generated from 32fs, 48fs, 64fs, 128fs, 256fs, 384fs by internal PLL)
- Master/Slave Operation

[ADC1 Block]

- Stereo with 6 Inputs Selector
- DR, S/N: 96dB (fs = 48kHz, when differential input)
- S/(N+D): 90dB (fs = 48kHz)
- Differential & Single-ended Inputs
- Digital HPF (fc=1Hz)
- 6 Analog Inputs Selector (2 differential, 4 single-ended)
- Digital Volume Control (24dB ~ -103dB, 0.5dB Step, Mute)

[ADC2 Block]

- DR, S/N: 95dB (fs = 48kHz)
- Single-ended Inputs
- Digital Volume Control (24dB ~ -103dB, 0.5dB Step, Mute)

[SRC Block]

- 3 Pair of Stereo → 1 Stereo Pair Selector
- 2ch x 1 system
- Supporting frequency: Fin = 7.35kHz ~ 96kHz → Fout = 7.35kHz ~ 48kHz
(FSO/FSI = 0.167~ 6.0)

[Guidance SRC Block] (GSRC)

- 1 Channel (24bit) Up-converter for Voice Guidance
- Supporting frequency: $F_{in} = 7.35\text{kHz} \sim 12\text{kHz} \rightarrow F_{out} = 44.1\text{kHz}$ or 48kHz

[DAC Block]

- 4ch (2 Stereos)
- 24bit 128 x Over-sampling advanced multi-bit ($f_s=8\text{kHz}\sim 48\text{kHz}$)
- DR, S/N: 108dB (Differential Output)
- S/(N+D): 90dB
- Digital Volume Control (12dB ~ -115dB, 0.5dB Step, Mute)

[Digital Interface Input/Output]

- Digital Signal Input Port (4ch):
24bit MSB justified, 24/20/16bit LSB justified and I²S Format
- Digital Signal Output Port (6ch):
24bit MSB justified, 24/16bit LSB justified and I²S Format

[Micro Computer Interface]

- I²C or 4-wired Interface

[General]

- Integrated PLL
- Integrated Regulator 3.3V \rightarrow 1.8V
- Power Supply: 3.3V \pm 0.3V
- Operating Temperature Range: -40°C ~ 85°C
- 80pin LQFP

■ Block Diagram

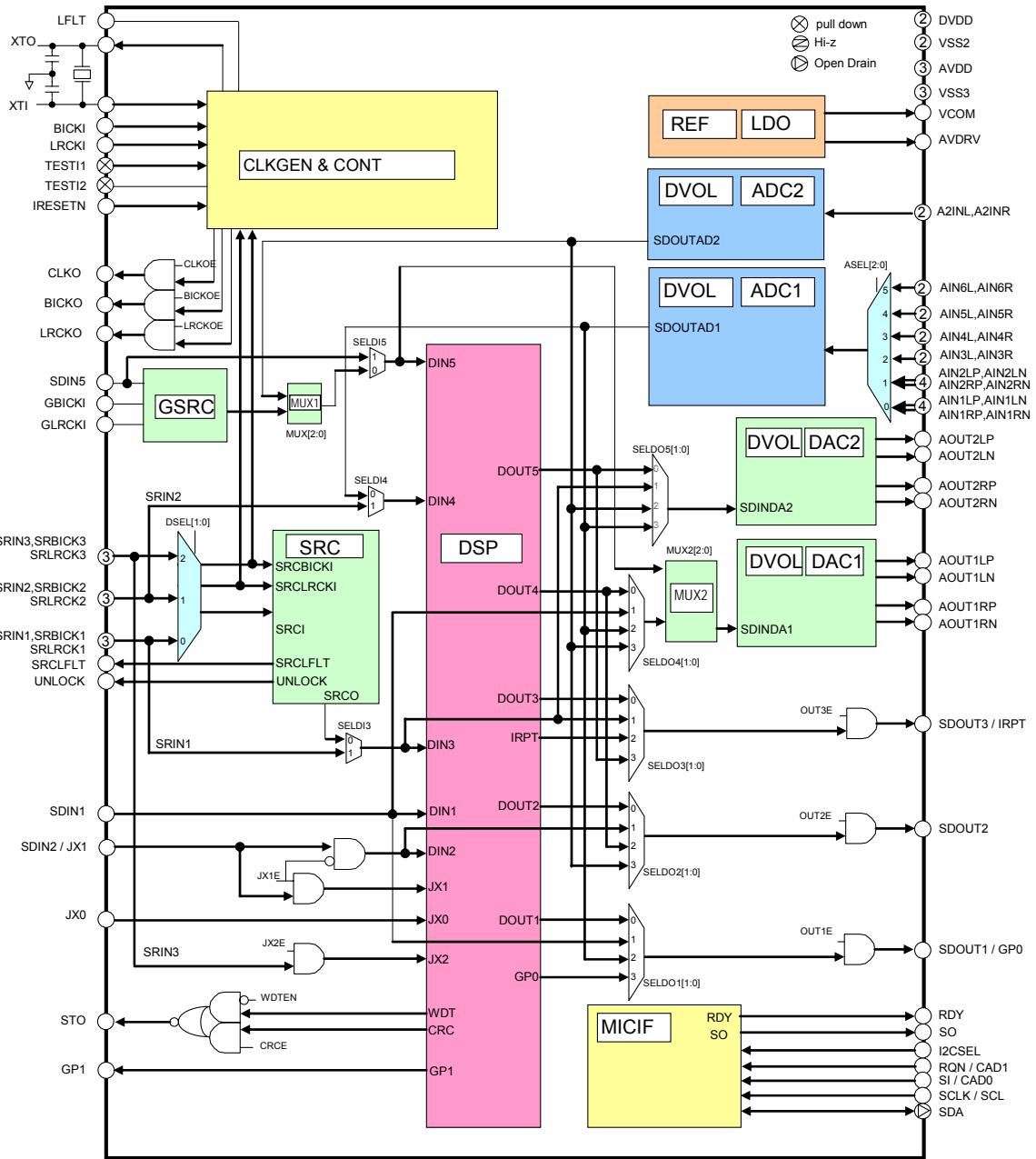


Figure 1. Block Diagram

* Figure 1 shows a simplified diagram of the AK7722, which is not the perfect same as the actual circuit diagram.

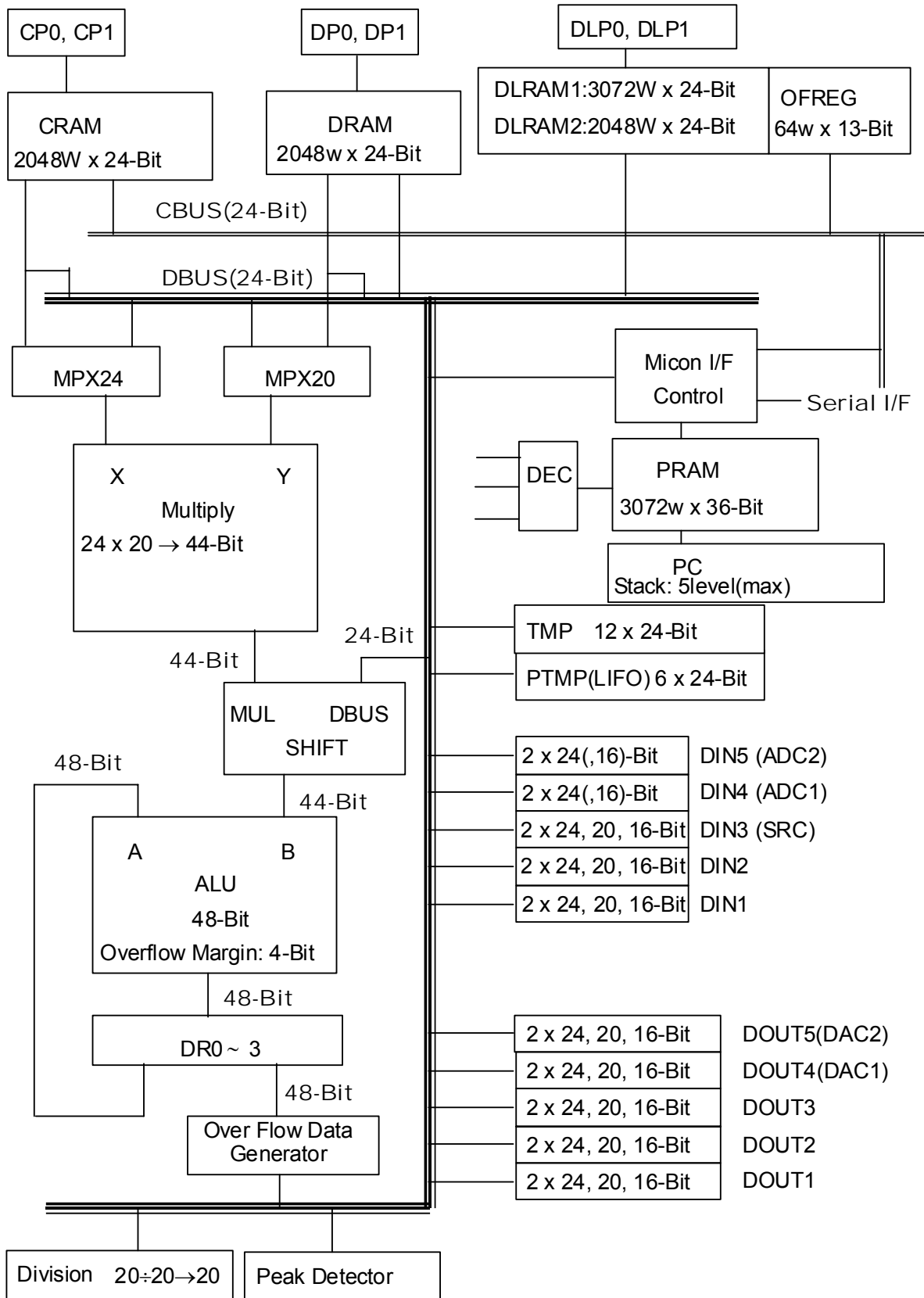


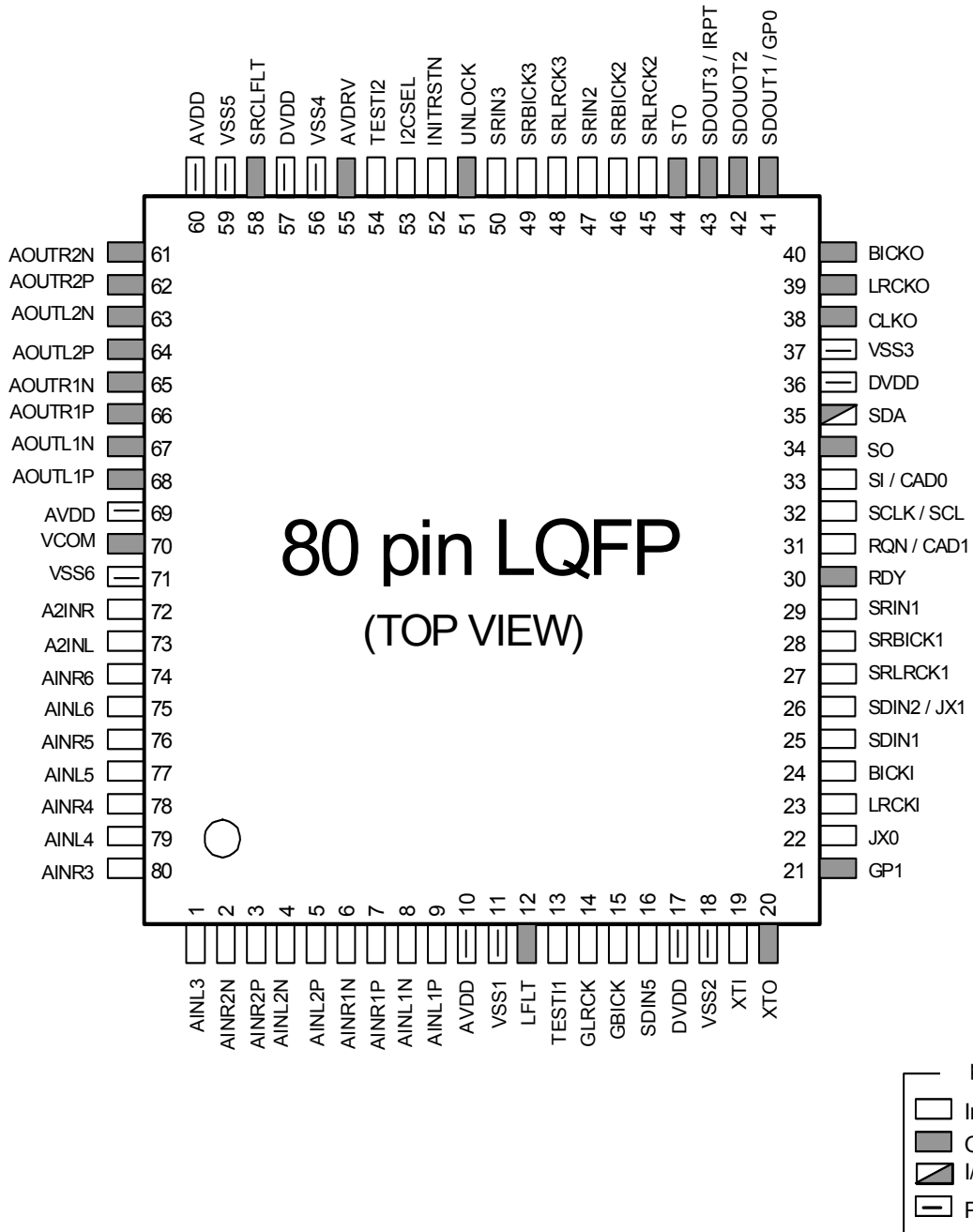
Figure 2. Main DSP Block Diagram of the AK7722

■ Ordering Guide

AK7722VQ
AKD7722

-40 ~ +85°C 80pin LQFP
Evaluation Board for AK7722

■ Pin Layout



PIN FUNCTION

| No. | Name | I/O | Function | Classification |
|-----|---------|-----|--|--------------------|
| 1 | AINL3 | I | ADC1 Lch Single-ended Input 3 Pin. | Analog Input |
| 2 | AINR2N | I | ADC1 Inverted Rch Differential Input 2 Pin | Analog Input |
| 3 | AINR2P | I | ADC1 Non-inverted Rch Differential Input 2 Pin | Analog Input |
| 4 | AINL2N | I | ADC1 Inverted Lch Differential Input 2 Pin | Analog Input |
| 5 | AINL2P | I | ADC1 Non-inverted Lch Differential Input 2 Pin | Analog Input |
| 6 | AINR1N | I | ADC1 Inverted Rch Differential Input 1 Pin | Analog Input |
| 7 | AINR1P | I | ADC1 Non-inverted Rch Differential Input 1 Pin | Analog Input |
| 8 | AINL1N | I | ADC1 Inverted Lch Differential Input 1 Pin | Analog Input |
| 9 | AINL1P | I | ADC1 Non-inverted Lch Differential Input 1 Pin | Analog Input |
| 10 | AVDD | - | Analog Power Supply Pin 3.0 ~ 3.6V | Power Supply |
| 11 | VSS1 | - | Analog Ground Pin 0V | Power Supply |
| 12 | LFLT | O | R and C Component Connect Pin for PLL Refer to “7. LFLT Pin External Connection”. This pin outputs “L” during initial reset. | Analog Output |
| 13 | TEST11 | I | Test 1 Pin (Internal pull-down) This pin must be connected to VSS. | Test |
| 14 | GLRCKI | I | Frame Clock Input Pin for Voice Guidance | Digital Input |
| 15 | GBICKI | I | Bit Clock Input Pin for Voice Guidance | Digital Input |
| 16 | SDIN5 | I | Serial Audio Input Pin for Voice Guidance | Digital Input |
| 17 | DVDD | - | Digital Power Supply Pin 3.0~3.6V | Power Supply |
| 18 | VSS2 | - | Ground Pin 0V | Power Supply |
| 19 | XTI | I | Crystal oscillator input pin Connect a crystal oscillator between this pin and the XTO pin, or input an external clock to the XTI pin. | Clock |
| 20 | XTO | O | Crystal Oscillator Output Pin When a crystal oscillator is used, connect it between XTI and XTO. When an external clock is used, leave this pin open. During initial reset, the output of this pin is not determinable. | Clock |
| 21 | GP1 | O | Programmable Bit Output Pin This pin outputs “L” during initial reset. | Digital Output |
| 22 | JX0 | I | Conditional Jump Pin0 The conditional jump pin (JX0) is valid by setting control register (JX0E) to “1”. | Conditional Input |
| 23 | LRCKI | I | LR Channel Select Clock Pin 1 LR clock should be input to this pin in slave mode. | System Clock Input |
| 24 | BICKI | I | Serial Bit Clock Input Pin 1 BITCLOCK (48fs or 64fs) should be input to this pin in slave mode. | System Clock Input |
| 25 | SDIN1 | I | Serial Data Input 1 Pin | Digital Input |
| 26 | SDIN2 | I | Serial Data Input 2 Pin | Digital Input |
| | JX1 | I | Conditional Jump Pin1 The conditional jump pin (JX1) is valid by setting control register (JX1E) to “1”. | Conditional Input |
| 27 | SRLRCK1 | I | LR Channel Select Clock Pin 1 (for SRC) | System Clock Input |
| 28 | SRBICK1 | I | Serial Bit Clock Input Pin 1 (for SRC) | System Clock Input |

| No. | Name | I/O | Function | Classification |
|-----|---------|-----|--|--------------------------|
| 29 | SRIN1 | I | Serial Data Input Pin 1 (for SRC) | Digital Input |
| | SDIN3 | I | Serial Data Input Pin 3 | |
| 30 | RDY | O | Data Write Ready Output Pin for Microprocessor Interface This pin outputs RDY, and outputs "H" during initial reset. | Microprocessor |
| 31 | RQN | I | Microprocessor Interface Write Request Pin (I2CSEL pin = "L") When initial reset state and Microcomputer interface are not in use, leave RQN pin = "H". | Interface |
| | CAD1 | I | I ² C Bus Address Setting Pin 1 (I2CSEL pin = "H") | I ² C |
| 32 | SCLK | I | Serial Data Clock Pin for Microprocessor Interface (I2CSEL pin = "L") When SCLK is not used, tie the SCLK pin = "H". | Microprocessor Interface |
| | SCL | I | I ² C Bus Data Clock Pin (I2CSEL pin = "H") | I ² C |
| 33 | SI | I | Serial Data Input Pin for Microprocessor Interface (I2CSEL pin = "L") When SI is not used, tie the SI pin = "L". | Microprocessor Interface |
| | CAD0 | I | I ² C Bus Address Setting Pin 0 (I2CSEL pin = "H") | I ² C |
| 34 | SO | O | Serial Data Output Pin for Microprocessor Interface Outputs "L" during initial reset. | Microprocessor Interface |
| 35 | SDA | O | I2CSEL pin = "L" Leave this pin Open. SDA outputs "L". | Open |
| | | I/O | I ² C Bus Data Clock Pin (I2CSEL pin = "H") Outputs "Hi-z" during initial reset. | I ² C |
| 36 | DVDD | - | Digital Power Supply Pin 3.0~3.6V | Power Supply |
| 37 | VSS3 | - | Ground Pin 0V | Power Supply |
| 38 | CLKO | O | Clock Output Pin This pin outputs "L" during initial reset. | Clock Output |
| 39 | LRCKO | O | LR Channel Select Output Pin This pin outputs "L" during initial reset in master mode. | System Clock Output |
| 40 | BICKO | O | Serial Bit Clock Output Pin This pin outputs "L" during initial reset in master mode. | System Clock Output |
| 41 | SDOUT1 | O | Serial Data Output1 Pin This pin outputs "L" during initial reset. | Digital Output |
| | GP0 | O | Programmable Bit Output Pin | Digital Output |
| 42 | SDOUT2 | O | Serial Data Output2 Pin This pin outputs "L" during initial reset. | Digital Output |
| 43 | SDOUT3 | O | Serial Data Output3 Pin This pin outputs "L" during initial reset. | Digital Output |
| | IRPT | O | Interrupt Status Output Pin | Digital Output |
| 44 | STO | O | Status Output Pin This pin outputs "H" during initial reset. | Status |
| 45 | SRLRCK2 | I | LR Channel Select Clock Pin 2 (for SRC) | System Clock Input |
| 46 | SRBICK2 | I | Serial Bit Clock Input Pin 2 (for SRC) | System Clock Input |
| 47 | SRIN2 | I | Serial Data Input Pin 2 (for SRC) | Digital Input |
| | SDIN4 | I | Serial Data Input Pin 4 | |
| 48 | SRLRCK3 | I | LR Channel Select Clock Pin 3 (for SRC) | System Clock Input |

| No. | Name | I/O | Function | Classification |
|-----|----------|-----|---|-------------------------|
| 49 | SRBICK3 | I | Serial Bit Clock Input Pin 3 (for SRC) | System Clock Input |
| 50 | SRIN3 | I | Serial Data Input Pin 3 (for SRC) | Digital Input |
| | JX2 | I | Conditional Jump Pin2 The conditional jump pin (JX2) is valid by setting control register (JX2E) to "1". | Conditional Input |
| 51 | UNLOCK | O | SRC UNLOCK State Output Pin This pin outputs "H" during initial reset. | SRC Status |
| 52 | INITRSTN | I | Reset Pin (for Initialization) Use to initialize the AK7722. Set this pin to "L" when power-up the AK7722. | System |
| 53 | I2CSEL | I | I ² C BUS Select Pin (Internal pull-down) I2CSEL pin = "L": 4-wired Interface I2CSEL pin = "H": I2C Bus selected mode. SCL and SDA are active. I2CSEL should be connected to "L" (VSS) or "H" (DVDD). | I ² C Select |
| 54 | TESTI2 | I | Test Input 2 Pin (Internal pull-down) This pin must be connected to VSS4. | Test |
| 55 | AVDRV | O | AVDRV Pin Connect a 1μF capacitor between this pin and VSS4 pin. No external circuits should be connected to this pin. This pin outputs "L" during initial reset. | Analog Output |
| 56 | VSS4 | - | Ground Pin 0V | Power Supply |
| 57 | DVDD | - | Digital Power Supply Pin 3.0~3.6V | Power Supply |
| 58 | SRCLFLT | O | Capacitor Connect Pin for SRCPLL Connect a 1μF capacitor between this pin and VSS4 pin. This pin outputs "L" during initial reset. | Analog Output |
| 59 | VSS5 | - | Ground Pin 0V | Power Supply |
| 60 | AVDD | - | Analog Power Supply Pin 3.0~3.6V | Power Supply |
| 61 | AOUTR2N | O | DAC2 Inverted Rch Differential Analog Output Pin "Hi-Z" output during initial reset | Analog Output |
| 62 | AOUTR2P | O | DAC2 Non-inverted Rch Differential Analog Output Pin "Hi-Z" output during initial reset | Analog Output |
| 63 | AOUTL2N | O | DAC2 Inverted Lch Differential Analog Output Pin "Hi-Z" output during initial reset | Analog Output |
| 64 | AOUTL2P | O | DAC2 Non-inverted Lch Differential Analog Output Pin "Hi-Z" output during initial reset | Analog Output |
| 65 | AOUTR1N | O | DAC1 Inverted Rch Differential Analog Output Pin "Hi-Z" output during initial reset | Analog Output |
| 66 | AOUTR1P | O | DAC1 Non-inverted Rch Differential Analog Output Pin "Hi-Z" output during initial reset | Analog Output |
| 67 | AOUTL1N | O | DAC1 Inverted Lch Differential Analog Output Pin "Hi-Z" output during initial reset | Analog Output |
| 68 | AOUTL1P | O | DAC1 Non-inverted Lch Differential Analog Output Pin "Hi-Z" output during initial reset | Analog Output |
| 69 | AVDD | - | Analog Power Supply Pin 3.0~3.6V | Power Supply |
| 70 | VCOM | O | Analog Common Voltage Output pin Connect 0.1μF and 2.2μF capacitors between this pin and the VSS6 pin. No external circuits should be connected to this pin. This pin outputs "L" during initial reset. | Analog Output |

| No. | Name | I/O | Function | Classification |
|-----|-------|-----|-----------------------------------|----------------|
| 71 | VSS6 | - | Ground Pin 0V | Power Supply |
| 72 | A2INR | I | ADC2 Rch Single-ended Input Pin | Analog Input |
| 73 | A2INL | I | ADC2 Lch Single-ended Input Pin | Analog Input |
| 74 | AINR6 | I | ADC1 Rch Single-ended Input Pin 6 | Analog Input |
| 75 | AINL6 | I | ADC1 Lch Single-ended Input Pin 6 | Analog Input |
| 76 | AINR5 | I | ADC1 Rch Single-ended Input Pin 5 | Analog Input |
| 77 | AINL5 | I | ADC1 Lch Single-ended Input Pin 5 | Analog Input |
| 78 | AINR4 | I | ADC1 Rch Single-ended Input Pin 4 | Analog Input |
| 79 | AINL4 | I | ADC1 Lch Single-ended Input Pin 4 | Analog Input |
| 80 | AINR3 | I | ADC1 Rch Single-ended Input Pin 3 | Analog Input |

■ Handling of Unused Pin

The following table illustrates recommended states for open pins:

| Classification | Pin Name | Setting |
|----------------|---|----------------|
| Analog | ANL1P, AINL1N, AINR1P, AINR1N, AINL2P, AINL2N, AINR2P, AINR2N, AINL3, AINR3, AINL4, AINR4, AINL5, AINR5, AINL6, AINR6 AOUTL1P, AOUTL1N, AOUTR1P, AOUTR1N AOUTL2P, AOUTL2N, AOUTR2P, AOUTR2N | Leave Open |
| Digital | XTO, GP1, RDY, SO, SDA(I2CSEL=“L”), CLKO, LRCKO, BICKO, SDOUT1, SDOUT2, SDOUT3, STO, UNLOCK | Leave Open |
| | TESTI1, GLRCK, GBICK, SDIN5, XTI, JX0, LRCKI, BICKI, SDIN1, SDIN2, SRLRCK1, SRBICK1, SRIN1, RQN, SI, SRLRCK2, SRBICK2, SRIN2, SRLRCK3, SRBICK3, SRIN3, TESTI2 | Connect to VSS |

The relationship between the I2CSEL pin and SDA pin

| | I2CSEL | INTRSTN | SDA |
|------------------------------|--------|---------|----------|
| Micro controller Interface | L | L | L |
| | L | H | L |
| I ² C-bus support | H | L | “Hi-Z” |
| | H | H | function |

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|---------------------------------|
| ABSOLUTE MAXIMUM RATINGS |
|---------------------------------|

(VSS1~VSS6=0V: [Note 1](#))

| Parameter | Symbol | min | max | Unit |
|--|--------|------|----------|------|
| Power Supply Voltage | | | | |
| Analog | AVDD | -0.3 | 4.3 | V |
| Digital | DVDD | -0.3 | 4.3 | V |
| Input Current (except for power supply pin) | IIN | – | ±10 | mA |
| Analog Input Voltage | VINA | -0.3 | AVDD+0.3 | V |
| Digital Input Voltage | VIND | -0.3 | DVDD+0.3 | V |
| Operating Ambient Temperature | Ta | -40 | 85 | °C |
| Storage Temperature | Tstg | -65 | 150 | °C |

Note 1. All indicated voltages are with respect to ground.

Note 2. VSS1-6 must be connected to the same ground plane.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.

Normal operation is not guaranteed at these extremes.

| |
|---|
| RECOMMENDED OPERATING CONDITIONS |
|---|

(VSS1~VSS6=0V: [Note 1](#))

| Parameter | Symbol | min | typ | max | Unit |
|----------------------|--------|-----|-----|-----|------|
| Power Supply Voltage | | | | | |
| Analog | AVDD | 3.0 | 3.3 | 3.6 | V |
| Digital | DVDD | 3.0 | 3.3 | 3.6 | V |

Note 3. The power supply sequence for AVDD and DVDD is not critical but all power supplies must be On before start operating the AK7722.

Note 4. Do not turn off the power supply of the AK7722 with the power supply of the surrounding device turned on.

DVDD must not exceed the pull-up of SDA and SCL of I2C BUS. (The diode exists for DVDD in the SDA and SCL pins.)

WARNING: AKM assumes no responsibility for the usage beyond the conditions in the datasheet.

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| ANALOG CHARACTERISTICS (CODEC) |
|---------------------------------------|

■ ADC Characteristics

1. ADC1

(Ta=25°C; AVDD=DVDD=3.3V, BITCLK=64fs; Signal frequency 1kHz; Measurement frequency = 20Hz~20kHz @fs=48kHz; CKM mode0 (CKM[2:0]=000); BITFS[1:0]=00(64fs); with Differential Input; in SRC reset, Unless otherwise specified.)

| Parameter | | min | typ | max | Unit | |
|-------------|---|-------|-------|-------|------|--|
| ADC Section | Resolution | 24 | | | Bits | |
| | Dynamic Characteristics | | | | | |
| | S/(N+D) (-1dBFS) | 82 | 90 | | dB | |
| | Dynamic Range (A-weighted) (Note 5) | 88 | 96 | | dB | |
| | S/N (A-weighted) | 88 | 96 | | dB | |
| | Inter-Channel Isolation (fin=1kHz) (Note 6) | 90 | 110 | | dB | |
| | DC accuracy | | | | | |
| | Channel Gain Mismatch | | 0.0 | 0.3 | dB | |
| | Analog Input | | | | | |
| | Input Voltage (Differential) (Note 7) | ±2.00 | ±2.20 | ±2.40 | Vp-p | |
| | Input Voltage (Single-ended) (Note 8) | 2.00 | 2.20 | 2.40 | Vp-p | |
| | Input Impedance | 41 | 62 | | kΩ | |

Note 5. S/(N+D) when -60dB FS signal is applied.

Note 6. Inter-channel isolation between AINR and AINL with -1dB FS signal input.

Note 7. AINL1P, AINL1N, AINR1P, AINR1N, AINL2P, AINL2N, AINR2P and AINR2N pins

Note 8. AINL3, AINR3, AINL4, AINR4, AINL5, AINR5, AINL6 and AINR6 pins.

Full scale output voltage is FS=AVDD×2.2/3.3.

2. ADC2

(Ta=25°C; AVDD=DVDD=3.3V, BITCLK=64fs; Signal frequency 1kHz; Measurement frequency =20Hz~20kHz @fs=48kHz; CKM mode0 (CKM[2:0]=000); BITFS[1:0]=00(64fs); in SRC reset, Unless otherwise specified.)

| Parameter | | min | typ | max | Unit | |
|-------------|--|------|------|------|------|--|
| ADC Section | Resolution | 24 | | | Bits | |
| | Dynamic Characteristics | | | | | |
| | S/(N+D) (-1dBFS) | 80 | 88 | | dB | |
| | Dynamic Range (A-weighted) (Note 9) | 87 | 95 | | dB | |
| | S/N (A-weighted) | 87 | 95 | | dB | |
| | Inter-Channel Isolation (fin=1kHz) (Note 10) | 90 | 110 | | dB | |
| | DC accuracy | | | | | |
| | Channel Gain Mismatch | | 0.1 | 0.3 | dB | |
| | Analog Input | | | | | |
| | Input Voltage (Note 11) | 2.00 | 2.20 | 2.40 | Vp-p | |
| | Input Impedance | 41 | 62 | | kΩ | |

Note 9. S/(N+D) when -60dB FS signal is applied.

Note 10. Inter-channel isolation between AINR and AINL with -1dB FS signal input.

Note 11. Full scale output voltage is FS=AVDD×2.2/3.3.

■ DAC1/2 Characteristics

(Ta=25°C; AVDD=DVDD=3.3V; VSS1~VSS6=0V; Signal frequency 1kHz; Measurement frequency =20Hz~20kHz @fs=48kHz; CKM[2:0]=000, BITFS[1:0]=00, in SRC Reset) Unless otherwise specified.)

| Parameter | min | typ | max | Unit |
|--|------------|------|------|------|
| DAC1 DAC2 | Resolution | | 24 | Bits |
| Dynamic Characteristics | | | | |
| S/(N+D) (0 dBFS) | 82 | 90 | | dB |
| Dynamic Range (A-weighted) (Note 12) | 98 | 108 | | dB |
| S/N (A-weighted) | 98 | 108 | | dB |
| Inter-channel Isolation (f=1kHz) (Note 13) | 90 | 110 | | dB |
| DC accuracy | | | | |
| Channel Gain Mismatch | | 0.0 | 0.5 | dB |
| Analog output | | | | |
| Output Voltage (Note 14) | 3.78 | 4.16 | 4.53 | Vp-p |
| Load Resistance | 5 | | | kΩ |
| Load Capacitance | | | 30 | pF |

Note 12. S/(N+D) when -60dBFS signal is applied.

Note 13. Indicates isolation between each DAC's of Lch and Rch when -1dBFS signal is applied.

Note 14. Full scale differential output voltage.

SRC CHARACTERISTICS

(Ta=25°C; AVDD = DVDD=3.3V; VSS1~VSS6=0V, data = 24bit; measurement bandwidth = 20Hz~ FSO/2; unless otherwise specified.)

| Parameter | Symbol | min | typ | max | Unit |
|--|---------|-------|------|------|------|
| Resolution | | | | 24 | Bits |
| Input Sample Rate | FSI | 7.35 | | 96 | kHz |
| Output Sample Rate | FSO | 7.35 | | 48 | kHz |
| THD+N (Input= 1kHz, 0dBFS) | | | | | |
| FSO/FSI=44.1kHz/48kHz | | | -112 | | dB |
| FSO/FSI=44.1kHz/96kHz | | | -104 | | dB |
| FSO/FSI=48kHz/44.1kHz | | | -112 | | dB |
| FSO/FSI=48kHz/96kHz | | | -112 | | dB |
| FSO/FSI=48kHz/8kHz | | | -111 | -103 | dB |
| FSO/FSI=8kHz/48kHz | | | -113 | | dB |
| FSO/FSI=8kHz/44.1kHz | | | -100 | | dB |
| Dynamic Range (Input= 1kHz, -60dBFS) | | | | | |
| FSO/FSI=44.1kHz/48kHz | | | 113 | | dB |
| FSO/FSI=44.1kHz/96kHz | | | 113 | | dB |
| FSO/FSI=48kHz/44.1kHz | | | 113 | | dB |
| FSO/FSI=48kHz/96kHz | | | 113 | | dB |
| FSO/FSI=48kHz/8kHz | | 109 | 112 | | dB |
| FSO/FSI=8kHz/48kHz | | | 113 | | dB |
| FSO/FSI=8kHz/44.1kHz | | | 113 | | dB |
| Dynamic Range (Input= 1kHz, -60dBFS, A-weighted) | | | | | |
| FSO/FSI=44.1kHz/48kHz | | | 115 | | dB |
| Ratio between Input and Output Sample Rate | FSO/FSI | 0.167 | | 6 | - |

DC CHARACTERISTICS

(Ta=-40°C~85°C; AVDD=DVDD=3.0~3.6V)

| Parameter | Symbol | min | typ | max | Unit |
|---|--------|----------|-----|---------|------|
| High Level Input Voltage (Note 15) | VIH | 80%DVDD | | | V |
| Low Level Input Voltage (Note 15) | VIL | | | 20%DVDD | V |
| SCL,SDA High Level Input Voltage | VIH | 70%DVDD | | | V |
| SCL,SDA Low Level Input Voltage | VIL | | | 30%DVDD | V |
| High Level Output Voltage Iout=-100μA | VOH | DVDD-0.5 | | | V |
| Low Level Output Voltage Iout=100μA (Note 16) | VOL | | | 0.5 | V |
| SDA Low Level Output Voltage Iout=3mA | VOL | | | 0.4 | V |
| Input Leak Current (Note 17) | Iin | | | ±10 | μA |
| Input Leak Current (pull-down pin) (Note 18) | Iid | | 22 | | μA |
| Input Leak Current (XTI pin) | Iix | | 26 | | μA |

Note 15. SCL and SDA pins are not included. (SCLK pins are included)

Note 16. The SDA pin is not included.

Note 17. Pull-down pins, and the XTI pin is not included.

Note 18. TESTI1 and TESTI2 pins are internal pulled-down pin. (Typ150kΩ)

POWER CONSUMPTION

(Ta=25°C; AVDD=DVDD=3.0~3.6V (when typ=3.3V, max=3.6V))

| Parameter | min | typ | max | Unit |
|--|-----|-----|-----|------|
| Power Supply Current (Note 19) | | | | |
| AVDD | | 55 | | mA |
| DVDD | | 65 | | mA |
| AVDD+DVDD | | 120 | 180 | mA |
| INISTRSTN pin= "L" (reference) (Note 20) | | 2 | | mA |

Note 19. The current of DVDD changes depending on the system frequency and contents of the DSP program.

Note 20. This is a reference value when using a crystal oscillator. Since most of the current are applied to the oscillator section in the initial reset state, the value may vary according to the crystal type and the external circuit. This is a "reference data" only.

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| DIGITAL FILTER CHARACTERISTICS |
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■ ADC Block (ADC1/2)

1. fs=48kHz

(Ta=-40°C ~85°C, AVDD=DVDD=3.0~3.6V, fs=48kHz, [Note 21](#))

| Parameter | Symbol | min | typ | max | Unit |
|--|--------|-----|-----|-------|------|
| Passband (±0.1dB) (Note 22) (-1.0dB) (-3.0dB) | PB | 0 | | 18.9 | kHz |
| | | | | 20.0 | kHz |
| | | | | 23.0 | kHz |
| Stopband | SB | 28 | | | kHz |
| Passband Ripple (Note 22) | PR | | | ±0.04 | dB |
| Stopband Attenuation (Note 23 , Note 24) | SA | 68 | | | dB |
| Group Delay Distortion | ΔGD | | 0 | | μs |
| Group Delay (Ts=1/fs) | GD | | 16 | | Ts |

Note 21. The passband and stopband frequencies are proportional to fs (system sampling rate). High-pass filter characteristics are not included.

Note 22. The passband is from DC to 18.9kHz when fs=48kHz.

Note 23. The stopband is 28kHz to 3.044MHz when fs=48kHz.

Note 24. When fs = 48kHz, the analog modulator samples the input signal at 512kHz. There is no attenuation of an input signal in band (n x 3.072MHz ±28kHz; n=0, 1, 2, 3...) of integer times of the sampling frequency by the digital filter.

■ DAC1-2

(Ta=-40 °C ~85 °C; AVDD=DVDD=3.0~3.6V; fs=48kHz)

| Parameter | Symbol | min | typ | max | Unit |
|--|--------|------|------|-------|------|
| Passband (±0.05dB) (Note 25) (-6.0dB) | PB | 0 | | 21.7 | kHz |
| | | | | 24 | kHz |
| Stopband (Note 25) | SB | 26.2 | | | kHz |
| Passband Ripple | PR | | | ±0.01 | dB |
| Stopband Attenuation | SA | 64 | | | dB |
| Group Delay (Ts=1/fs) (Note 26) | GD | | 24 | | Ts |
| Digital Filter + Analog Filter | | | | | |
| Amplitude Characteristics 20Hz~20.0kHz | | | ±0.5 | | dB |

Note 25. The pass band and stop band frequencies are proportional to “fs” (system sampling rate), and represents PB=0.4535fs (@±0.05dB) and SB=0.5465fs, respectively.

Note 26. The digital filter delay is calculated as the time from setting data into the input register until an analog signal is output.

■ SRC

(Ta=-40°C ~85°C; AVDD=DVDD=3.0~3.6V)

| Parameter | | Symbol | min | typ | max | Unit |
|-----------------------|---------------------------------|--------|-----------|-----|-----------|------|
| Passband | $0.980 \leq FSO/FSI \leq 6.000$ | PB | 0 | | 0.4583FSI | kHz |
| | $0.900 \leq FSO/FSI < 0.990$ | PB | 0 | | 0.4167FSI | |
| | $0.450 \leq FSO/FSI < 0.910$ | PB | 0 | | 0.2177FSI | |
| | $0.225 \leq FSO/FSI < 0.455$ | PB | 0 | | 0.0917FSI | |
| | $0.167 \leq FSO/FSI < 0.227$ | PB | 0 | | 0.0917FSI | |
| Stopband | $0.980 \leq FSO/FSI \leq 6.000$ | SB | 0.5417FSI | | | kHz |
| | $0.900 \leq FSO/FSI < 0.990$ | SB | 0.5021FSI | | | |
| | $0.450 \leq FSO/FSI < 0.910$ | SB | 0.2813FSI | | | |
| | $0.225 \leq FSO/FSI < 0.455$ | SB | 0.1573FSI | | | |
| | $0.167 \leq FSO/FSI < 0.227$ | SB | 0.1354FSI | | | |
| Passband Ripple | $0.225 \leq FSO/FSI < 0.455$ | PR | | | ±0.0100 | dB |
| | $0.167 \leq FSO/FSI < 0.227$ | PR | | | ±0.0612 | |
| Stopband Attenuation | | SA | 92.3 | | | dB |
| Group Delay (Ts=1/fs) | (Note 27) | GD | | 56 | | Ts |

Note 27. This delay is the a period from the rising edge of SRLRCKn, just after the data is input, to the rising edge of LRCLKO, just after the data is output, when there is no phase difference between SRLRCKn and LRCLKO.

| |
|----------------------------------|
| SWITCHING CHARACTERISTICS |
|----------------------------------|

■ System Clock

(Ta=-40°C~85°C; AVDD=DVDD=3.0~3.6V, VSS1~VSS6=0V)

| Parameter | Symbol | min | typ | max | Unit |
|--|--------|------|-------------------|------|------|
| XTI CKM[2:0]=000, 001, 010 | | | | | |
| a) with a Crystal Oscillator: | | | | | |
| CKM[2:0]=000 fs=44.1kHz fs=48kHz | fXTI | - | 11.2896 12.288 | - | MHz |
| CKM[2:0]=001 fs=44.1kHz fs=48kHz | fXTI | - | 16.9344 18.432 | - | MHz |
| b) with an External Clock | | | | | |
| Duty Cycle | | 40 | 50 | 60 | % |
| CKM[2:0]=000, 010 fs=44.1kHz fs=48kHz | fXTI | 11.0 | 11.2896 12.288 | 12.4 | MHz |
| CKM[2:0]=001 fs=44.1kHz fs=48kHz | fXTI | 16.5 | 16.9344 18.432 | 18.6 | MHz |
| LRCKI Frequency (Note 28) | fs | 7.35 | | 48 | kHz |
| BICKI Frequency | | | | | |
| High Level Width | tBCLKH | 64 | | | ns |
| Low Level Width | tBCLKL | 64 | | | ns |
| Frequency | fBCLK | 0.23 | 3.072 | 3.1 | MHz |

Note 28. LRCKI frequency and sampling rate (fs) should be the same.

Note 29. When BICKI is the source of master clock, it should be synchronized to LRCKI and the frequency is stable.

■ SRC Input Clock

(Ta=-40°C~85°C; AVDD=DVDD=3.0~3.6V; VSS1~VSS6=0V)

| Parameter | Symbol | min | typ | max | Unit |
|-------------------|--------|------|-------|-------|------|
| SRLRCKn Frequency | fs | 7.35 | | 96 | kHz |
| SRBICKn Frequency | | | | | |
| Frequency | fBCLK | 0.23 | 3.072 | 6.144 | MHz |
| High Level Width | tBCLKH | 32 | | | ns |
| Low Level Width | tBCLKL | 32 | | | ns |

■ GSRC Input Clock

(Ta=-40 °C ~85 °C; AVDD=DVDD=3.0~3.6V; VSS1~VSS6=0V)

| Parameter | Symbol | min | typ | max | Unit |
|------------------|--------|------|-----|-----|------|
| GLRCK Frequency | fs | 7.35 | | 12 | kHz |
| GBICK Frequency | | | | | |
| Frequency | fBCLK | 230 | 512 | 780 | kHz |
| High Level Width | tBCLKH | 100 | | | ns |
| Low Level Width | tBCLKL | 100 | | | ns |

■ Reset

(Ta=-40°C~85°C; AVDD=DVDD=3.0~3.6V)

| Parameter | Symbol | min | typ | max | Unit |
|-------------------|--------|-----|-----|-----|------|
| INIRSTN (Note 30) | tRST | 600 | | | ns |

Note 30. It must be "L" when power-up the AK7722.

■ Audio Interface (SDIN1-2, SRIN1-3, SDOUT1-3)

(Ta=-40°C~85°C; AVDD=DVDD=3.0~3.6V, CL=20pF)

| Parameter | Symbol | min | typ | max | Unit |
|---|--------|-----|-----|-----|------|
| DSP Section Input SDIN1-2, SRIN1-3 (Note 31) | | | | | |
| Delay Time from BICKI “↑” to LRCKI (Note 32) | tBLRD | 20 | | | ns |
| Delay Time from LRCKI to BICKI “↑” (Note 32) | tLRBD | 20 | | | ns |
| Serial Data Input Latch Setup Time | tBSIDS | 80 | | | ns |
| Serial Data Input Latch Hold Time | tBSIDH | 80 | | | ns |
| SRC Section Input SRIN1-3 (Note 33) | | | | | |
| Delay Time from SRBICK1-3 “↑” to SRLRCK1-3 (Note 34) | tBLRD | 20 | | | ns |
| Delay Time from SRLRCK1-3 to SRBICK1-3 “↑” (Note 34) | tLRBD | 20 | | | ns |
| Serial Data Input Latch Setup Time | tBSIDS | 40 | | | ns |
| Serial Data Input Latch Hold Time | tBSIDH | 40 | | | ns |
| Output SDOUT1-3 (Note 31) | | | | | |
| BICKO Frequency | fBCLK | | 64 | | fs |
| BICKO Duty Factor | | | 50 | | % |
| Delay Time from BICKO “↓” to LRCKO (Note 35) | tBLRD | -20 | | 40 | ns |
| Delay Time from LRCKI to Serial Data Output (Note 36) | tLRD | | | 80 | ns |
| Delay Time from BICKI to Serial Data Output (Note 33) | tBSOD | | | 80 | ns |
| Delay Time from LRCKO to Serial Data Output (Note 36) | tLRD | | | 80 | ns |
| Delay Time from BICKO to Serial Data Output (Note 33) | tBSOD | | | 80 | ns |
| SDINn → SDOUTn (n=1-2) (Note 37) | | | | | |
| Delay Time from SDINn to SDOUTn Data Output | tIOD | | | 60 | ns |

Note 31. BICKI=SRBICKn (n=1, 2, 3) in CKM mode 4.

Note 32. BICKI edge must not occur at the same time as LRCKI edge. The BICKI polarity is inverted in PCM mode 0/2.

Note 33. Except CKM mode 4

Note 34. SRBICK1-3 edge must not occur at the same time as SRLRCK1-3 edge. When BIEDGE bit= “1”, this value is for SRBICK1-3 “↓” since SRBICK1-3 are polarity reversal.

Note 35. When SELBCK bit= “1”, this value is for BICKO “↑” since BICKO is polarity reversal.

Note 36. Except I²S.

Note 37. SDIN1 → SDOUT1: Control Register Setting, SELDO1[1:0]=1h, OUT1E bit= “1”

SDIN2/JX1 → SDOUT2: Control Register Setting, SELDO2[1:0]=1h, OUT2E bit= “1”

SRIN1/SDIN3 → SDOUT3: Control Register Setting, SELDI3 bit = “1”, SELDO3[1:0]=1h, OUT3E bit= “1”

■ Microprocessor Interface

(Ta=-40°C~85°C; AVDD=DVDD=3.0~3.6V; CL=20pF)

| Parameter | Symbol | min | typ | max | Unit |
|--|--------|-----|-----|-----|------|
| Microprocessor Interface Signal | | | | | |
| RQN Fall Time | tWRF | | | 30 | ns |
| RQN Rise Time | tWRR | | | 30 | ns |
| SCLK Fall Time | tSF | | | 30 | ns |
| SCLK Rise Time | tSR | | | 30 | ns |
| SCLK Frequency | fSCLK | | | 2.1 | MHz |
| SCLK Low Level Width | tSCLKL | 200 | | | ns |
| SCLK High Level Width | tSCLKH | 200 | | | ns |
| Microprocessor → AK7722 | | | | | |
| RQN High Level Width | tWRQH | 500 | | | ns |
| From RQN “↓” to SCLK “↓” | tWSC | 500 | | | ns |
| From SCLK “↑” to RQN “↑” | tSCW | 800 | | | ns |
| SI Latch Setup Time | tSIS | 200 | | | ns |
| SI Latch Hold Time | tSIH | 200 | | | ns |
| AK7722 → Microprocessor | | | | | |
| Delay Time from SCLK “↓” to SO Output | tSOS | | | 200 | ns |
| Hold Time from SCLK “↑” to SO Output (Note 38) | tSOH | 200 | | | ns |

Note 38. Except for, when writing to 8th bit of command code.

■ I²C BUS Interface

(Ta=-40°C~85°C; AVDD=DVDD=3.0~3.6V)

| Parameter | Symbol | min | typ | max | Unit |
|---|---------|-----|-----|-----|------|
| I²C Timing | | | | | |
| SCL clock frequency | fSCL | | | 400 | kHz |
| Bus Free Time Between Transmissions | tBUF | 1.3 | | | μs |
| Start Condition Hold Time (prior to first Clock pulse) | tHD:STA | 0.6 | | | μs |
| Clock Low Time | tLOW | 1.3 | | | μs |
| Clock High Time | tHIGH | 0.6 | | | μs |
| Setup Time for Repeated Start Condition | tSU:STA | 0.6 | | | μs |
| SDA Hold Time from SCL Falling | tHD:DAT | 0 | | 0.9 | μs |
| SDA Setup Time from SCL Rising | tSU:DAT | 0.1 | | | μs |
| Rise Time of Both SDA and SCL Lines | tR | | | 0.3 | μs |
| Fall Time of Both SDA and SCL Lines | tF | | | 0.3 | μs |
| Setup Time for Stop Condition | tSU:STO | 0.6 | | | μs |
| Pulse Width of Spike Noise Suppressed by Input Filter | tSP | 0 | | 50 | ns |
| Capacitive load on bus | Cb | | | 400 | pF |

Note 39. I²C-bus is a trademark of NXP B.V.

■ Timing Diagram

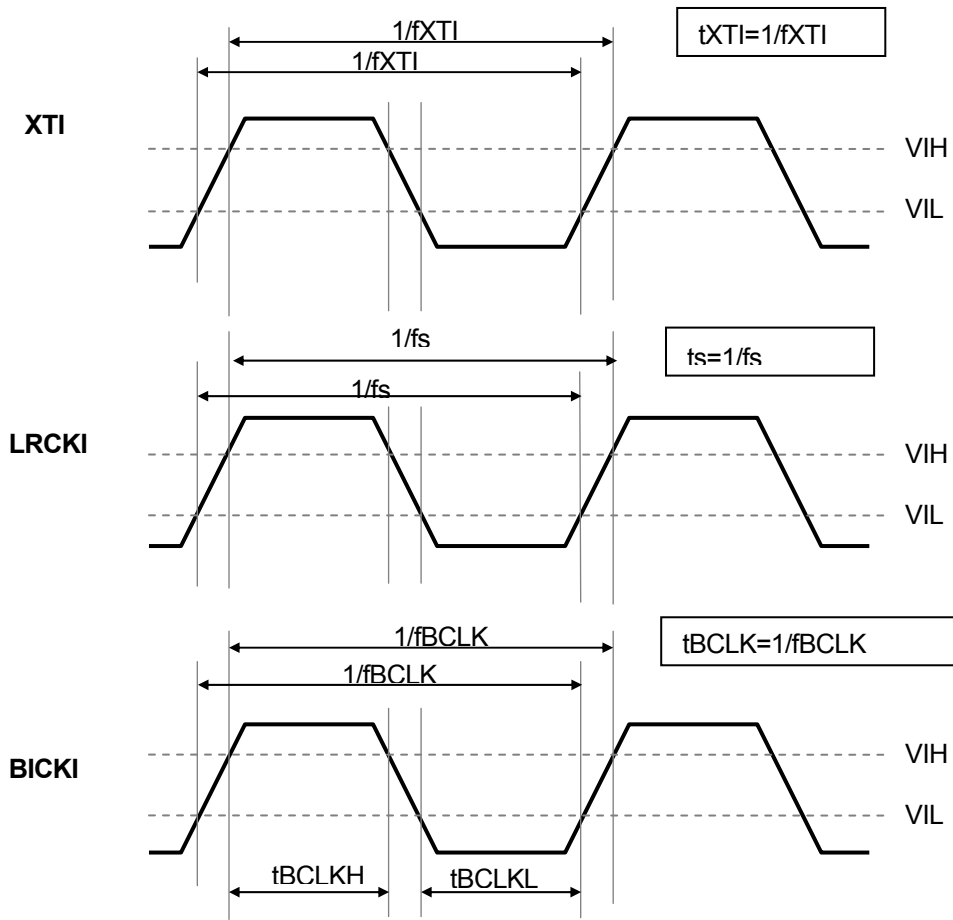


Figure 3. System Clock

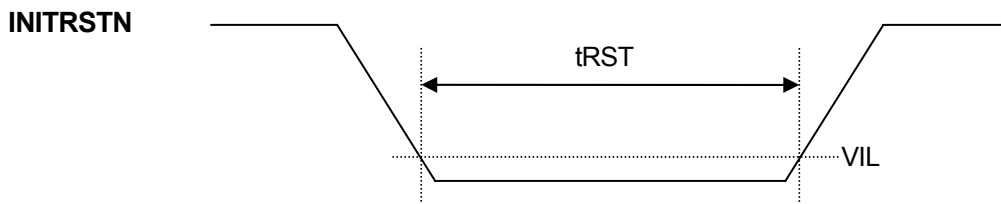


Figure 4. Reset

Note 40. The INTRSTN pin must be “L” when power-up/power-down the AK7722.

1) Audio Interface

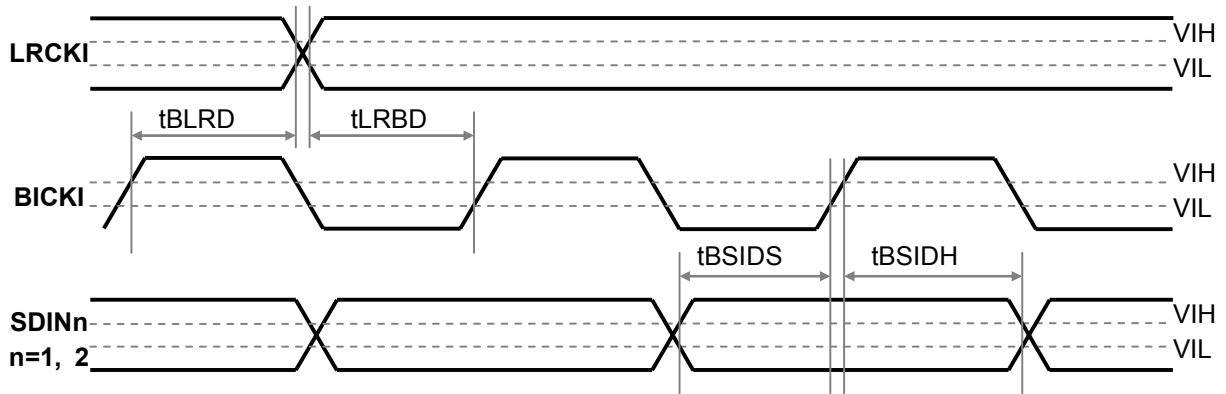


Figure 5. DSP Block Input Interface in Slave Mode

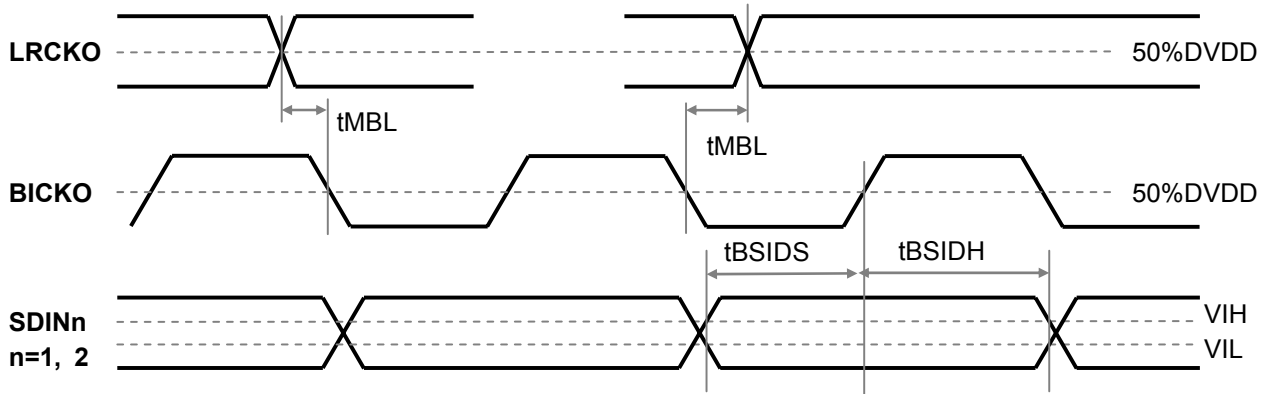


Figure 6. DSP Block Input Interface in Master Mode

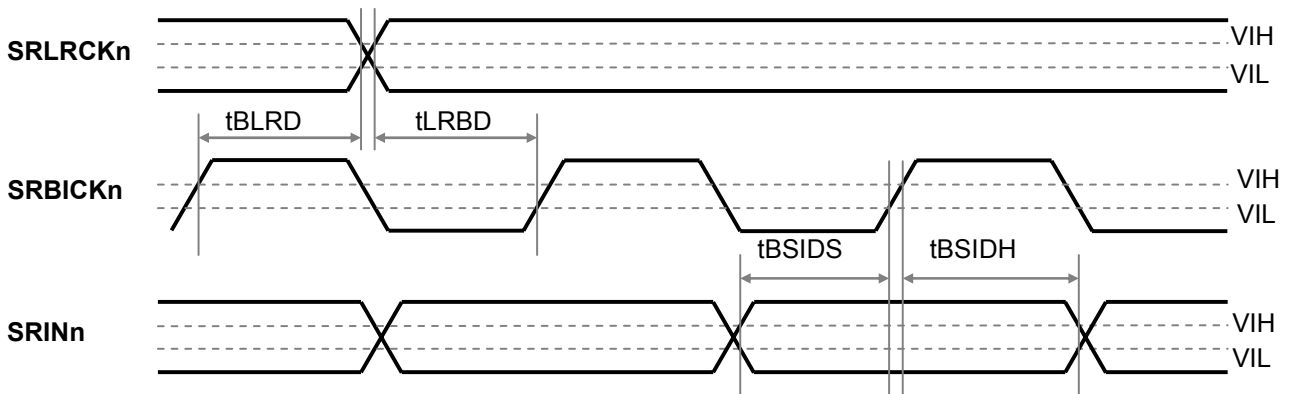


Figure 7. SRC Block Input Interface

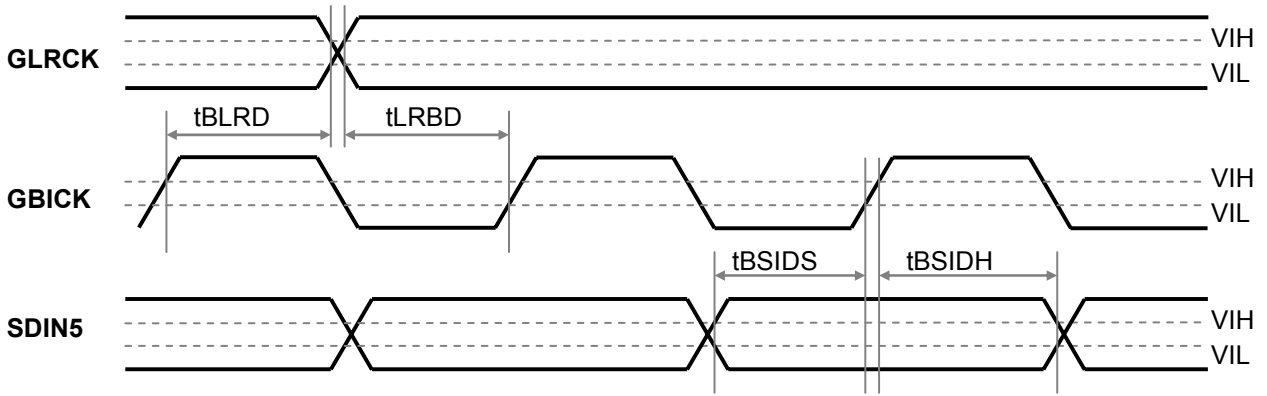


Figure 8. GSRC Block Input Interface

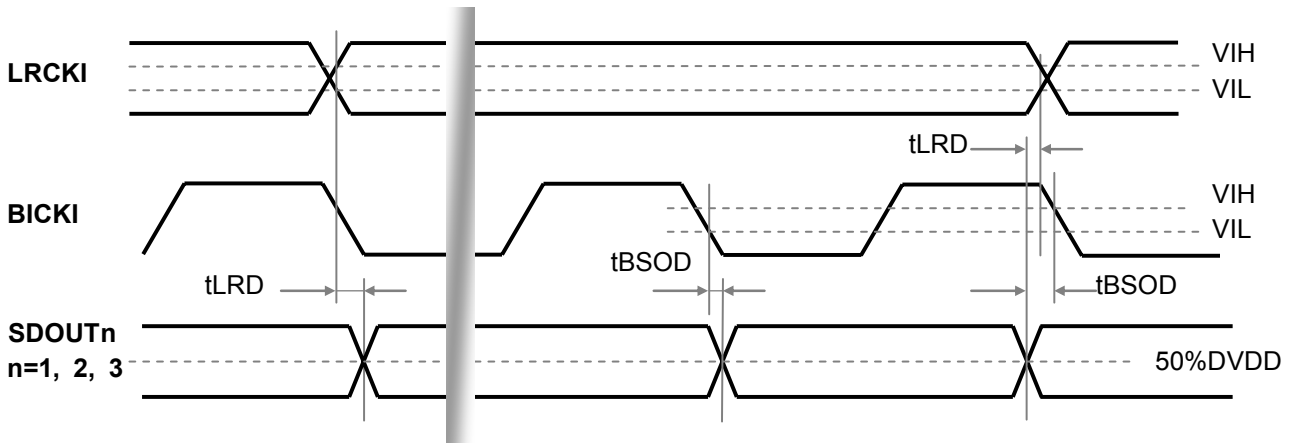


Figure 9. Output Interface in Slave Mode

2) Micro-controller Interface

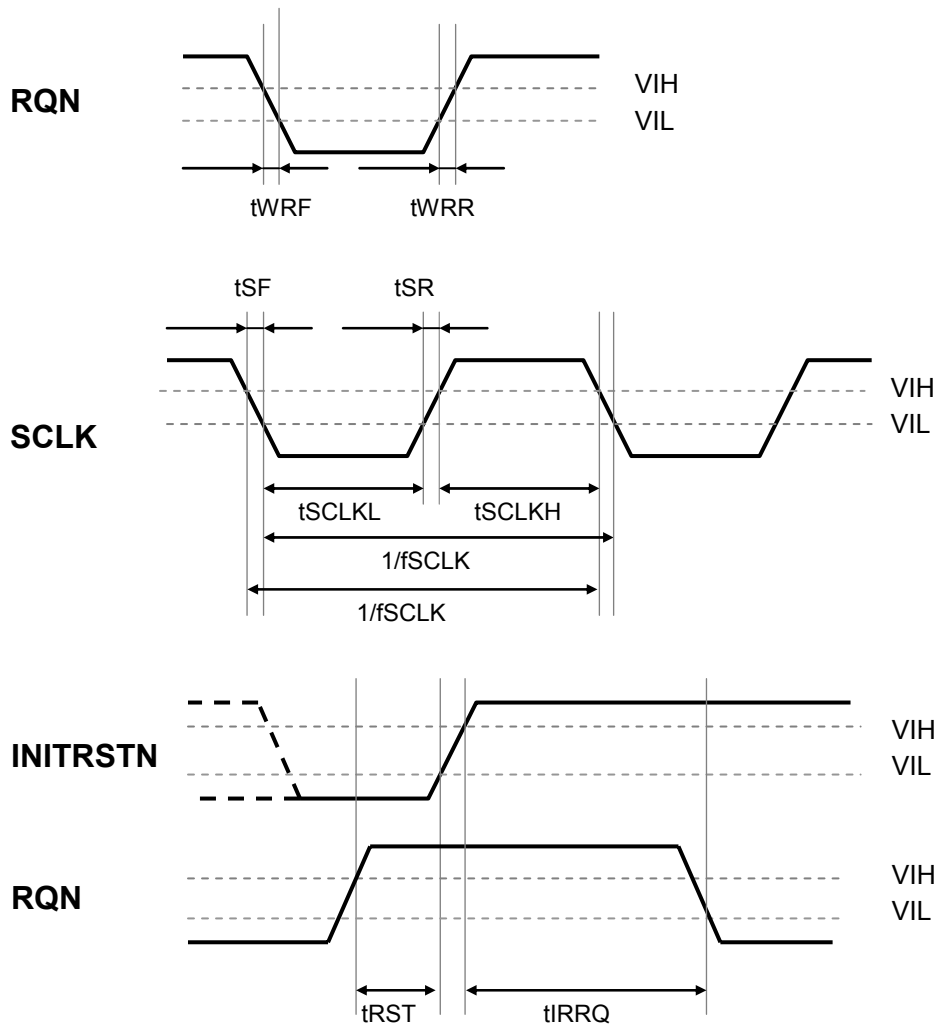


Figure 10. Micro-controller Interface Signal

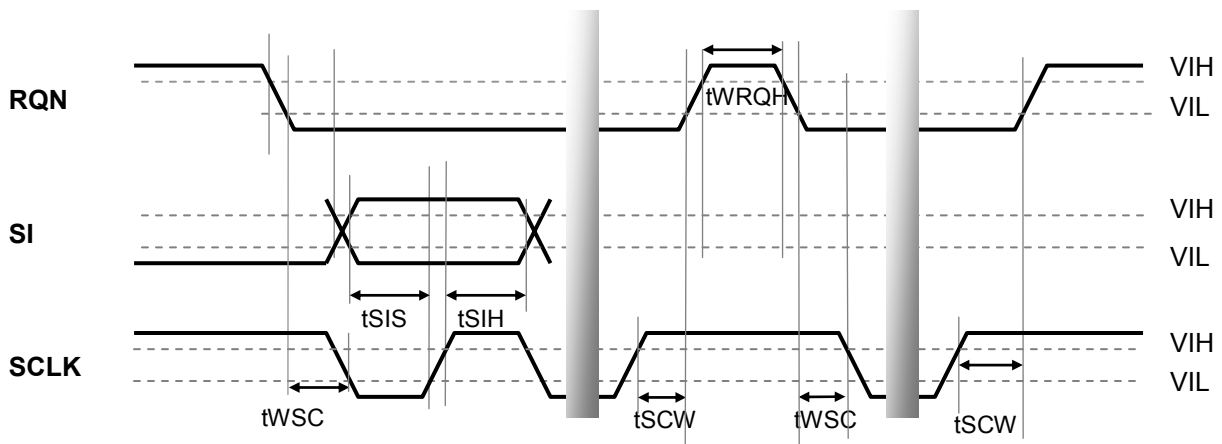


Figure 11. Micro-controller → AK7722

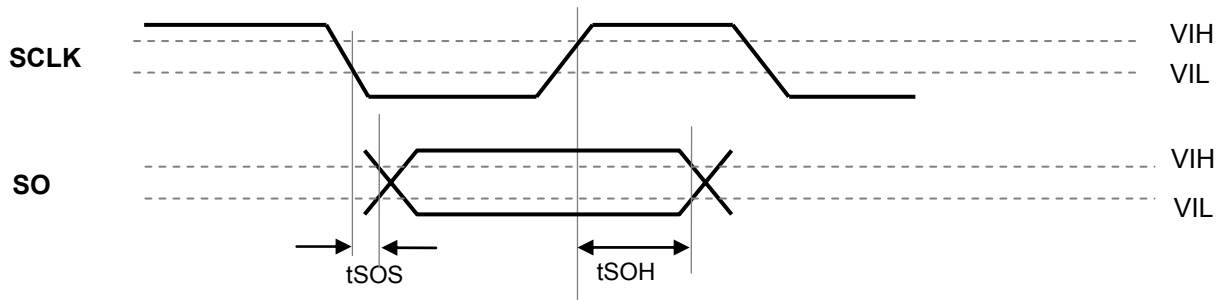


Figure 12. AK7722 → Micro-controller

3) I²C-Bus Interface

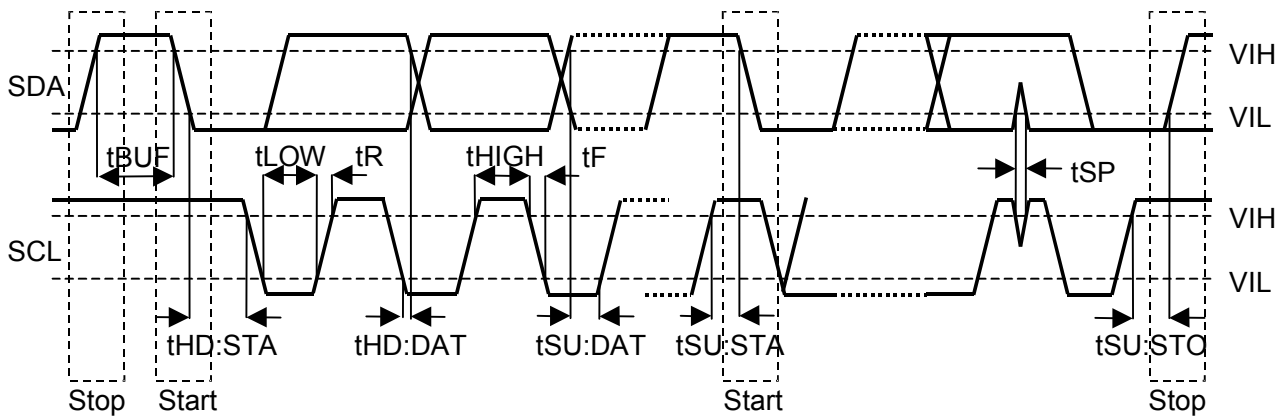
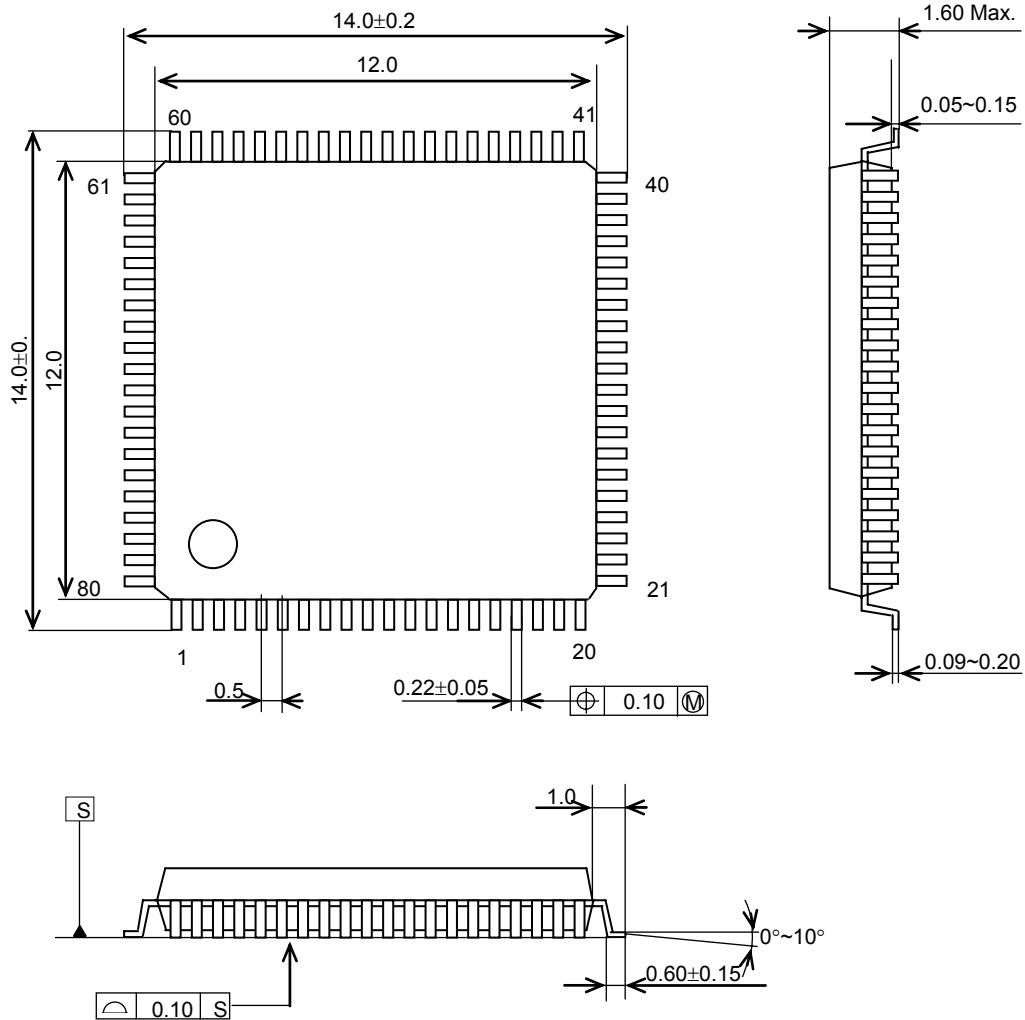


Figure 13. I²C-bus Interface

PACKAGE

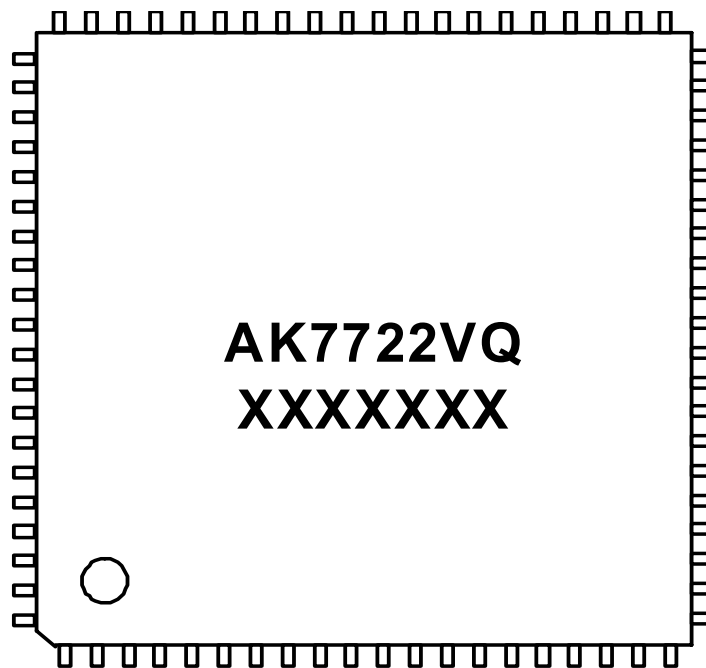
80pin LQFP (Unit: mm)



■ Materials and Lead Specification

- Package: Epoxy
- Lead frame: Copper
- Lead-finish: Soldering (Pb free) plate

MARKING



- 1) Pin#1 indication
- 2) Date Code: XXXXXXXX (7 digits)
- 3) Marking Code: AK7722VQ

REVISION HISTORY

| Date (YY/MM/DD) | Revision | Reason | Page | Contents |
|-----------------|----------|---------------|------|----------|
| 11/09/09 | 00 | First Edition | | |

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