



2.5V, 3.3V LVCMOS 1:9 Clock Fanout Buffer AK8180B

Features

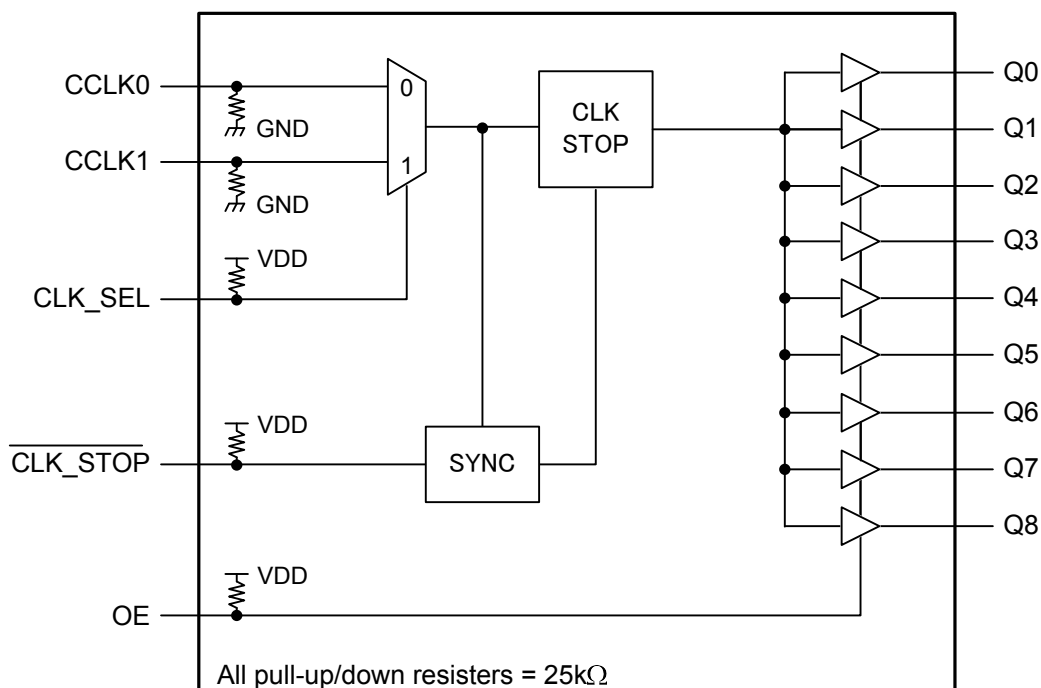
- 9 LVCMOS outputs
- Selectable LVCMOS inputs
- 2.5V or 3.3V power supply
- Clock frequency up to 350MHz
- Output-to-output skew : 150ps max
- Synchronous output stop in logic state
- High-impedance output control
- Drive up to 18 series terminated clock lines
- Operating Temperature Range: -40 to +85°C
- Package: 32-pin LQFP (Pb free)
- Pin compatible with MPC9447

Description

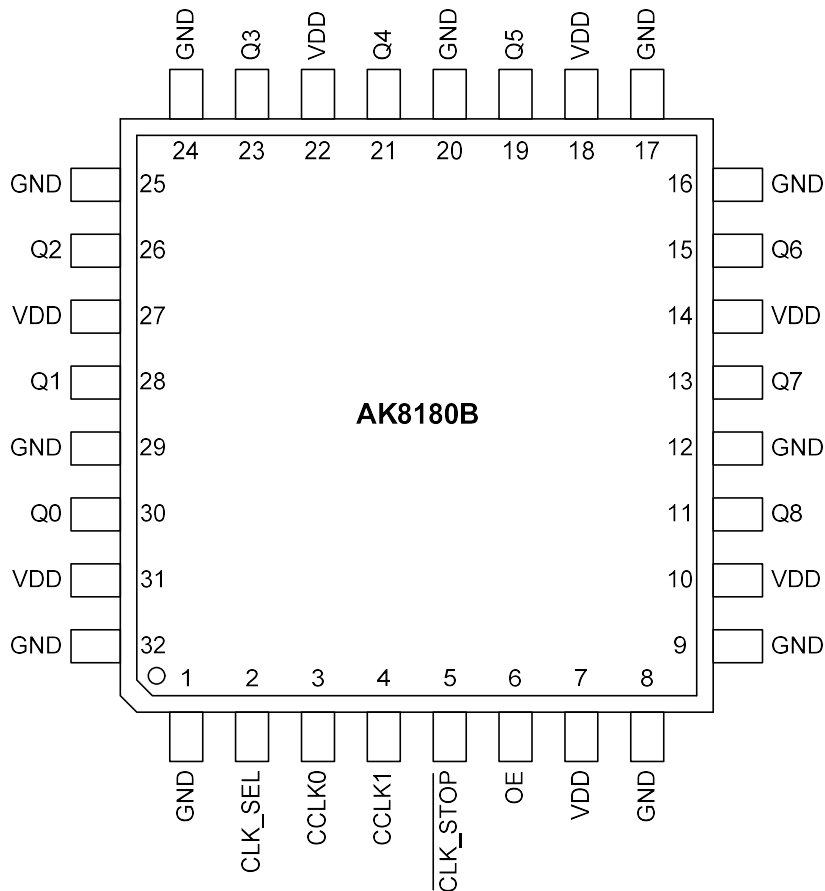
The AK8180B is a member of AKM's LVCMOS clock fanout buffer family designed for telecom, networking and computer applications, requiring a range of clocks with high performance and low skew. The AK8180B distributes 9 buffered clocks up to 350MHz. The 9 outputs can drive terminated 50 Ω clock lines. The CLK_STOP control allows the output signal to start and stop only in a logic low state. The OE control sets the outputs to high-impedance mode.

AK8180B are derived from AKM's long-term-experienced clock device technology, and enable clock output to perform low skew. The AK8180B is available in a 7mm x 7mm 32-pin LQFP package.

Block Diagram



Pin Descriptions



Package: 32-Pin LQFP(Top View)

| Pin No. | Pin Name | Pin Type | Pullup /down | Description |
|---------|----------|----------|--------------|--|
| 1 | GND | -- | -- | Ground |
| 2 | CLK_SEL | IN | PU | Clock Input Select |
| 3 | CCLK0 | IN | PD | Clock Input (LVCMOS) |
| 4 | CCLK1 | IN | PD | Clock Input (LVCMOS) |
| 5 | CLK_STOP | IN | PU | Clock Output Disable (Active low) |
| 6 | OE | IN | PU | Clock Output Enable (Disable=High impedance) |
| 7 | VDD | -- | -- | Power supply |
| 8, | GND | -- | -- | Ground |
| 9 | GND | -- | -- | Ground |
| 10 | VDD | -- | -- | Power supply |
| 11 | Q8 | OUT | -- | Clock output |
| 12 | GND | -- | -- | Ground |

PU: Pull up PD: Pull down

(continued on next page)

| Pin No. | Pin Name | Pin Type | Pullup /down | Description |
|---------|----------|----------|--------------|--------------|
| 13 | Q7 | OUT | -- | Clock output |
| 14 | VDD | -- | -- | Power supply |
| 15 | Q6 | OUT | -- | Clock output |
| 16 | GND | -- | -- | Ground |
| 17 | GND | -- | -- | Ground |
| 18 | VDD | -- | -- | Power supply |
| 19 | Q5 | OUT | -- | Clock output |
| 20 | GND | -- | -- | Ground |
| 21 | Q4 | OUT | -- | Clock output |
| 22 | VDD | -- | -- | Power supply |
| 23 | Q3 | OUT | -- | Clock output |
| 24 | GND | -- | -- | Ground |
| 25 | GND | -- | -- | Ground |
| 26 | Q2 | OUT | -- | Clock output |
| 27 | VDD | -- | -- | Power supply |
| 28 | Q1 | OUT | -- | Clock output |
| 29 | GND | -- | -- | Ground |
| 30 | Q0 | OUT | -- | Clock output |
| 31 | VDD | -- | -- | Power supply |
| 32 | GND | -- | -- | Ground |

Ordering Information

| Part Number | Marking | Shipping Packaging | Package | Temperature Range |
|-------------|---------|--------------------|-------------|-------------------|
| AK8180B | AK8180B | Tape and Reel | 32-pin LQFP | -40 to 85 °C |

Absolute Maximum Rating

Over operating free-air temperature range unless otherwise noted ⁽¹⁾

| Items | Symbol | Ratings | Unit |
|--|------------------|--------------------|------|
| Supply voltage | VDD | -0.3 to 4.6 | V |
| Input voltage | V _{in} | GND-0.3 to VDD+0.3 | V |
| Input current (any pins except supplies) | I _{IN} | ±10 | mA |
| Storage temperature | T _{stg} | -55 to 130 | °C |

Note

(1) Stress beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under “Recommended Operating Conditions” is not implied. Exposure to absolute-maximum-rating conditions for extended periods may affect device reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.



ESD Sensitive Device

This device is manufactured on a CMOS process, therefore, generically susceptible to damage by excessive static voltage. Failure to observe proper handling and installation procedures can cause damage. AKM recommends that this device is handled with appropriate precautions.

Recommended Operation Conditions

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|-------------------------------|----------------|------------|-------|-----|-------|------|
| Operating temperature | T _a | | -40 | | 85 | °C |
| Supply voltage ⁽¹⁾ | VDD | VDD±5% | 2.375 | 2.5 | 2.625 | V |
| | | | 3.135 | 3.3 | 3.465 | |

(1) Power of 2.5V or 3.3V requires to be supplied from a single source. A decoupling capacitor of 0.01μF for power supply line should be located close to each VDD pin.

General Specification

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|-------------------------------|-----------------|------------------|------|-------|-----|------|
| Output Termination Voltage | V _{TT} | | | VDD/2 | | V |
| ESD Protection 1 | MM | Machine model | 200 | | | V |
| ESD Protection 2 | HBM | Human Body Model | 2000 | | | V |
| Latch-Up Immunity | LU | | 200 | | | mA |
| Power Dissipation Capacitance | | Per output | | 10 | | pF |
| Input Capacitance | | | | 4.0 | | pF |

Power Supply Current <3.3V>

VDD= 3.3V±5%, Ta: -40 to +85°C

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|-----------------------------------|--------|---------------------------|-----|-----|-----|------|
| Full operation ⁽¹⁾ | IDD1 | CCLK0=350MHz CLK_SEL=L | | 120 | 140 | mA |
| Quiescent state ⁽¹⁾⁽²⁾ | IDD2 | | | 1.0 | 2.0 | mA |

(1) The outputs have no loads. (2) All inputs are in default state by the internal pull up/down resistors.

DC Characteristics <3.3V>

All specifications at VDD= 3.3V±5%, Ta: -40 to +85°C, unless otherwise noted

| Parameter | Symbol | Conditions | MIN | TYP | MAX | Unit |
|------------------------------|-----------------|--|------|-----|--------------|------|
| High Level Input Voltage | V _{IH} | LVC MOS | 2.0 | | VDD+0.3 | V |
| Low Level Input Voltage | V _{IL} | LVC MOS | -0.3 | | 0.8 | V |
| Input Current ⁽¹⁾ | I _{L1} | V _{in} =GND or VDD | -300 | | +300 | μA |
| High Level Output Voltage | V _{OH} | I _{OH} = -24mA ⁽²⁾ | 2.4 | | | V |
| Low Level Output Voltage | V _{OL} | I _{OL} = +24mA I _{OL} = +12mA | | | 0.55 0.30 | V |
| Output Impedance | | | | 17 | | Ω |

(1) Input pull-up / pull down resistors influence input current.

(2) The AK8180B is capable of driving 50 Ω transmission lines of the incident edge. Each output drives one 50 Ω parallel terminated transmission line to a termination voltage of VTT. Alternatively, the device drives up to two 50 Ω series terminated transmission lines (for VDD=3.3V) or one 50 Ω series terminated transmission line (for VDD=2.5V).

AC Characteristics <3.3V> ⁽¹⁾

All specifications at VDD= 3.3V±5%, Ta: -40 to +85°C, unless otherwise noted

| Parameter | Symbol | Conditions | MIN | TYP | MAX | Unit |
|-------------------------------------|--------------------------------------|--|-----|-----|-----|------|
| Input Frequency | f _{IN} | Pin: CCLK | 0 | | 350 | MHz |
| Input Pulse Width | t _{pWIN} | Pin: CCLK | 1.4 | | | ns |
| Input Rise/Fall time ⁽³⁾ | t _{rIN} , t _{fOUT} | Pin: CCLK 0.8 to 2.0V | | | 1.0 | ns |
| Output Frequency | f _{OUT} | Pin: Q0-8 | 0 | | 350 | MHz |
| Propagation Delay | t _{PLH} , t _{PHL} | CCLK to any Q | 0.8 | 1.6 | 2.8 | ns |
| Output Disable Time | t _{PLZ} , t _{PHZ} | | | | 11 | ns |
| Output Enable Time | t _{PZL} , t _{PZH} | | | | 11 | ns |
| Setup Time | t _S | CCLK to $\overline{\text{CLK_STOP}}$ | 0.0 | | | ns |
| Hold Time | t _H | CCLK to $\overline{\text{CLK_STOP}}$ | 1.0 | | | ns |
| Output-to-Output Skew | t _{skPP} | | | | 150 | ps |
| Device-to-Device Skew | t _{skD} | | | | 2.0 | ns |
| Output Pulse Skew ⁽⁴⁾ | t _{skO} | CCLK | | | 300 | ps |
| Output Duty Cycle | DC _{OUT} | f _{OUT} < 170MHz DC _{REF} =50% | 45 | 50 | 55 | % |
| Output Rise/Fall Time | t _r , t _f | 0.55 to 2.4V | 0.1 | | 1.0 | ns |
| Cycle-to-Cycle Jitter | t _{JITCC} | 1 σ | | 6 | | ps |

(1) AC characteristics apply for parallel output termination of 50 Ω to VTT.

(2) V_{cmr}(AC) is the crosspoint of the differential input signal. Normal AC operation is obtained when the crosspoint is within the V_{cmr} range and the input swing lies within the V_{pp}(AC) specification. Violation of V_{cmr} or V_{pp} impacts t_{PLH/PHL} and t_{skD}.

(3) Violation of the 1.0 ns maximum input rise and fall time limit will affect the device propagation delay, device-to-device skew, input pulse width, output duty cycle and maximum frequency specifications.

(4) Output pulse skew t_{skO} is the absolute difference of the propagation delay times: | t_{PLH} - t_{PHL} |.

Power Supply Current <2.5V>

VDD= 2.5V±5%, Ta: -40 to +85°C

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|-----------------------------------|--------|---------------------------|-----|-----|-----|------|
| Full operation ⁽¹⁾ | IDD1 | CCLK0=350MHz CLK_SEL=L | | 95 | 115 | mA |
| Quiescent state ⁽¹⁾⁽²⁾ | IDD2 | | | 0.7 | 1.3 | mA |

(1) The outputs have no loads. (2) All inputs are in default state by the internal pull up/down resistors.

DC Characteristics <2.5V>

All specifications at VDD= 2.5V±5%, Ta: -40 to +85°C, unless otherwise noted

| Parameter | Symbol | Conditions | MIN | TYP | MAX | Unit |
|------------------------------|-----------------|--|------|-----|---------|------|
| High Level Input Voltage | V _{IH} | LVC MOS | 1.7 | | VDD+0.3 | V |
| Low Level Input Voltage | V _{IL} | LVC MOS | -0.3 | | 0.7 | V |
| Input Current ⁽¹⁾ | I _{L1} | V _{in} =GND or VDD | -300 | | +300 | μA |
| High Level Output Voltage | V _{OH} | I _{OH} = -15mA ⁽²⁾ | 1.8 | | | V |
| Low Level Output Voltage | V _{OL} | I _{OL} = +15mA | | | 0.6 | V |
| Output Impedance | | | | 19 | | Ω |

(1) Input pull-up / pull down resistors influence input current.

(2) The AK8180B is capable of driving 50 Ω transmission lines of the incident edge. Each output drives one 50 Ω parallel terminated transmission line to a termination voltage of VTT. Alternatively, the device drives up to two 50 Ω series terminated transmission lines(for VDD=3.3V) or one 50 Ω series terminated transmission lines(for VDD=2.5V).

AC Characteristics <2.5V> ⁽¹⁾

All specifications at VDD= 2.5V±5%, Ta: -40 to +85°C, unless otherwise noted

| Parameter | Symbol | Conditions | MIN | TYP | MAX | Unit |
|-------------------------------------|---------------------------------------|---------------------------------------|-----|-----|-----|------|
| Input Frequency | f _{IN} | Pin: CCLK | 0 | | 350 | MHz |
| Input Pulse Width | t _{pWIN} | Pin: CCLK | 1.4 | | | ns |
| Input Rise/Fall time ⁽³⁾ | t _{rIN} , t _{fOUT} | Pin: CCLK 0.8 to 2.0V | | | 1.0 | ns |
| Output Frequency | f _{OUT} | Pin: Q0-8 | 0 | | 350 | MHz |
| Propagation Delay | t _{PLH} , t _{PHL} | CCLK to any Q | 0.9 | 1.8 | 3.6 | ns |
| Output Disable Time | t _{P LZ} , t _{P HZ} | | | | 11 | ns |
| Output Enable Time | t _{P ZL} , t _{P ZH} | | | | 11 | ns |
| Setup Time | t _S | CCLK to $\overline{\text{CLK_STOP}}$ | 0.0 | | | ns |
| Hold Time | t _H | CCLK to $\overline{\text{CLK_STOP}}$ | 1.0 | | | ns |
| Output-to-Output Skew | t _{skPP} | | | | 150 | ps |
| Device-to-Device Skew | t _{skD} | | | | 2.7 | ns |
| Output Pulse Skew ⁽⁴⁾ | t _{skO} | CCLK | | | 200 | ps |
| Output Duty Cycle | DC _{OUT} | DC _{REF} =50% | 45 | 50 | 55 | % |
| Output Rise/Fall Time | t _r , t _f | 0.6 to 1.8V | 0.1 | | 1.0 | ns |
| Cycle-to-Cycle Jitter | t _{JITCC} | 1 σ | | 10 | | ps |

(1) AC characteristics apply for parallel output termination of 50 Ω to VTT.

(2) V_{cmr}(AC) is the crosspoint of the differential input signal. Normal AC operation is obtained when the crosspoint is within the V_{cmr} range and the input swing lies within the V_{pp}(AC) specification. Violation of V_{cmr} or V_{pp} impacts t_{PLH/PHL} and t_{skD}.

(3) Violation of the 1.0 ns maximum input rise and fall time limit will affect the device propagation delay, device-to-device skew, input pulse width, output duty cycle and maximum frequency specifications.

(4) Output pulse skew t_{skO} is the absolute difference of the propagation delay times: | t_{PLH} - t_{PHL} |.

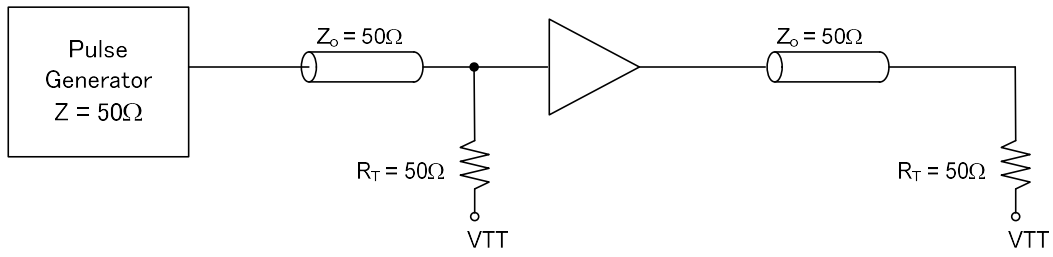


Figure 1 CCLK AC Test Reference

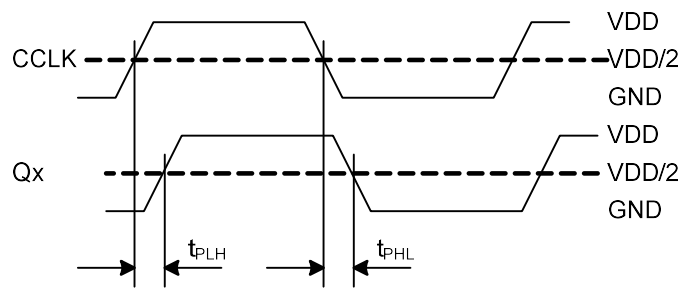
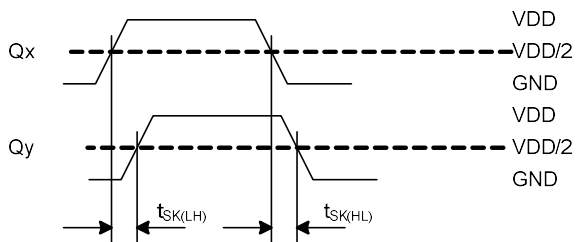
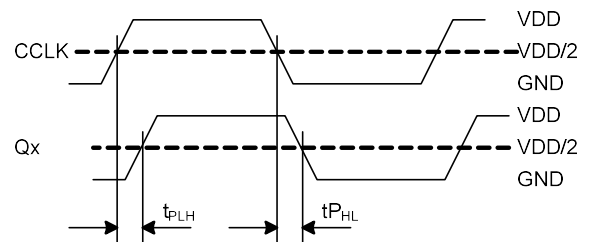


Figure 2 Propagation Delay Test Reference



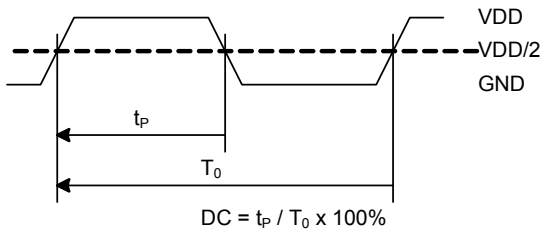
The pin-to-pin skew is defined as the worst case difference in propagation delay between any two similar delay paths within a single device.



$$t_{skP} = |t_{PLH} - t_{PHL}|$$

Figure 3 Output-to-Output Skew

Figure 4 Output Pulse Skew Test Reference



The time from the PLL controlled edge to the non controlled edge, divided by the time between PLL controlled edges, expressed as a percentage.

Figure 5 Output Duty Cycle

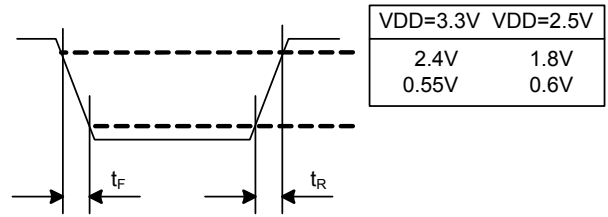


Figure 6 Output Translation Test Reference

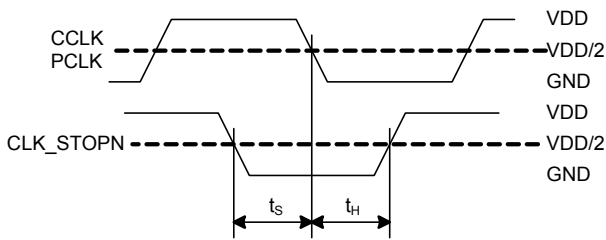
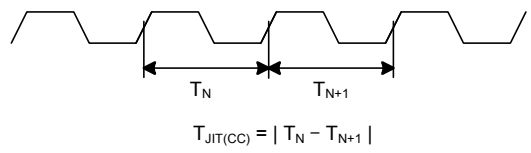


Figure 7 Setup and Hold Time Test Reference



The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs.

Figure 8 Cycle-to-Cycle Jitter

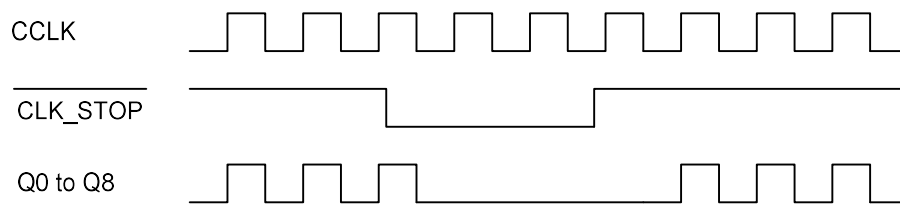
Function Table

The following table shows the inputs/outputs clock state configured through the control pins.

Table 1: Control-Pin-Setting Function Table

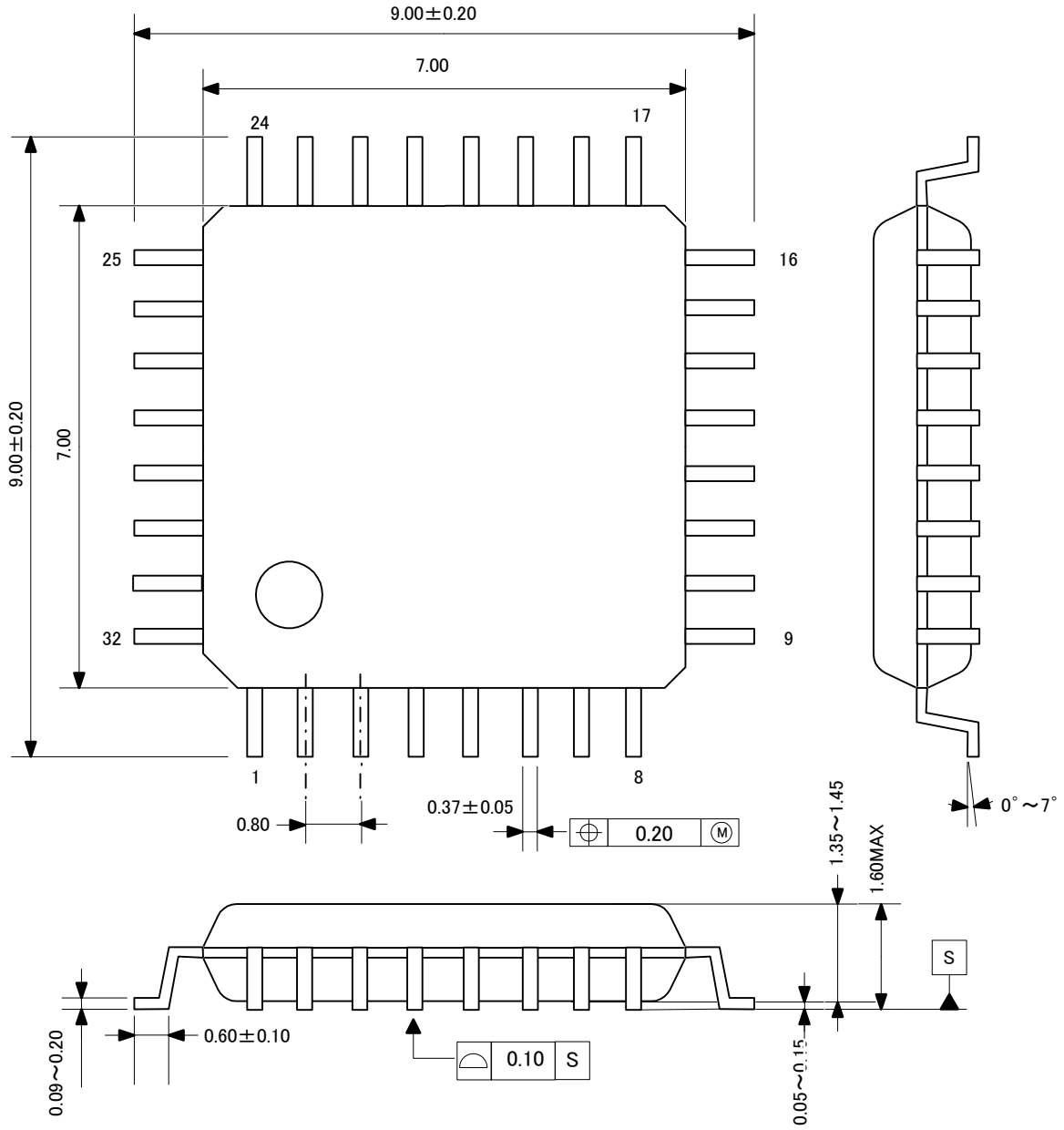
| Control Pin | Default | 0 | 1 |
|-------------------------------|---------|---|----------------------|
| CLK_SEL | 1 | CCLK0 input selected | CCLK1 input selected |
| OE | 1 | Outputs disabled. (high impedance) | Outputs enabled |
| $\overline{\text{CLK_STOP}}$ | 1 | Outputs synchronously stopped in logic low state. | Outputs active |

Application example of $\overline{\text{CLK_STOP}}$



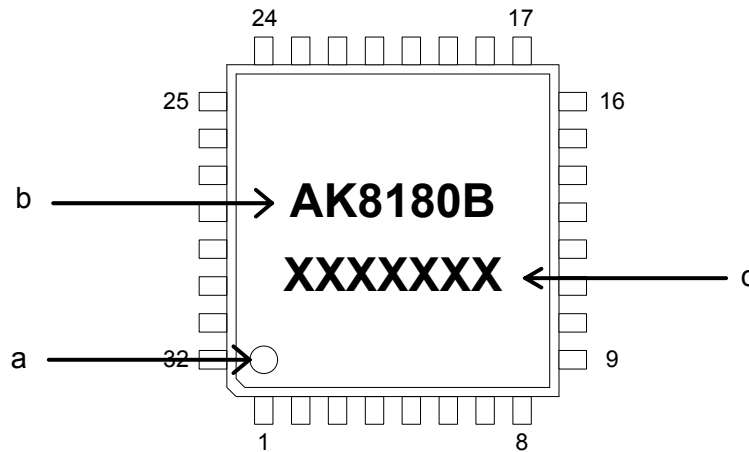
Package Information

- Mechanical data : 32-lead LQFP




• **Marking**

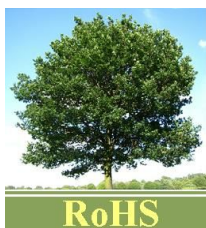
- a: #1 Pin Index
- b: Part number
- c: Date code (7 digits)



(1) **AKM** is the brand name of AKM's IC's.

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(*) RoHS compliant products from AKM are identified with "Pb free" letter indication on product label posted on the anti-shield bag and boxes.

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